

SIGMA 5/7
TROUBLESHOOTING HANDBOOK

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Prepared by
Field Engineering Publications

FOREWORD

This handbook contains troubleshooting information for both the Sigma 5 and the Sigma 7 Computers. Troubleshooting information for the Sigma 5 was formerly issued under publication No. 65-50-xx while the Sigma 7 was issued under publication No. 65-70-xx. This handbook includes the information from both the Sigma 5 and Sigma 7 Handbooks and also contains information not previously covered in either handbook. The handbook is divided into three sections as follows:

Section I - Sigma 5 information

Section II - Sigma 7 information

Section III - Information common to both the Sigma 5 and Sigma 7.

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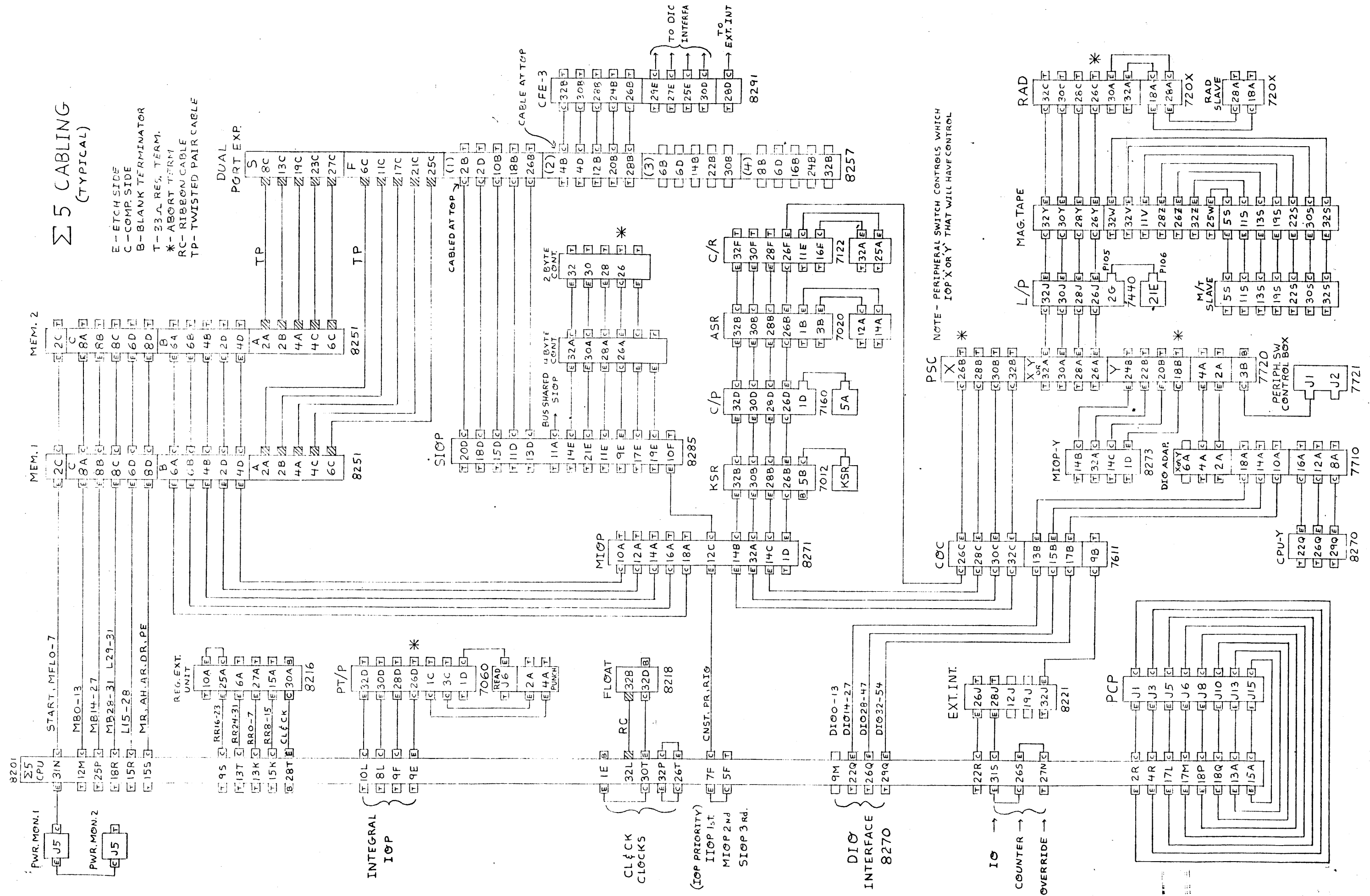
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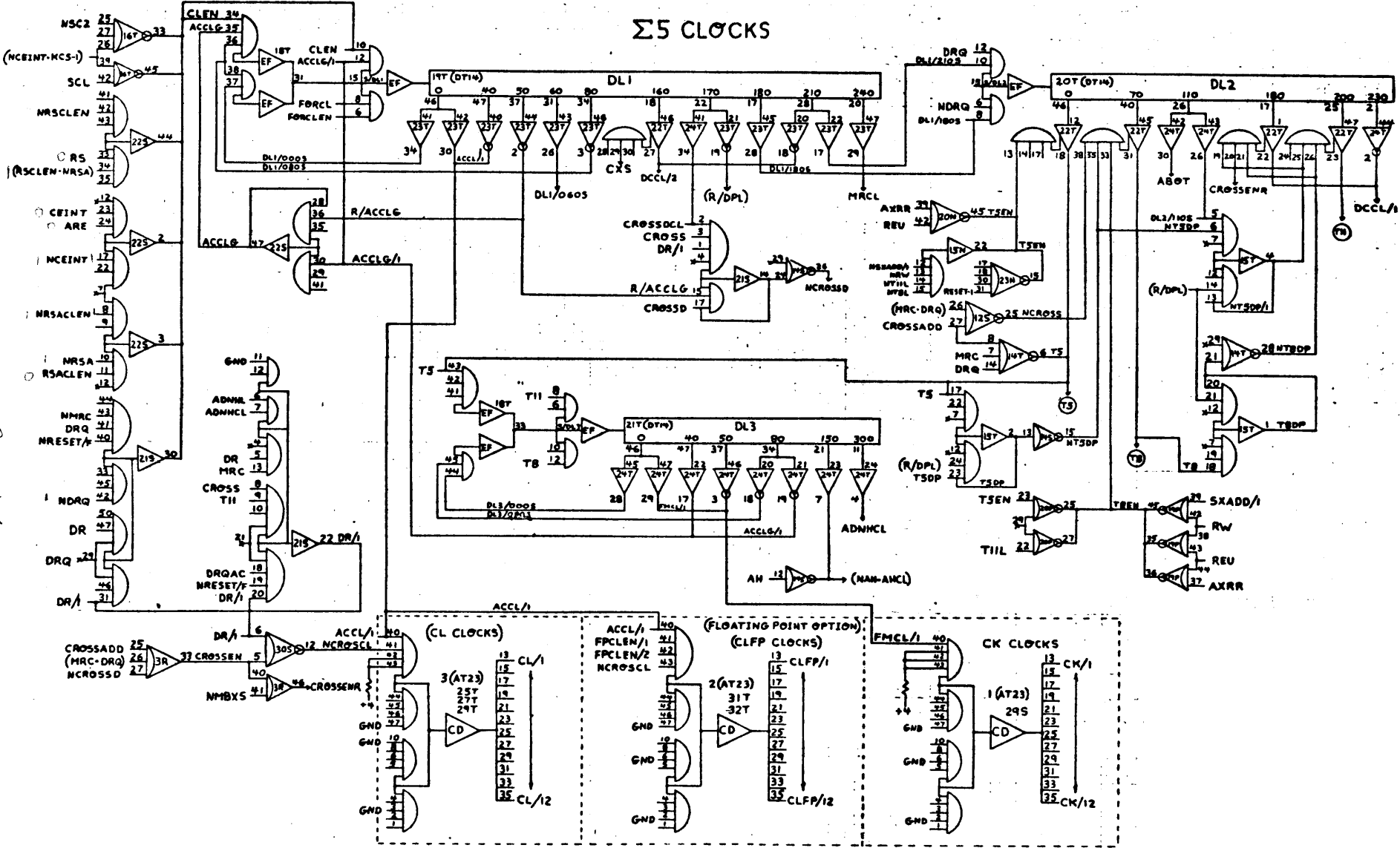
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Σ 5 CABLING (TYPICAL)

- E- ETCH SIDE
- C- COMP. SIDE
- B- BLANK TERMINATOR
- T- 33Ω RES. TERM.
- *- ABORT TERM.
- RC- RIBBON CABLE
- TP- TWISTED PAIR CABLE

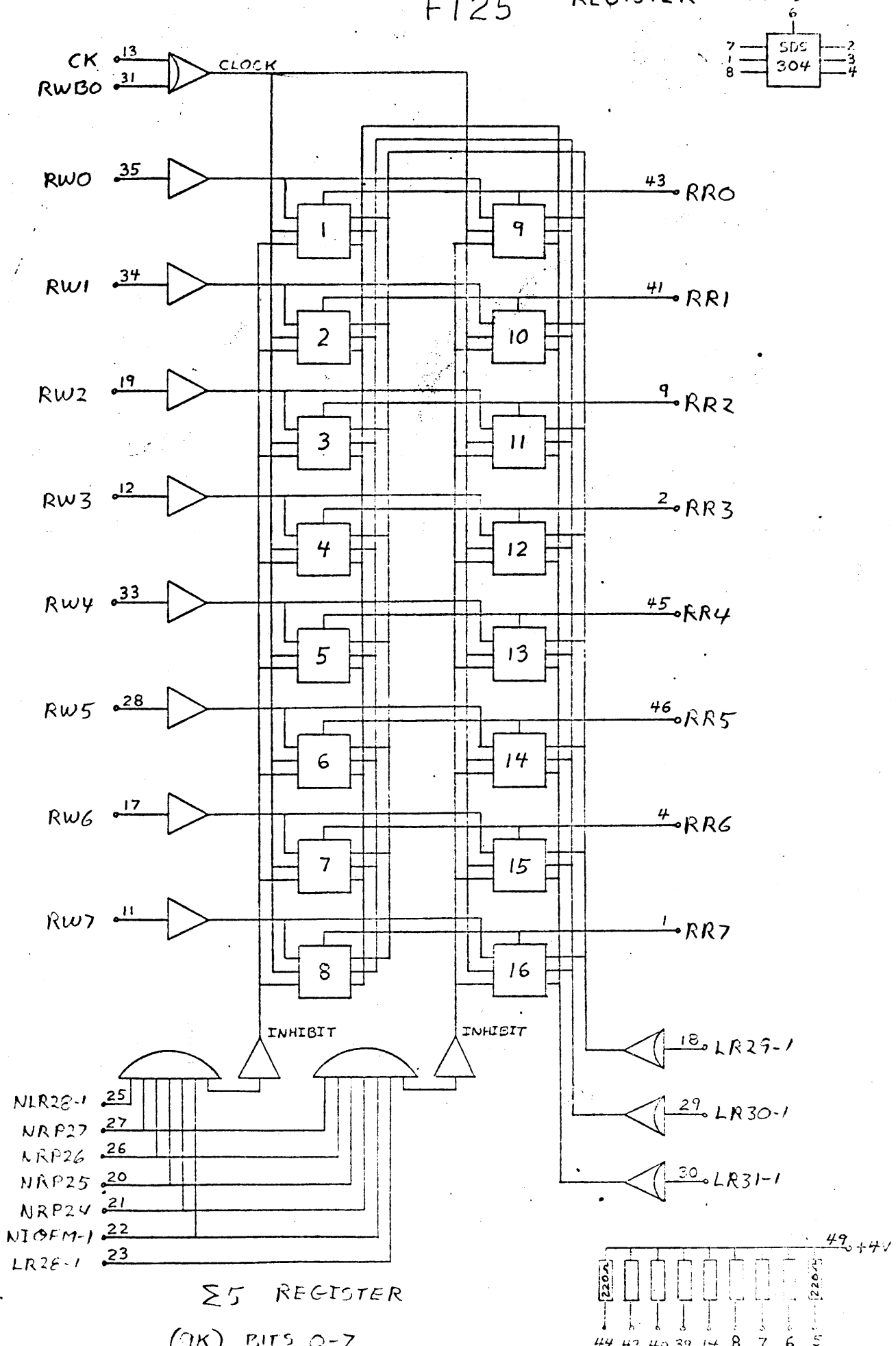


Σ5 CLOCKS



Page 1-4

FT25 REGISTER (9K)

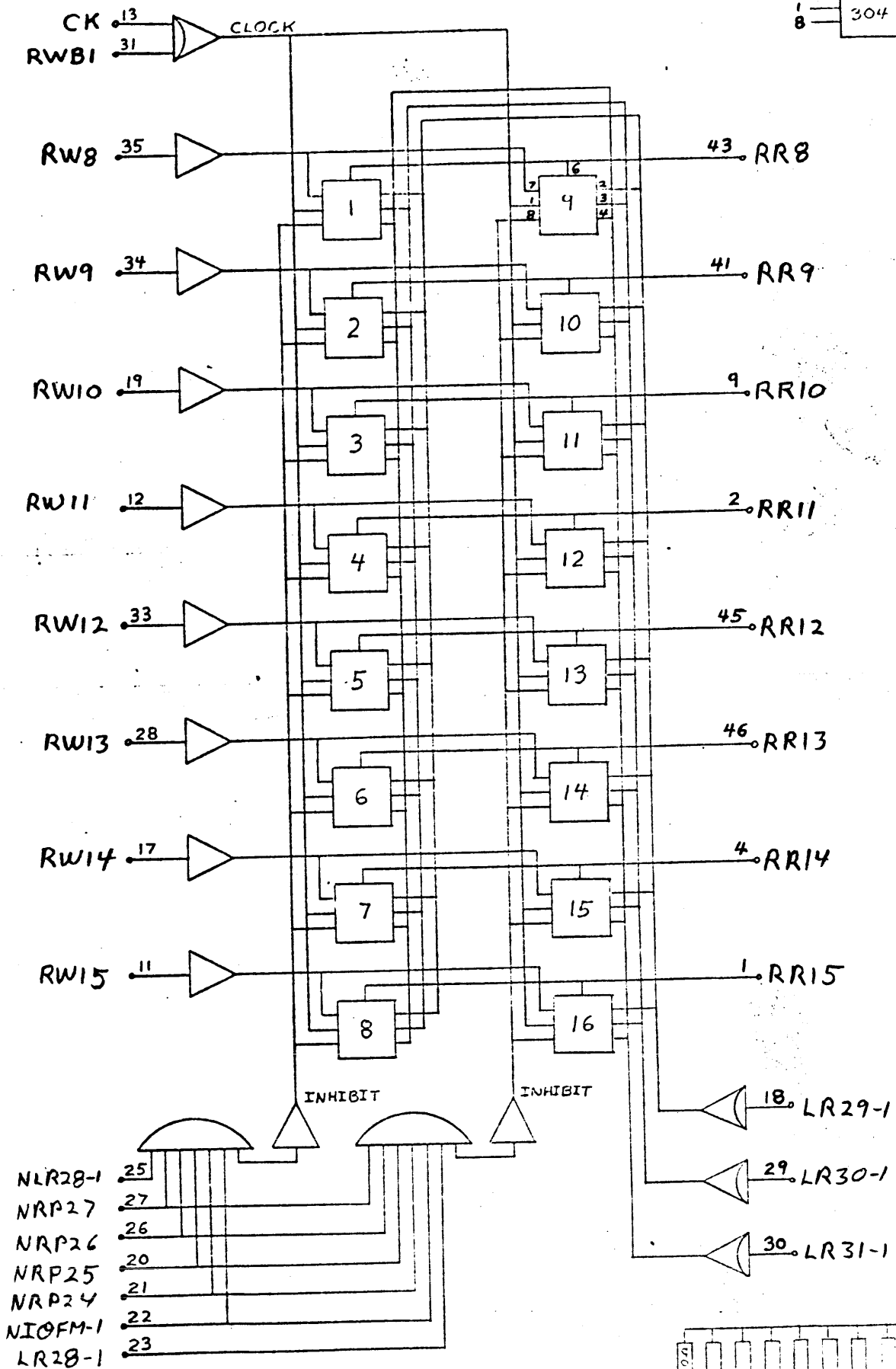
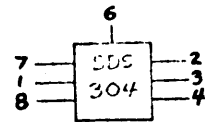


Σ5 REGISTER

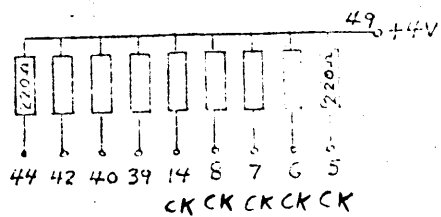
(9K) BITS 0-7

FT25

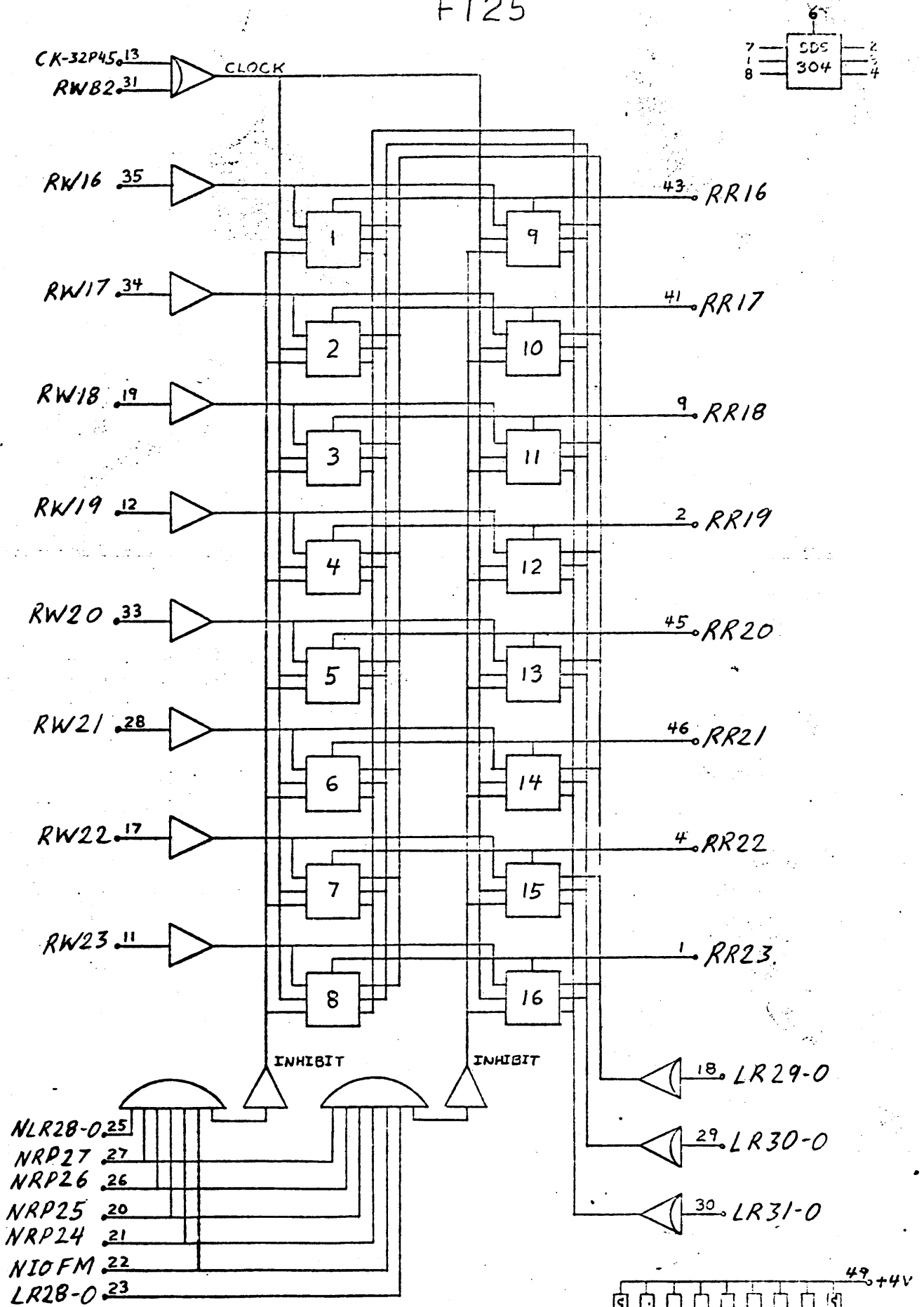
REGISTER (19K)



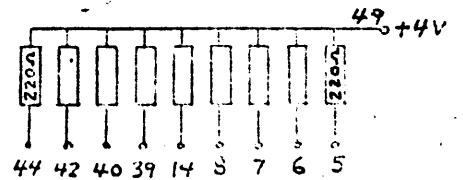
Σ5 REGISTER
 (19K) BITS 8-15



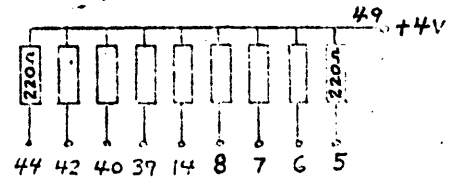
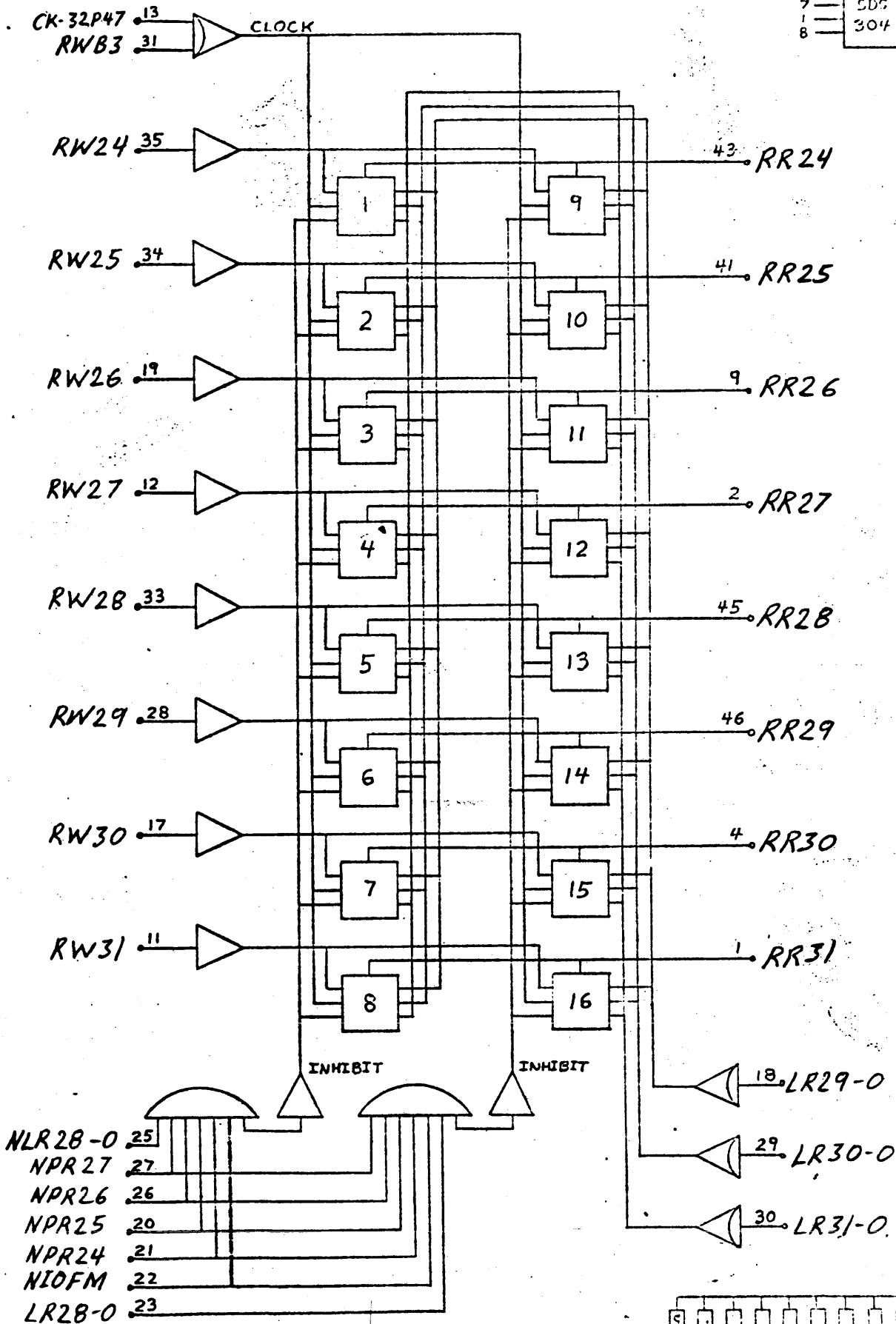
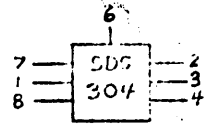
FT25



{ 5 Register.
(55) Bits 16-23



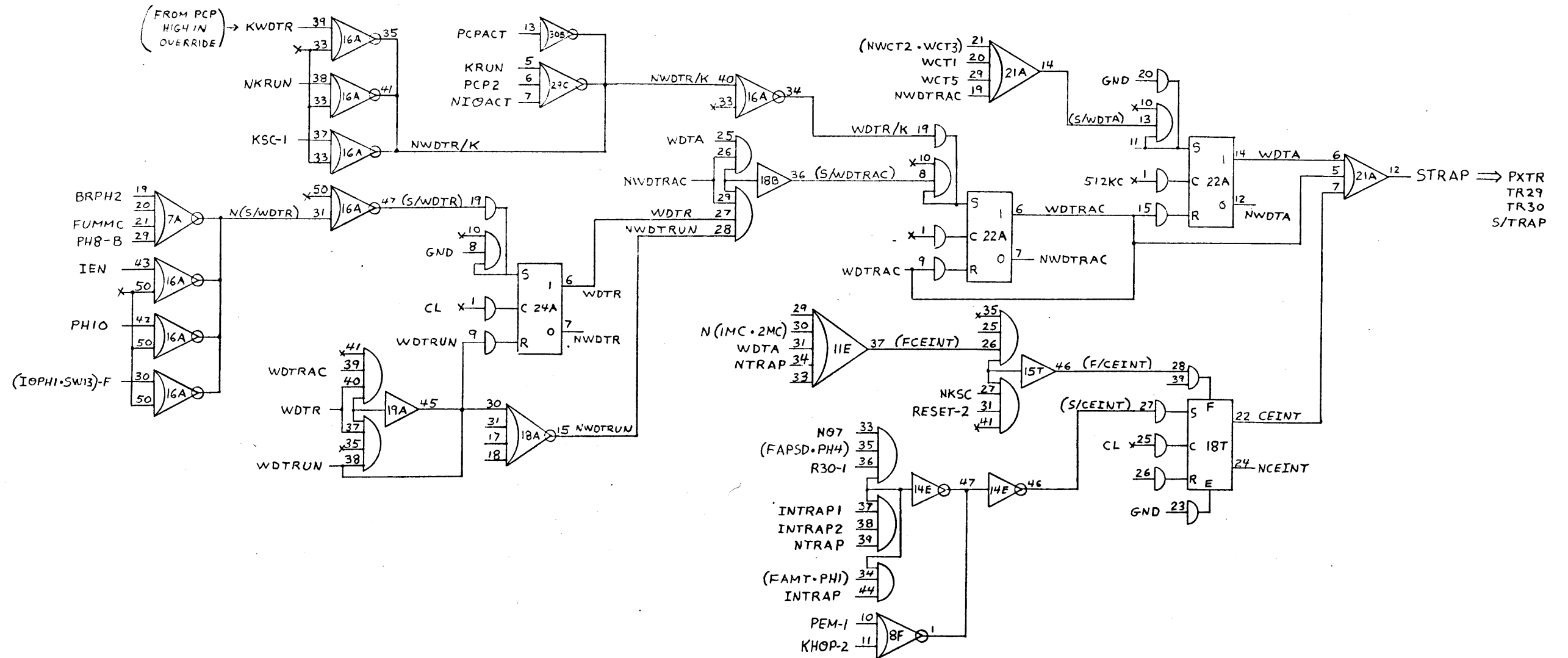
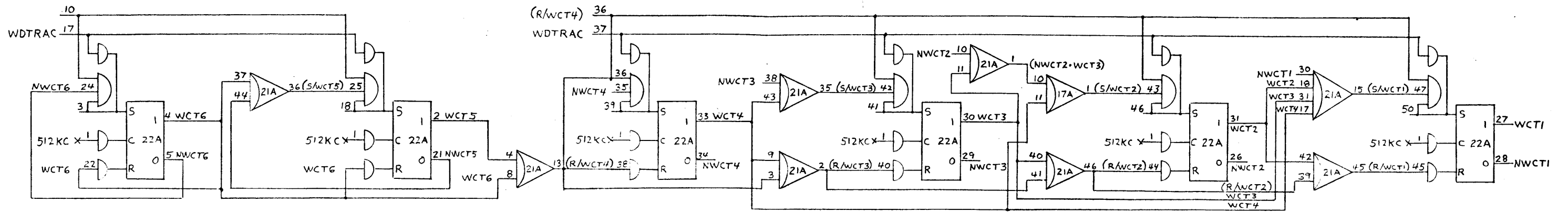
FT25



{ 5 Register.
 (9T) Bits 24-31

Σ5 WATCHDOG TIMER TRAP (46)

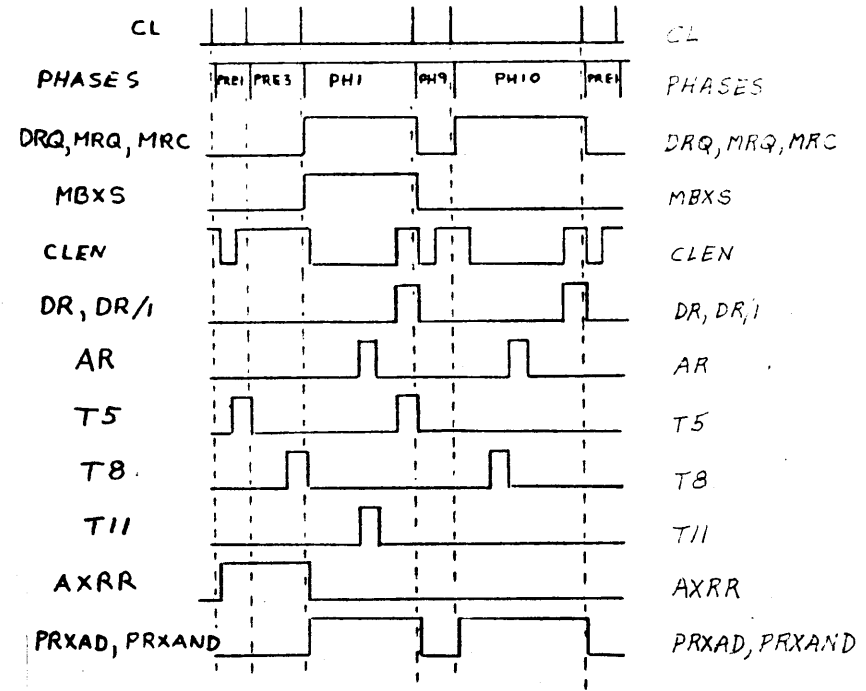
6/1/68
TO 'G' REV.
Cochrane



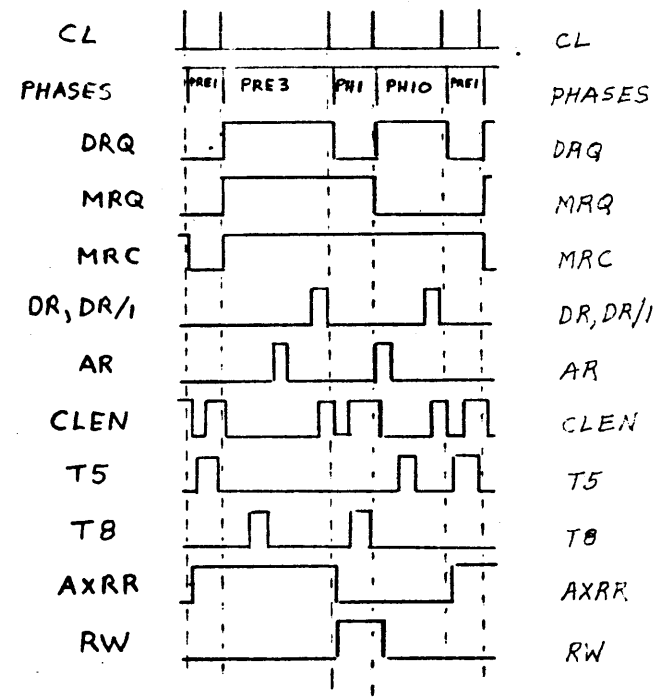
STW
35C0 0100 f HOLD SW ON

Σ5 TIMING STW & LW

Colman



LW
32C0 0100 f HOLD SW ON



SIGMA 5 FAMILY TERMS

FABYTE	08B47	FUBAL	03B46
FACAL	08A36	FUBCR	12C01
FACOMP	10B12	FUBCS	03B44
FACOMP/1	08B17	FUBDR	12C45
FACOMP/L	08B45	FUBIR	12035
FADIV	07A36	FUEXU	09B45
FADIVH	04B18	FUINT	03B36
FADW	08B46	FULAD	08A01
FADW/1	08A35	FULAWORDW	14F34
FAFL	03A10	FULRP	04B44
FAHW	08B36	FUMH	04B10
FAILL	04B45	FUMI	17A36
FAILL/1	30C10	FUMMC	03B41
FAIM	08B44	FUMSP	08B11
FAIO	07A02	FUMTHOVER	26N19
FAIO/1	04B47	FUMTSIGN	18B47
FALCF	11A10	FUPLM	08A46
FALCFP	09A01	FUPSW	03B28
FALOAD	11A28	FUPLW	03B27
FALOAD/A	08A02	FUS	04B05
FALOAD/C	04B25	FUSE	04B17
FAMDS	04B15	FUSEF/1	32E18
FAMDST	30D13	FUSIO	28F19
FAMT	03B06	FUMAIT	08A45
FAMUL	07A35	FUXW	03B19
FAMULNH	04B11		
FANIMP	11B46		
FAPRIV	08A13		
FAPSD	08B10		
FARWD	03B35		
FASIO	08B18		
FASLL	08B35		
FASEL	09A13		
FASH	07A01		
FAST-1	07A45		
FAST/A-1	05044		
FAST/C	07A46		
FAST/L	03B25		
FAST/M	10B45		
FST/S	03B26		
FASTORE	08B06		
FASTORE/1	10B01		
FASTORE/3	08A15		
FASUB	07A34		
FAW	07A34		
FAWORDW	09A02		
FUAIO	03B45		
FUANLZ	03B05		
FUAWM	03B47		

SIGMA 5 PHASE LOCATIONS

PCP PHASES

PCP 1	29A02 \
PCP 2	28A27
PCP 3	28A31
PCP 4	28A30
PCP 5	29A14
PCP 6	28A33

PRE PHASES

PRE 1	31A07
PRE 2	31A27
PRE 3	32A07
PRE 4	31A31

EXECUTION PHASES

PH 1	31A30
PH 2	31A33
PH3	31A02
PH 4	31A04
PH 5	32A27
PH 6	32A31
PH 7	32A30
PH 8	32A33
PH 9	32A02
PH10	32A04

A REGISTER (FF)

	<u>A</u>	<u>NA</u>	<u>Set/A</u>	<u>Reset/A</u>	<u>Extra Set gates</u>	<u>Extra Reset gates</u>
0	3L33	3L40	3L36	3L30	2L-5L	5L
1	3L25	3L26	3L31	3L24	2L-5L	
2	3L19	3L21	3L20	3L17	2L-5L	
3	3L05	3L22	3L12	3L03	2L-5L	
4	4L33	4L40	4L36	4L30	2L-5L	
5	4L25	4L26	4L31	4L24	2L-5L	
6	4L19	4L21	4L20	4L17	2L-5L	
7	4L05	4L22	4L12	4L03	2L-5L	
8	3M23	3M25	3M12	3M02	2M	
9	3M19	3M21	3M28	3M02	2M	
10	3M31	3M29	3M27	3M02	2M	
11	3M27	3M22	3M35	3M02	2M	
12	4M23	4M25	4M12	4M02	2M	
13	4M19	4M21	4M28	4M02	2M	
14	4M31	4M29	4M37	4M02	2M	
15	4M27	4M22	4M35	4M02	2M	
16	14P23	14P25	14P12	14P02	16P	
17	14P19	14P21	14P28	14P02	16P	
18	14P31	14P29	14P37	14P02	16P	
19	14P27	14P22	14P35	14P02	16P	
20	15P23	15P25	15P12	15P02	16P	
21	15P19	15P21	15P28	15P02	16P	
22	15P31	15P29	15P37	15P02	16P	
23	15P27	15P22	15P35	15P02	16P	
24	14Q23	14Q25	14Q12	14Q02	16Q	
25	14Q19	14Q21	14Q28	14Q02	16Q	
26	14Q31	14Q29	14Q37	14Q02	16Q	
27	14Q27	14Q22	14Q35	14Q02	11Q-16Q	
28	15Q23	15Q25	15Q12	15Q02	13Q-16Q	
29	15Q19	15Q21	15Q28	15Q02	13Q-16Q	
30	15Q31	15Q29	15Q37	15Q02	13Q-16Q	
31	15Q27	15Q22	15Q35	15Q02	13Q-16Q	

ADDER (PR)

	<u>PR</u>
0	25L02
1	25L01
2	26L02
3	26L01
4	27L02
5	27L01
6	28L02
7	28L01
8	25M02
9	25M01
10	26M02
11	26M01
12	27M02
13	27M01
14	28M02
15	28M01
16	2P02
17	2P01
18	3P02
19	3P01
20	4P02
21	4P01
22	5P02
23	5P01
24	2Q02
25	2Q01
26	3Q02
27	3Q01
28	4Q02
29	4Q01
30	5Q02
31	5Q01

ADDER (G)

	<u>G</u>
0	25L06
1	25L04
2	26L06
3	26L04
4	27L06
5	27L04
6	28L06
7	28L04
8	25M06
9	25M04
10	26M06
11	26M04
12	27M06
13	27M04
14	28M06
15	28M04
16	2P06
17	2P04
18	3P06
19	3P04
20	4P06
21	4P04
22	5P06
23	5P04
24	2Q06
25	2Q04
26	3Q06
27	3Q04
28	4Q06
29	4Q04
30	5Q06
31	5Q04

ADDER (K)

	<u>K</u>
0	29K26
1	29K27
2	29K25
3	15N26
4	29K19
5	29K18
6	29K20
7	15N27
8	30K26
9	30K27
10	30K25
11	15N25
12	30K19
13	30K18
14	30K20
15	15N17
16	17N26
17	17N27
18	17N25
19	15N19
20	17N19
21	17N18
22	17N20
23	15N18
24	16N26
25	16N27
26	16N25
27	15N20
28	16N19
29	16N18
30	16N20
31	8P12

B REGISTER (FF)

	<u>B</u>	<u>NB</u>	<u>Set/B</u>	<u>Reset/B</u>	Extra <u>Set terms</u>
0	22L27	22L28	22L50	22L45	21L
1	22L31	22L26	22L46	22L44	21L
2	22L30	22L29	22L41	22L40	21L
3	22L33	22L34	22L39	22L38	21L
4	23L27	23L28	23L50	23L45	21L
5	23L31	23L26	23L46	23L44	21L
6	23L30	23L29	23L41	23L40	21L
7	23L33	23L34	23L39	23L38	21L
8	20M27	20M28	20M50	20M45	19M
9	20M31	20M26	20M46	20M44	19M
10	20M30	20M29	20M41	20M40	19M
11	20M33	20M34	20M39	20M38	19M
12	21M27	21M28	21M50	21M45	19M
13	21M31	21M36	21M46	21M44	19M
14	21M30	21M29	21M41	21M40	19M
15	21M04	21M05	21M03	21M22	19M
16	7P27	7P28	7P50	7P45	9P
17	7P31	7P26	7P46	7P44	9P
18	7P30	7P29	7P41	7P40	9P
19	7P33	7P34	7P39	7P38	9P
20	8P27	8P28	8P50	8P45	9P
21	8P31	8P26	8P46	8P44	9P
22	8P30	8P29	8P41	8P40	9P
23	8P33	8P34	8P39	8P38	9P
24	7Q27	7Q28	7Q50	7Q45	9Q
25	7Q31	7Q26	7Q46	7Q44	9Q
26	7Q30	7Q29	7Q41	7Q40	9Q
27	7Q33	7Q34	7Q39	7Q38	9Q
28	7Q02	7Q21	7Q18	7Q23	9Q
29	7Q04	7Q05	7Q03	7Q22	9Q
30	8Q02	8Q21	8Q18	8Q23	9Q
31	8Q04	8Q05	8Q03	8Q22	9Q

C REGISTER (FB)

	<u>C</u>
0	25L15
1	25L05
2	26L15
3	26L05
4	27L15
5	27L05
6	28L15
7	28L05
8	25M15
9	25M05
10	26M15
11	26M05
12	27M15
13	27M05
14	28M15
15	28M05
16	2P15
17	2P05
18	3P15
19	3P05
20	4P15
21	4P05
22	5P15
23	5P05
24	2Q15
25	2Q05
26	3Q15
27	3Q05
28	4Q15
29	4Q05
30	5Q15
31	5Q05

D REGISTER (FFS)

	<u>D</u>	<u>ND</u>	<u>Set/D</u>	<u>Reset/D</u>
0	25L23	\$	\$	25L07
1	25L28	\$	\$	25L07
2	26L23	\$	\$	26L07
3	26L28	\$	\$	26L07
4	27L23	\$	\$	27L07
5	27L28	\$	\$	27L07
6	28L23	\$	\$	28L07
7	28L28	\$	\$	28L07
8	25M23	\$	\$	25M07
9	25M28	\$	\$	25M07
10	26M23	\$	\$	26M07
11	26M28	\$	\$	26M07
12	27M23	\$	\$	27M07
13	27M28	\$	\$	27M07
14	28M23	\$	\$	28M07
15	28M28	\$	\$	28M07
16	2P23	\$	\$	2P07
17	2P28	\$	\$	2P07
18	3P23	\$	\$	3P07
19	3P28	\$	\$	3P07
20	4P23	\$	\$	4P07
21	4P28	\$	\$	4P07
22	5P23	\$	\$	5P07
23	5P28	\$	\$	5P07
24	2Q23	\$	\$	2Q07
25	2Q28	\$	\$	2Q07
26	3Q23	\$	\$	3Q07
27	3Q28	\$	\$	3Q07
28	4Q23	\$	\$	4Q07
29	4Q28	\$	\$	4Q07
30	5Q23	\$	\$	5Q07
31	5Q28	\$	\$	5Q07

DATA AND ADDRESS SWITCHES

	<u>KS</u>		<u>KSP</u>
0	17L01	15	17M44
1	17L02	16	2R01
2	17L03	17	2R02
3	17L04	18	2R07
4	17L07	19	2R08
5	17L08	20	2R44
6	17L09	21	2R43
7	17L42	22	2R40
8	17M01	23	2R09
9	17M02	24	4R01
10	17M03	25	4R02
11	17M04	26	4R07
12	17M07	27	4R08
13	17M08	28	4R44
14	17M09	29	4R09
15	17M42	30	4R40
16	18P01	31	4R43
17	18P02		
18	18P03		
19	18P04		
20	18P07		
21	18P08		
22	18P09		
23	18P42		
24	18Q01		
25	18Q02		
26	18Q03		
27	18Q04		
28	18Q07		
29	18Q08		
30	18Q09		
31	18Q42		

LR LINES (B)

LR28-0	26P14
LR29-0	16N24
LR30-0	15N24
LR31	26P30

MB LINES (BCR)

	<u>BCR/MB</u>
0	12M04
1	12M06
2	12M08
3	12M10
4	12M13
5	12M18
6	12M20
7	12M22
8	12M27
9	12M34
10	12M36
11	12M38
12	12M40
13	27M01
14	25P04
15	25P06
16	25P08
17	25P10
18	25P13
19	25P18
20	25P20
21	25P22
22	25P27
23	25P34
24	25P36
25	25P38
26	25P40
27	25P42
28	18R04
29	18R06
30	18R08
31	18R10

O REGISTER (FF)

	<u>O</u>	<u>NO</u>	<u>S/O</u>	<u>R/O</u>
1	22L04	22L05	22L03	22L22
2	22L02	22L21	22L18	22L23
3	22L06	22L07	\$	22L09
4	23L02	23L21	23L18	23L23
5	23L04	23L05	23L03	23L22
6	23L14	23L12	23L11	23L15
7	23L06	23L07	\$	23L09

P REGISTER (FF)

	<u>P</u>	<u>NP</u>	<u>Set/P</u>	<u>Reset/P</u>	<u>Extra Set Terms</u>
15	12R33	12R40	12R36	12R30	
16	12R25	12R26	12R31	12R24	
17	12R19	12R21	12R20	12R17	
18	12R05	12R22	12R12	12R03	
19	13R33	13R40	13R36	13R30	
20	13R25	13R26	13R31	13R24	
21	13R19	13R21	13R20	13R17	
22	13R05	13R22	13R12	13R03	
23	14R25	14R26	14R31	14R24	
24	14R19	14R21	14R20	14R17	
25	14R05	14R22	14R12	14R03	17S
26	16R33	16R40	16R36	16R30	
27	16R25	16R26	16R31	16R24	
28	16R19	16R21	16R20	16R17	
29	16R05	16R	16R12	16R03	17S
30	17R33	17R40	17R36	17R30	
31	17R25	17R26	17R31	17R24	
32	17R19	17R21	17R20	17R17	17S
33	17R05	17R22	17R12	17R03	17S

R REGISTER (FF)

	<u>R</u>	<u>NR</u>	<u>Set/R</u>	<u>Rèset/R</u>
28	23M33	23M40	23M36	
29	23M25	23M26	23M31	23M24
30	23M19	23M21	23M20	23M17
31	23M05	23M22	23M12	23M03

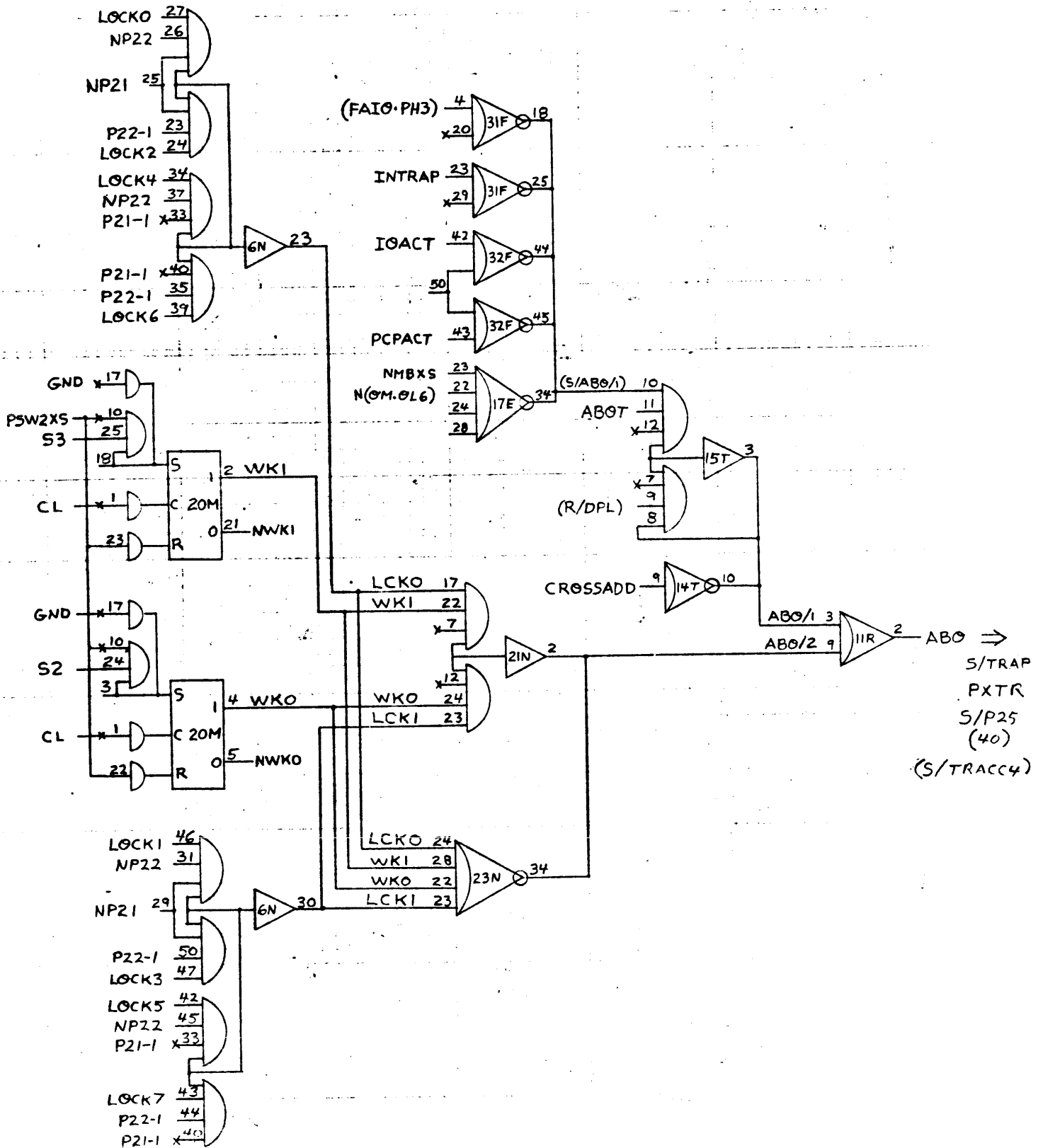
FAST MEMORY

	<u>RR</u>		<u>RW</u>
0	5K43	0	13L17
1	5K41	1	13L05
2	5K09	2	13L19
3	5K02	3	13L18
4	5K45	4	13L28
5	5K46	5	13L27
6	5K04	6	13L25
7	5K01	7	13L26
8	16K43	8	13L34
9	16K41	9	13L35
10	16K09	10	13L41
11	16K02	11	13L36
12	16K45	12	13L47
13	16K46	13	13L46
14	16K04	14	13L44
15	16K01	15	13L45
16	1S43	16	10S17
17	1S41	17	10S05
18	1S09	18	10S19
19	1S02	19	10S18
20	1S45	20	10S28
21	1S46	21	10S27
22	1S04	22	10S25
23	1S01	23	10S26
24	1T43	24	10S34
25	1T41	25	10S35
26	1T09	26	10S41
27	1T02	27	10S36
28	1T45	28	10S47
29	1T46	29	10S46
30	1T04	30	10S44
31	1T01	31	10S45

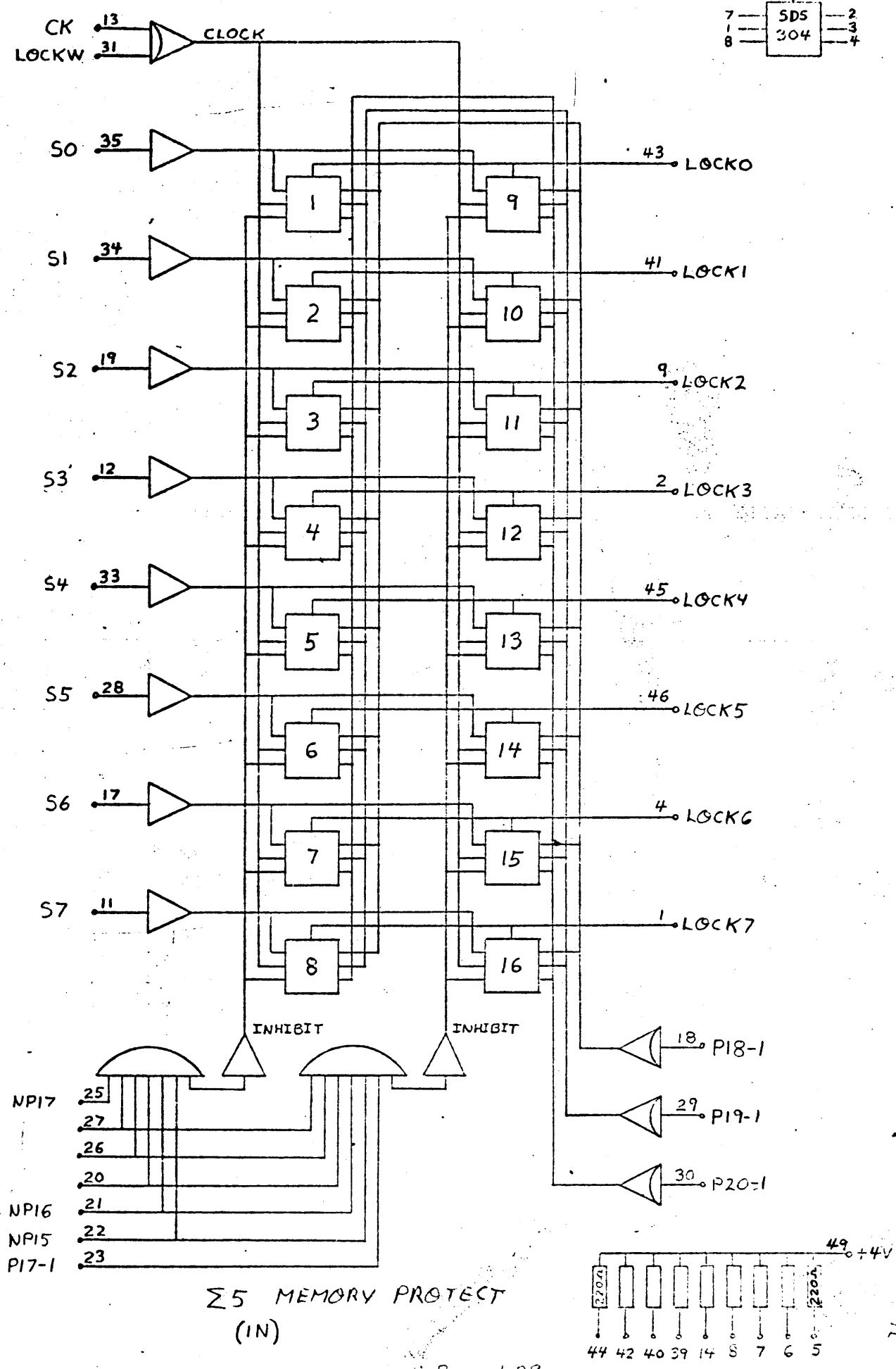
SUM BUSS

	<u>S</u>	<u>Extra Gates</u>
0	25L19	30L
1	25L17	
2	26L19	
3	26L17	
4	27L19	
5	27L17	
6	28L19	
7	28L17	
8	25M19	
9	25M17	
10	26M19	
11	26M17	
12	27M19	
13	27M17	
14	28M19	
15	28M17	
16	02P19	
17	2P17	
18	3P19	
19	3P17	
20	4P19	
21	5P17	
22	5P19	
23	5P17	1Q
24	02Q19	
25	2Q17	
26	3Q19	
27	3Q17	
28	4Q19	
29	4Q17	
30	5Q19	
31	5Q17	8N

MEMORY PROTET VIOLATION (TRAP TO 40)



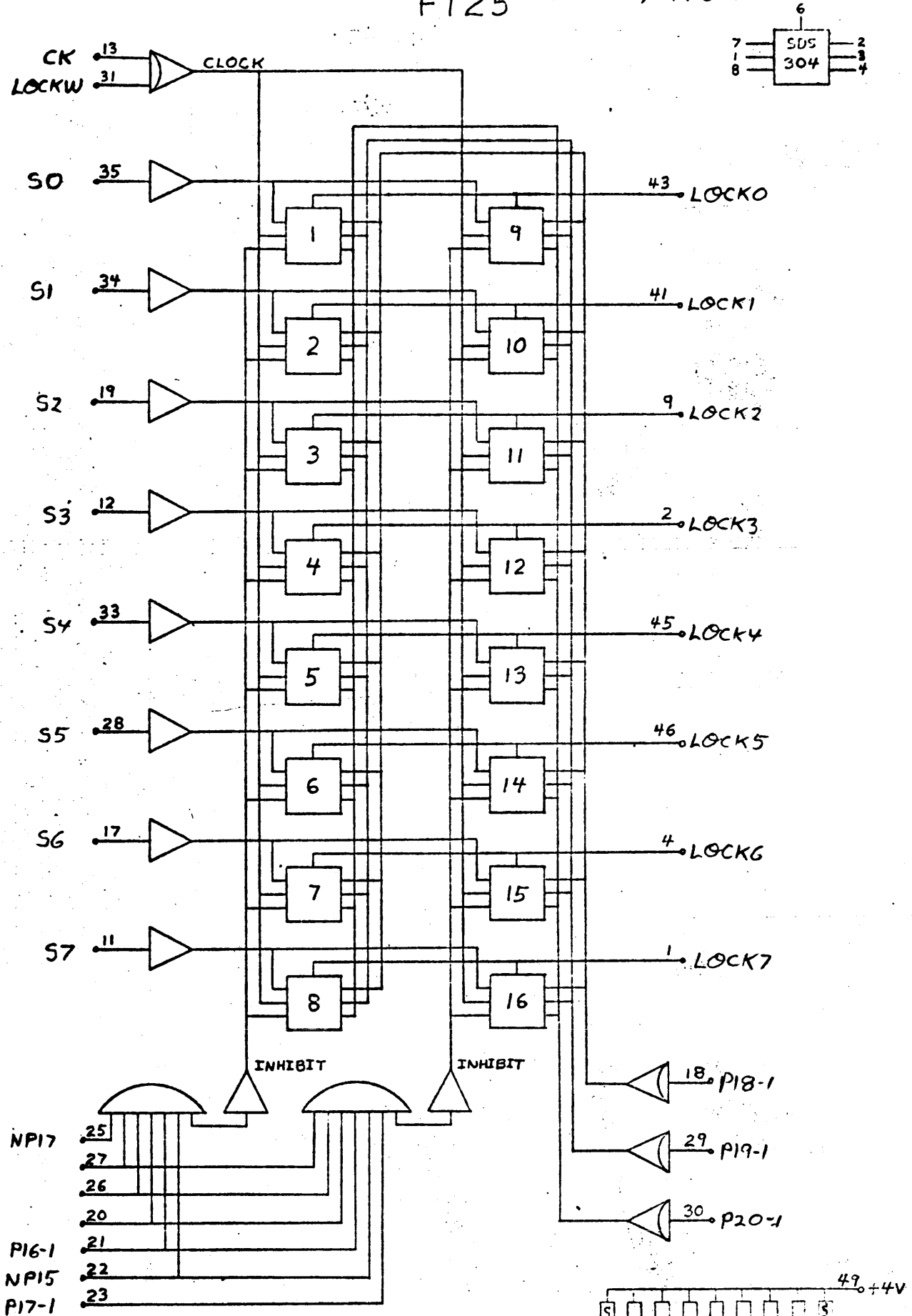
FT25 MEMORY PROTECT (IN)



Σ5 MEMORY PROTECT
(IN)

76
20
20

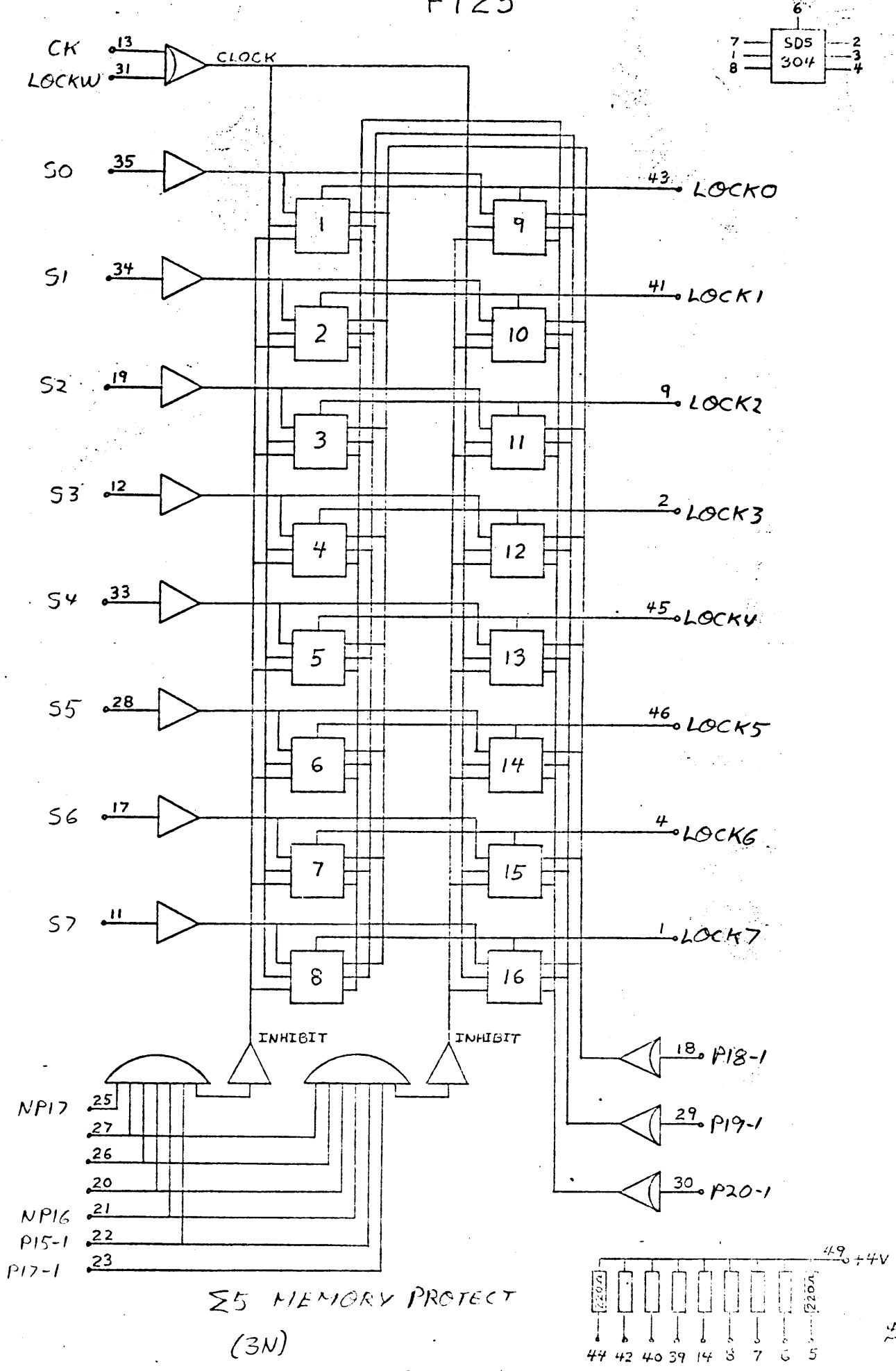
FT25 MEMORY PROTECT (2N)



Σ5 MEMORY PROTECT (2N)

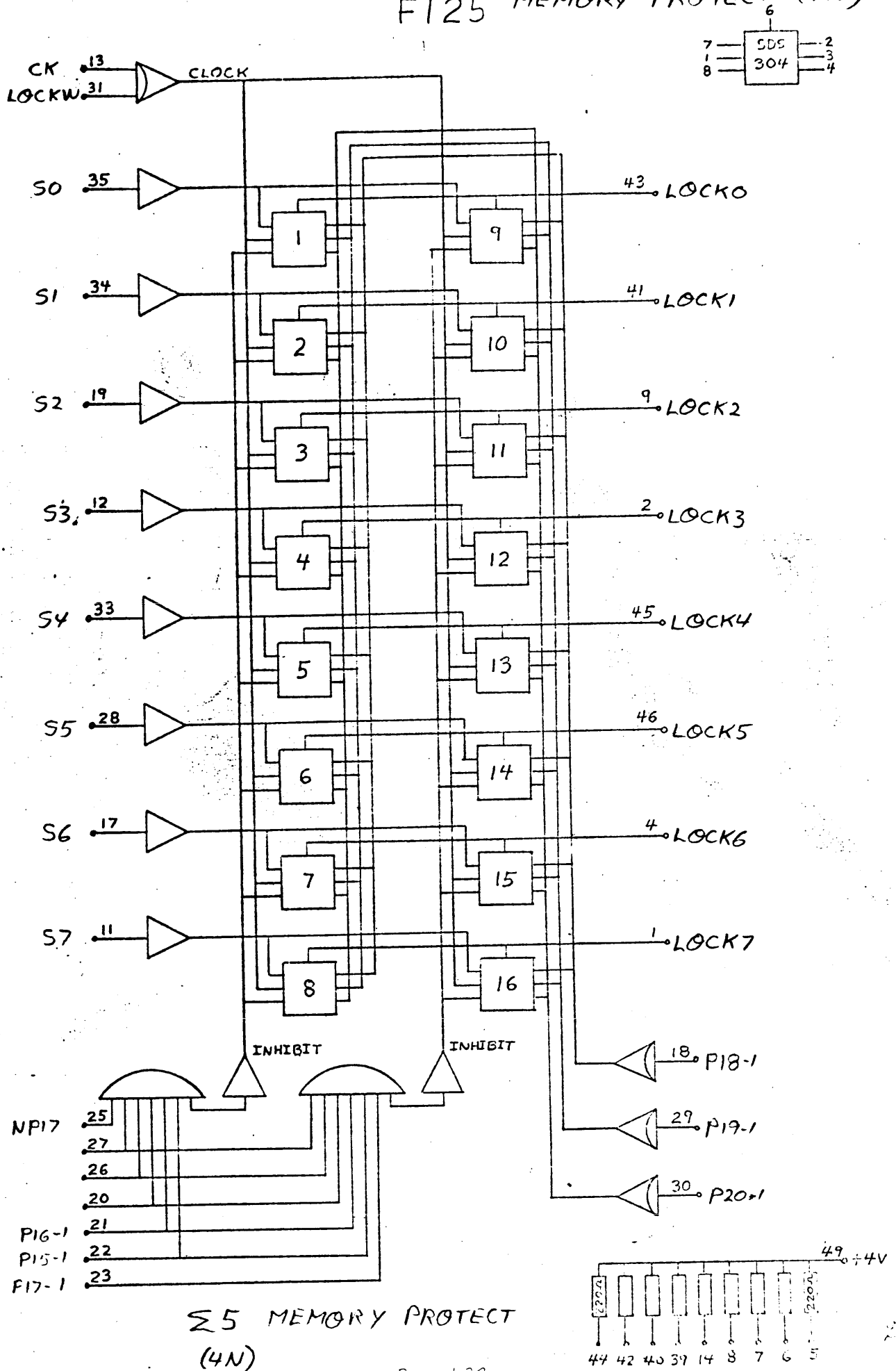
20 21 22

FT25 MEMORY PROTECT (3N)



2500

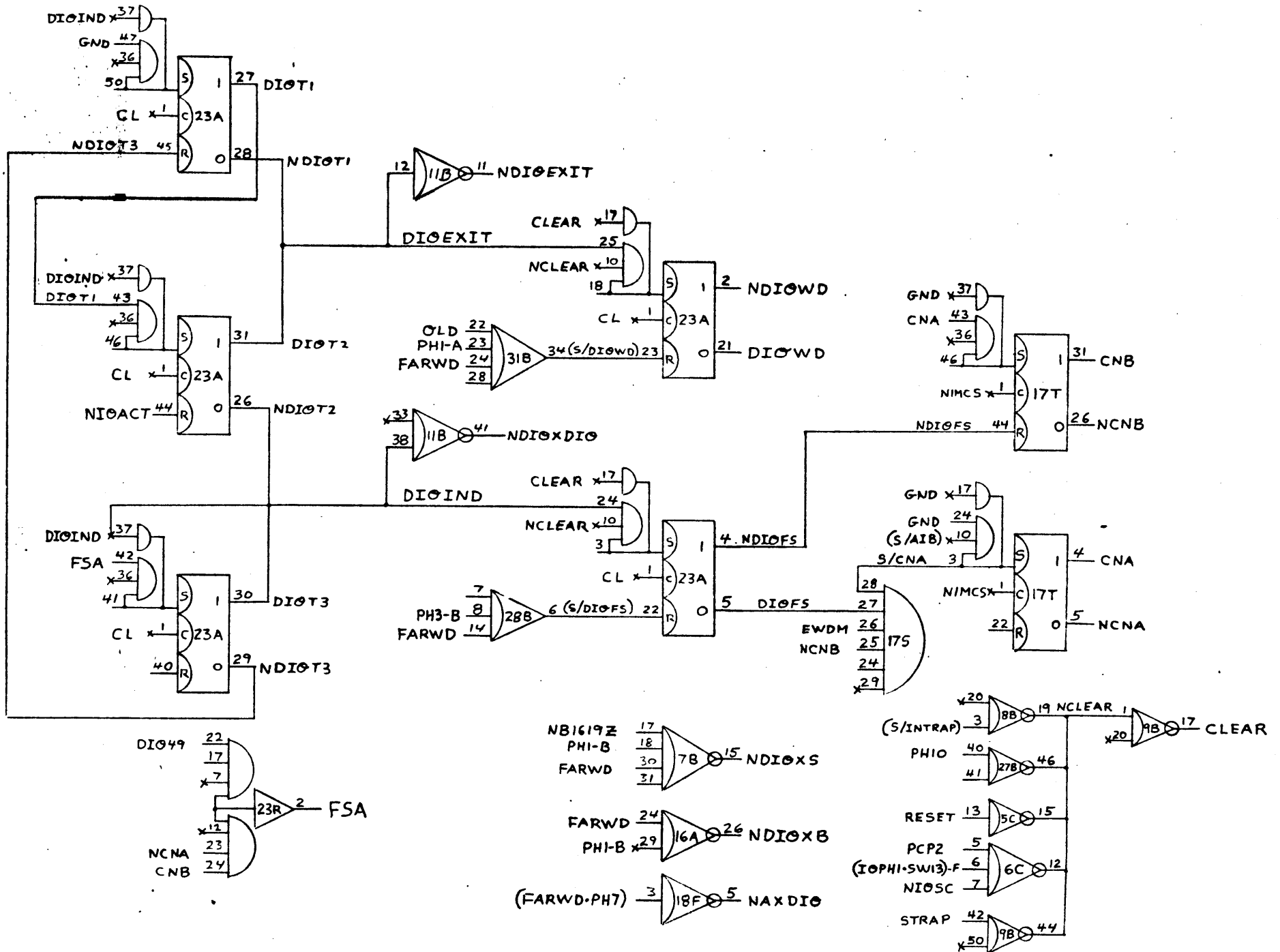
FT25 MEMORY PROTECT (4N)



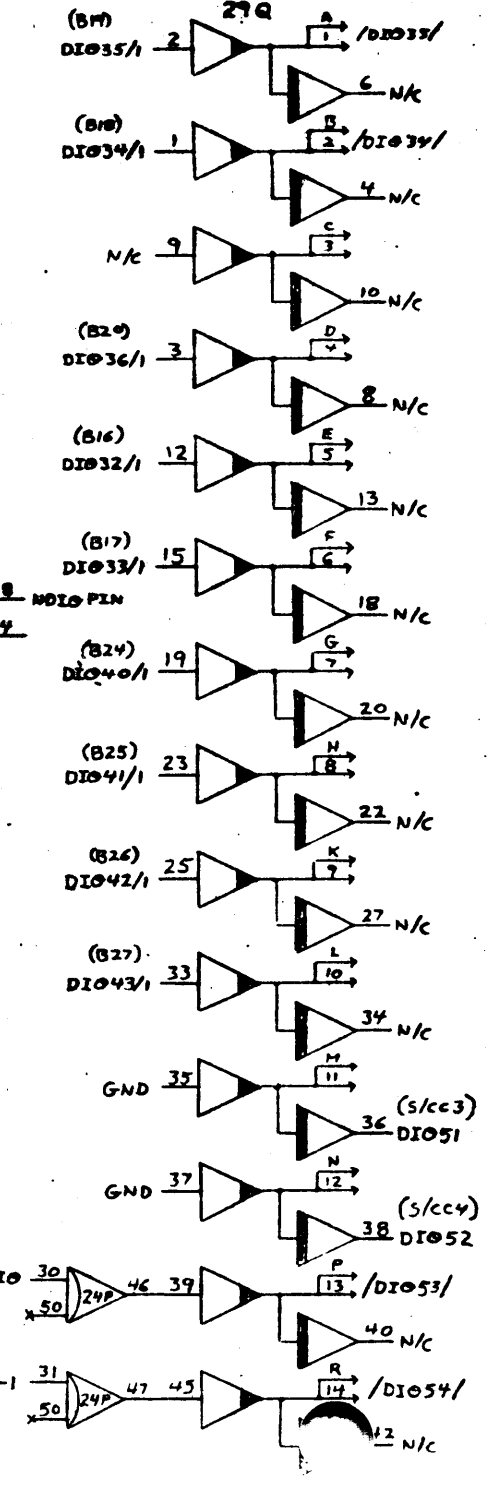
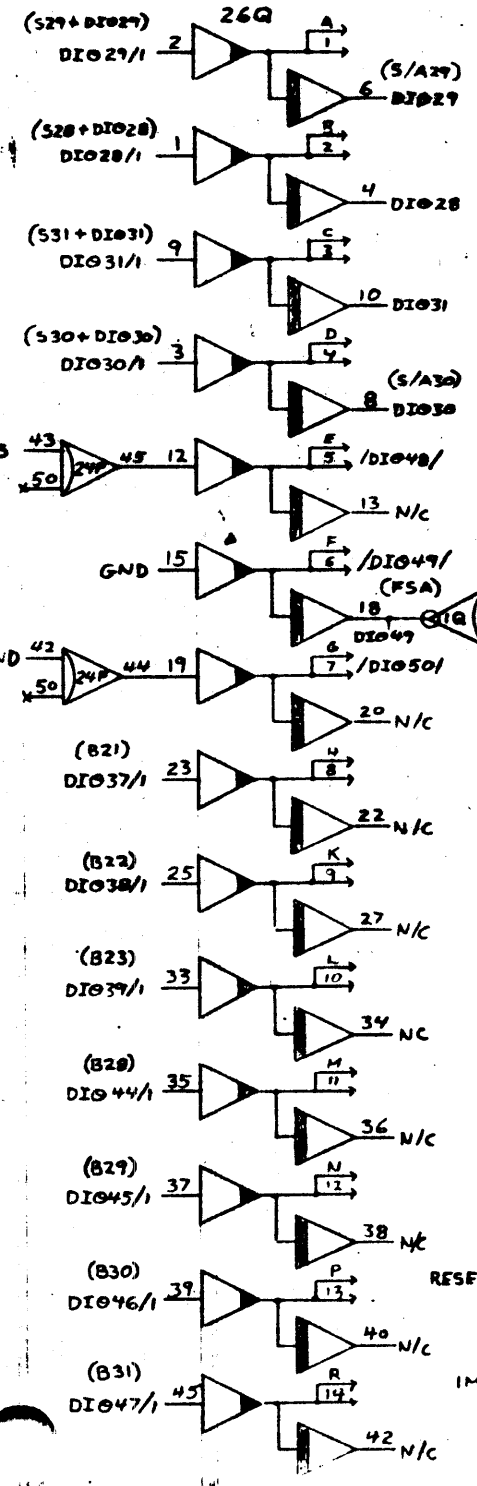
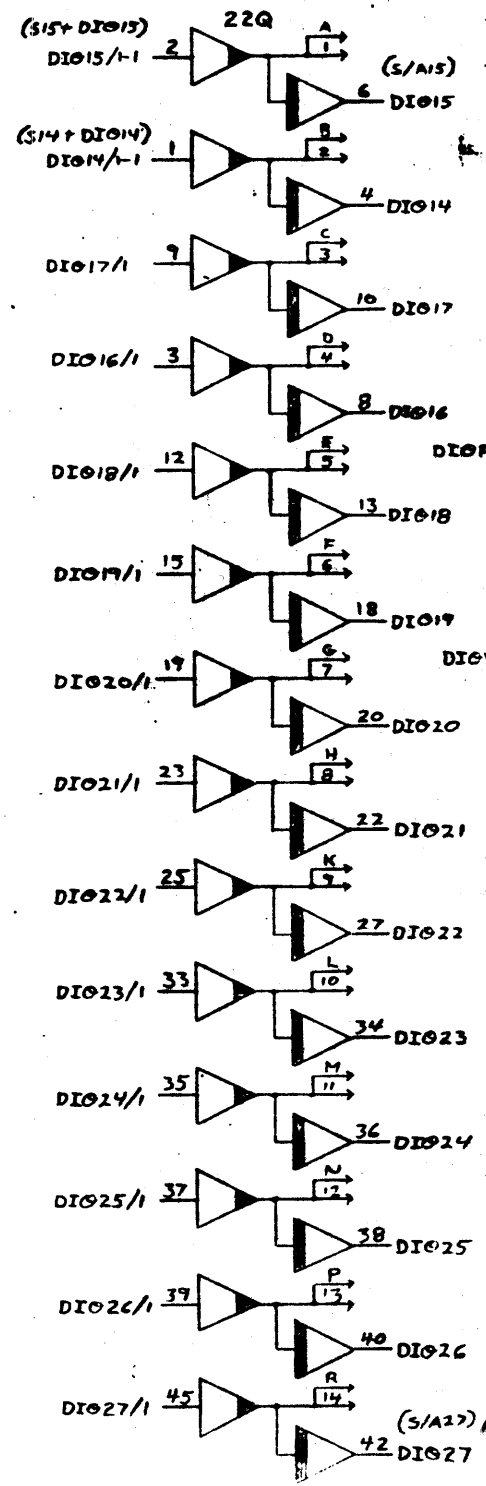
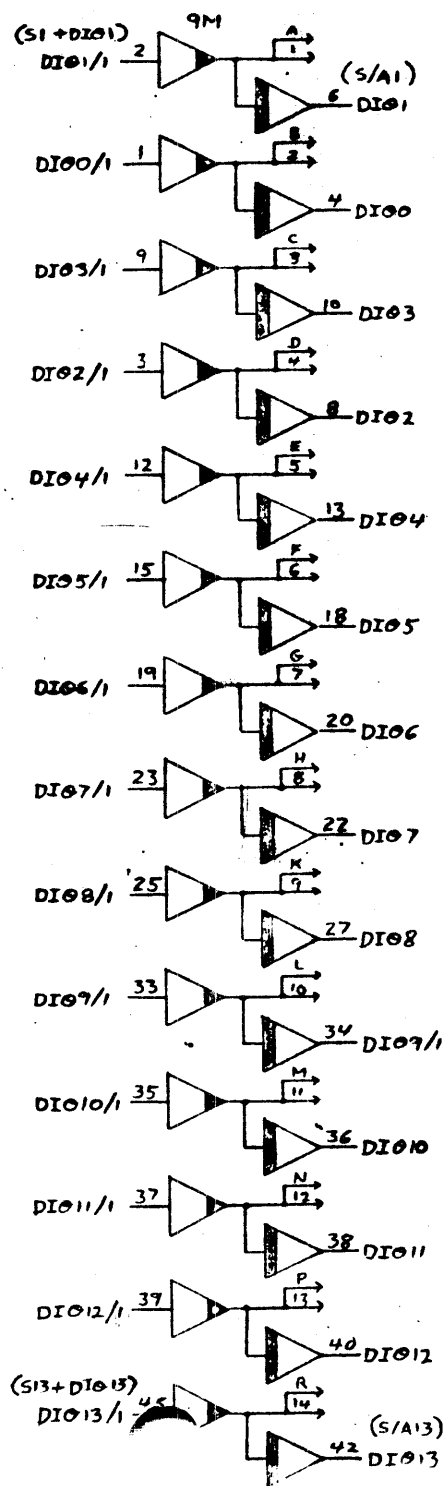
Σ5 MEMORY PROTECT (4N)

Σ5 DIO LOGIC

4/69
G. Malone



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Σ5 FLOAT OPTION 8218

COCHRANE

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	XT 10	IT 17	BT 16		IT 25	BT 11	Y	IT 25		IT 25	Y	IT 16	XT 10	BT 10	BT 10	LT 20	LT 20	BT 18	BT 11	IT 16	Y	IT 26	GT 11	FT 22	XT 10		ST 14						A
B	ZT 26 32 L	FT 22	IT 16	IT 16	BT 16	BT 16	Y			IT 16	Y		IT 16	XT 10	FT 26	FT 26	FT 26	FT 26	XT 10	IT 16	Y	LT 42	LT 42	LT 42	LT 18	LT 42	LT 42	LT 42	LT 42	LT 18	LT 42	LT 42	B
C	XT 10	FT 41	FT 22	FT 41	GT 12	FT 41	FT 22	FT 41		GT 12	BT 10	FT 22	FT 41	GT 12	FT 41	FT 41	FT 22	IT 16	GT 12	GT 11	FT 18	FT 22	FT 18	GT 12	FT 18	FT 18	FT 22	XT 10	GT 12	FT 22	GT 12	FT 22	C
D	ZT 23 30 T	LT 42	LT 42	LT 18		LT 42	LT 42	LT 42	LT 42	LT 18	LT 42	LT 42	XT 10	LT 18	LT 42	LT 42	LT 18	LT 42	LT 42	LT 42	XT 10	LT 42	LT 18	LT 42	LT 42	LT 42	LT 42	LT 18	XT 10	LT 18	LT 42	LT 42	D
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

CLOCK WIRES

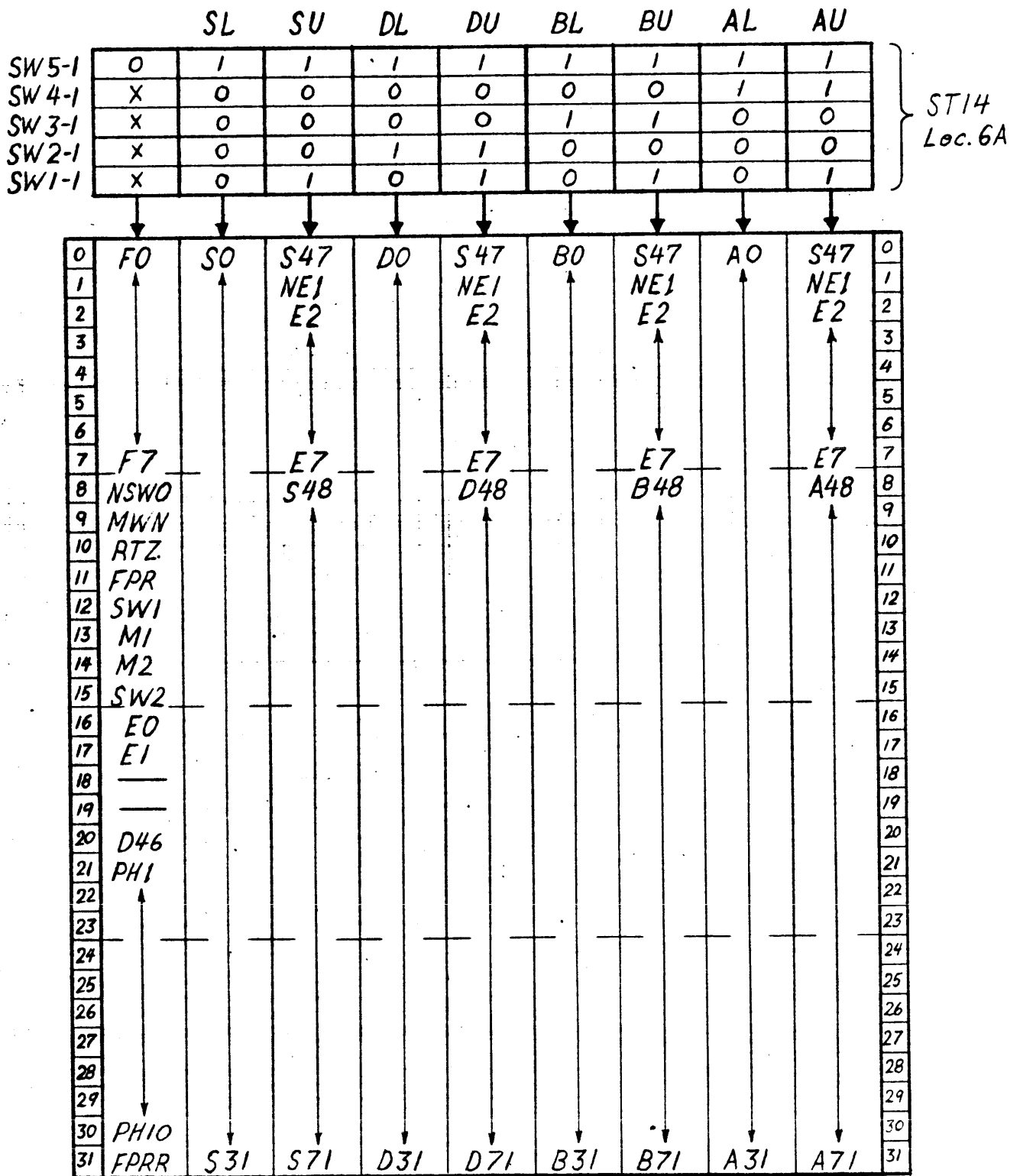
32D04 -TO- 09A01
 06 — 05B09
 08 — 31B01
 10 — 03C01
 17 — 06C01
 19 — 08C01
 21 — 11C01
 24 — 17C01
 33 — 25C01
 36 — 27C01
 43 — 18D09
 32D47 -TO- 31D09

PHASE TEST POINTS

PH1-03C06
 PH2-21C06
 PH3-26C06
 PH4-31B27
 PH5-09A21
 PH6-09A05
 PH7-09A12
 PH8-09A07
 PH9-30C06
 PH10-31B06

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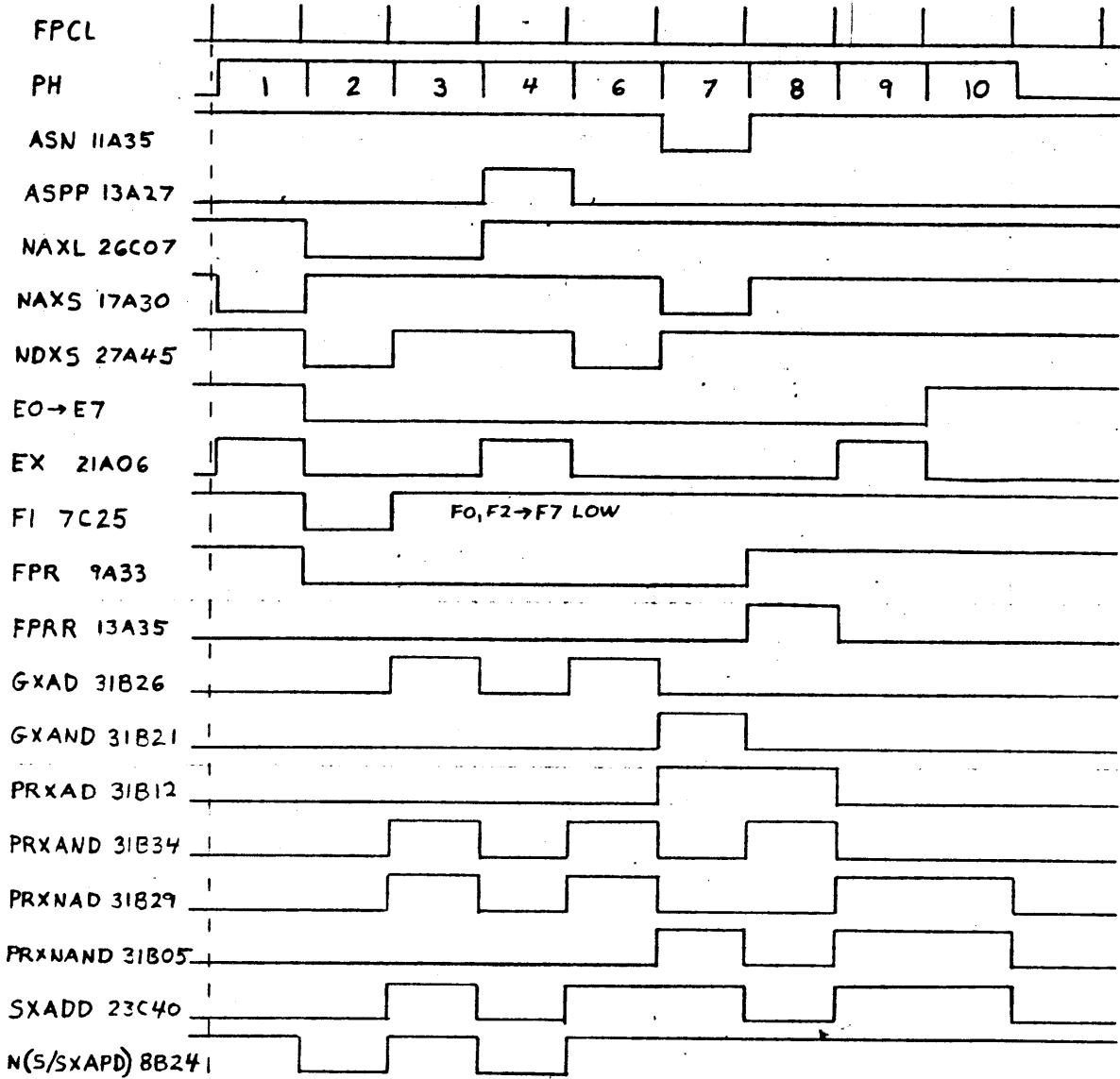
§5 FLOAT SWITCH DISPLAY.



Note: To display FLOAT registers on PCP panel with ST14 switch module, the Register Selection Switch must be on EXT.

Σ5 FLOAT BOY

EXU.LOC. 140
 DIAG. 32C (ID FAL) NEW 5/7 DIAG. 408 (ID FAL)
 EXU.LOC. 14



SINGLE CLOCK RESULTS TO CPU

	SU	SL	40 AU 71	AD AL 451	DU	DL
PH4 31B27	40000000	00000000	COAAAAAAAA	AAAAAAAAAA	COAAAAAAAA	BF800000
PH6 9A05	C0555555	55555554	"	"	"	AAAAAAAA
PH7 9A12	40AAAAAAAA	AAAAAAAAAC	40000000	00000000	C0555555	55555554
PH8 9A07	"	"	40AAAAAAAA	AAAAAAAAAC	"	"
PH9 30C06	C0555555	55555554	"	"	"	"
PH10 31B06	BF555555	"	3FAAAAAA	"	BF555555	"

Float Add Long Example

SIGMA 5 FLOAT PHASES

<u>FF</u>		<u>NFF</u>		<u>S/FF</u>	<u>R/FF</u>	<u>C/</u>
PH1	3C06	NPH1	3C07	\$	09	01
PH2	21C06	NPH2	21C07	\$	09	01
PH3	21C06	NPH3	26C07	\$	09	01
PH4	31B27	NPH4	31B28	50	45	01
NPH5	9A02	PH5	0A21	18	23	01
NPH6	9A04	PH6	9A05	03	22	01
NPH7	9A14	PH7	9A12	11	15	01
NPH8	9A06	PH8	9A07	\$	09	01
PH9	30C06	NPH9	30C07	\$	09	01
PH10	31B06	NPH10	31B07	\$	09	01

A-REGISTER (FLOAT)

	<u>FF</u>	<u>NFF</u>	<u>S/</u>	<u>R/</u>	<u>C/</u>
A0	11C31	26	46	44	01
1	11C30	29	41	40	01
2	11C33	34	39	38	01
3	11C27	28	50	45	01
4	16C30	29	41	40	01
5	16C31	26	46	44	01
6	16C27	28	50	45	01
7	16C33	34	39	38	01
8	16C02	21	18	23	01
9	16C04	05	03	22	01
10	16C14	12	11	15	01
11	21C33	34	39	38	01
12	21C30	29	41	40	01
13	21C31	26	46	44	01
14	21C27	28	30	45	01
15	21C04	05	03	22	01
16	21C02	21	18	23	01
17	21C14	12	11	15	01
18	26C14	12	11	15	01
19	26C33	34	39	38	01
20	26C30	29	41	40	01
21	26C31	26	46	44	01
22	26C27	28	50	45	01
23	26C04	05	03	22	01
24	26C02	21	18	23	01
25	30C14	12	11	15	01
26	30C04	05	03	22	01
27	30C02	21	18	23	01
28	30C30	29	41	40	01
29	30C31	26	46	44	01
30	30C27	28	50	45	01
A31	30C33	34	39	38	01
A47	1C06	07	5	09	01
48	1C02	21	18	23	01
49	1C04	05	03	22	01
50	1C14	12	11	15	01
51	1C33	34	39	38	01
52	1C30	29	41	40	01
53	1C31	26	46	44	01
54	1C27	28	50	45	01
55	3C04	05	03	22	01
56	3C33	34	39	38	01
57	3C02	21	18	23	01
58	3C14	12	11	15	01
59	3C30	29	41	40	01
60	3C31	26	46	44	01
61	3C27	28	50	45	01
62	6C27	28	50	45	01
63	6C04	05	03	22	01
64	6C33	34	39	38	01
65	6C02	21	18	23	01
66	6C14	12	11	15	01
67	6C30	29	41	40	01
68	6C31	26	46	44	01
69	11C04	05	03	22	01
70	11C02	21	18	23	01
A71	11C14	12	11	15	01

ADDER PR (FLOAT)

PRO	8D01
1	8D02
2	9D01
3	9D02
4	11D01
5	11D02
6	13D01
7	13D02
8	14D01
9	14D02
10	15D01
11	15D02
12	17D01
13	17D02
14	18D01
15	18D02
16	21D01
17	21D02
18	22D01
19	22D02
20	24D01
21	24D02
22	25D01
23	25D02
24	26D01
25	26D02
26	27D01
27	27D02
28	30D01
29	30D02
30	31D01
PR31	31D02
PR46	11B01
47	11B02
48	10B01
49	10B02
50	9B01
51	9B02
52	7B01
53	7B02
54	6B01
55	6B02
56	5B01
57	5B02
58	4B01
59	4B02
60	2B01
61	2B02
62	1B01
63	1B02
64	1D01
65	1D02
66	2D01
67	2D02
68	6D01
69	6D02
70	7D01
71	7D02

ADDER G (FLOAT)

G0	8D04
1	8D06
2	9D04
3	9D06
4	11D04
5	11D06
6	13D04
7	13D06
8	14D04
9	14D06
10	15D04
11	15D06
12	17D04
13	17D06
14	18D04
15	18D06
16	21D04
17	21D06
18	22D04
19	22D06
20	24D04
21	24D06
22	25D09
23	25D06
24	26D04
25	26D06
26	27D04
27	27D06
28	30D04
29	30D06
30	31D04
G31	31D06
G46	11B04
G47	11B06
48	10B04
49	10B06
50	9B04
51	9B06
52	7B04
53	7B06
54	6B04
55	6B06
56	5B04
57	5B06
58	4B04
59	4B06
60	2B04
61	2B06
62	1B04
63	1B06
64	1D04
65	1D06
66	2D04
67	2D06
68	6D04
69	6D06
70	7D04
71	7D06

ADDER K (FLOAT)

K0	10D26
1	10D27
2	10D25
3	9D26
4	10D19
5	10D18
6	10D20
7	19D27
8	16D26
9	16D27
10	16D25
11	19D25
12	16D19
13	16D18
14	16D20
15	19D17
16	23D26
17	23D27
18	23D25
19	19D19
20	23D19
21	23D18
22	23D20
23	19D18
24	29D26
25	29D27
26	29D25
27	19D20
28	29D19
29	29D18
30	29D20
K31	27B27
K46	5D28
47	5D26
48	8B26
49	8B27
50	8B25
51	5D27
52	8B19
53	8B18
54	8B20
55	5D25
56	3B26
57	3B27
58	3B25
59	5D19
60	3B19
61	3B18
62	3B20
63	5D18
64	3D26
65	3D27
66	3D25
67	5D20
68	3D19
69	3D18
70	3D20
71	10D22

B-REGISTER (F.GAT)

	<u>FF</u>		<u>NFF</u>	<u>S/</u>	<u>R/</u>	<u>C/</u>
	BO	17C41	43	\$	42	01
	1	17C37	39	\$	42	01
	2	17C33	35	\$	42	01
	3	17C29	31	\$	42	01
	4	17C03	05	\$	09	01
	5	17C07	15	\$	09	01
	6	17C17	19	\$	09	01
	7	17C21	27	\$	09	01
	8	16C06	07	\$	09	01
	9	31C03	05	\$	09	01
	10	31C07	15	\$	09	01
	11	31C17	19	\$	09	01
	12	31C21	27	\$	09	01
	13	29C03	05	\$	09	01
	14	29C07	15	\$	09	01
	15	29C17	19	\$	09	01
	16	29C21	27	\$	09	01
	17	27C03	05	\$	09	01
	18	27C07	15	\$	09	01
	19	27C17	19	\$	09	01
	20	27C21	27	\$	09	01
	21	25C03	05	\$	09	01
	22	25C07	15	\$	09	01
	23	25C17	19	\$	09	01
	24	25C21	27	\$	09	01
	25	20C03	05	\$	09	01
	26	20C07	15	\$	09	01
	27	20C17	19	\$	09	01
	28	20C21	27	\$	09	01
	29	18C03	05	\$	09	01
	30	18C07	15	\$	09	01
	31	18C17	19	\$	09	01
	B48	31C41	43	\$	42	01
	49	31C37	39	\$	42	01
	50	31C33	35	\$	42	01
	51	31C29	31	\$	42	01
	52	29C41	43	\$	42	01
	53	29C37	39	\$	42	01
	54	29C35	35	\$	42	01
	55	29C29	31	\$	42	01
	56	27C41	43	\$	42	01
	57	27C37	39	\$	42	01
	58	23C33	35	\$	42	01
	59	27C29	31	\$	42	01
	60	25C41	43	\$	42	01
	61	25C37	39	\$	42	01
	62	25C33	35	\$	42	01
	63	25C29	31	\$	42	01
	64	20C41	43	\$	42	01
	65	20C37	39	\$	42	01
	66	20C33	35	\$	42	01
	67	20C29	31	\$	42	01
	68	18C41	43	\$	42	01
	69	18C37	39	\$	42	01
	70	18C33	35	\$	42	01
	71	18C29	31	\$	42	01

C GATES (FLOAT)

CO	8D05
1	8D15
2	9D05
3	9D15
4	11D05
5	11D15
6	13D05
7	13D15
8	14D05
9	14D15
10	15D05
11	15D15
12	17D05
13	17D15
14	18D05
15	18D15
16	a1D05
17	21D15
18	22D05
19	22D15
20	24D05
21	24D15
22	25D05
23	25D15
24	26D05
25	26D15
26	27D05
27	27D15
28	30D05
29	30D15
30	31D05
31	31D15
C46	11B05
47	11B15
48	10B05
49	10B15
50	9B05
51	9B15
52	7B05
53	7B15
54	6B05
55	6B15
56	5B05
57	5B15
58	4B05
59	4B15
60	2B05
61	2B15
62	1B05
63	1B15
64	1D05
65	1D15
66	2D05
67	2D15
68	6D05
69	6D15
70	7D05
71	7D15

D-REGISTER (FLOAT)

<u>FF</u>		<u>NFF</u>	<u>S/</u>	<u>R/</u>	<u>C/</u>
D0	8D28	\$	\$	07	09
1	8D23	\$	\$	07	09
2	9D28	\$	\$	07	09
3	9D23	\$	\$	07	09
4	11D28	\$	\$	07	09
5	11D23	\$	\$	07	09
6	13D28	\$	\$	07	09
7	13D23	\$	\$	07	09
8	14D28	\$	\$	07	09
9	14D23	\$	\$	07	09
10	15D28	\$	\$	07	09
11	15D23	\$	\$	07	09
12	17D28	\$	\$	07	09
13	17D23	\$	\$	07	09
14	18D28	\$	\$	07	09
15	18D23	\$	\$	07	09
16	21D28	\$	\$	07	09
17	21D23	\$	\$	07	09
18	22D28	\$	\$	07	09
19	22D23	\$	\$	07	09
20	24D28	\$	\$	07	09
21	24D23	\$	\$	07	09
22	25D28	\$	\$	07	09
23	25D23	\$	\$	07	09
24	26D28	\$	\$	07	09
25	26D23	\$	\$	07	09
26	27D28	\$	\$	07	09
27	27D23	\$	\$	07	09
28	30D28	\$	\$	07	09
29	30D23	\$	\$	07	09
30	31D28	\$	\$	07	09
31	31D23	\$	\$	07	09
D46	11B28	\$	\$	07	09
D47	11B23	\$	\$	07	09
48	10B28	\$	\$	07	09
49	10B25	\$	\$	07	09
50	9B28	\$	\$	07	09
51	9B23	\$	\$	07	09
52	7B28	\$	\$	07	09
53	7B35	\$	\$	07	09
54	6B28	\$	\$	07	09
55	6B23	\$	\$	07	09
56	5B28	\$	\$	07	09
57	7b23	\$	\$	07	09
58	4B28	\$	\$	07	09
59	4B23	\$	\$	07	09
60	2B28	\$	\$	07	09
61	2B23	\$	\$	07	09
62	1B28	\$	\$	07	09
63	1B23	\$	\$	07	09
64	1D28	\$	\$	07	09
65	1D23	\$	\$	07	09
66	2D28	\$	\$	07	09
67	2D23	\$	\$	07	09
68	6D28	\$	\$	07	09
69	6D23	\$	\$	07	09
70	7D28	\$	\$	07	09
71	7D23	\$	\$	07	09

E-REGISTER (FLOAT)

	<u>FF</u>		<u>NFF</u>	<u>S/</u>	<u>R/</u>	<u>C/</u>
E0		8C33	40	36	30	01
E1		8C25	26	31	24	01
E2		8C19	21	20	17	01
E3		8C05	22	12	03	01
E4		10C33	40	36	30	01
E5		10C25	26	31	24	01
E6		10C19	21	20	17	01
E7		10C05	22	12	03	01

F-REGISTER (FLOAT)

<u>FF</u>		<u>NFF</u>	<u>S/</u>	<u>R/</u>	<u>C/</u>
F0	TC33	40	36	30	01
F1	TC25	26	31	24	01
F2	7C19	21	20	17	01
F3	7C05	22	12	03	01
F4	12C33	40	36	30	01
F5	12C25	26	31	24	01
F6	12C19	21	20	17	01
F7	12C05	22	12	03	01

FP GATES (FLOAT)

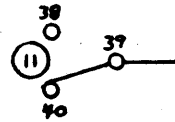
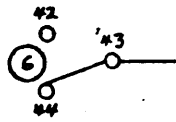
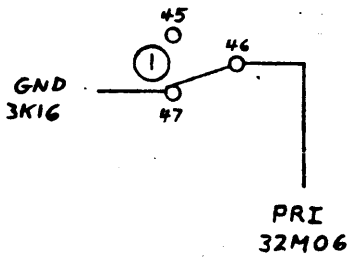
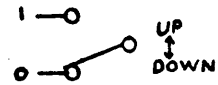
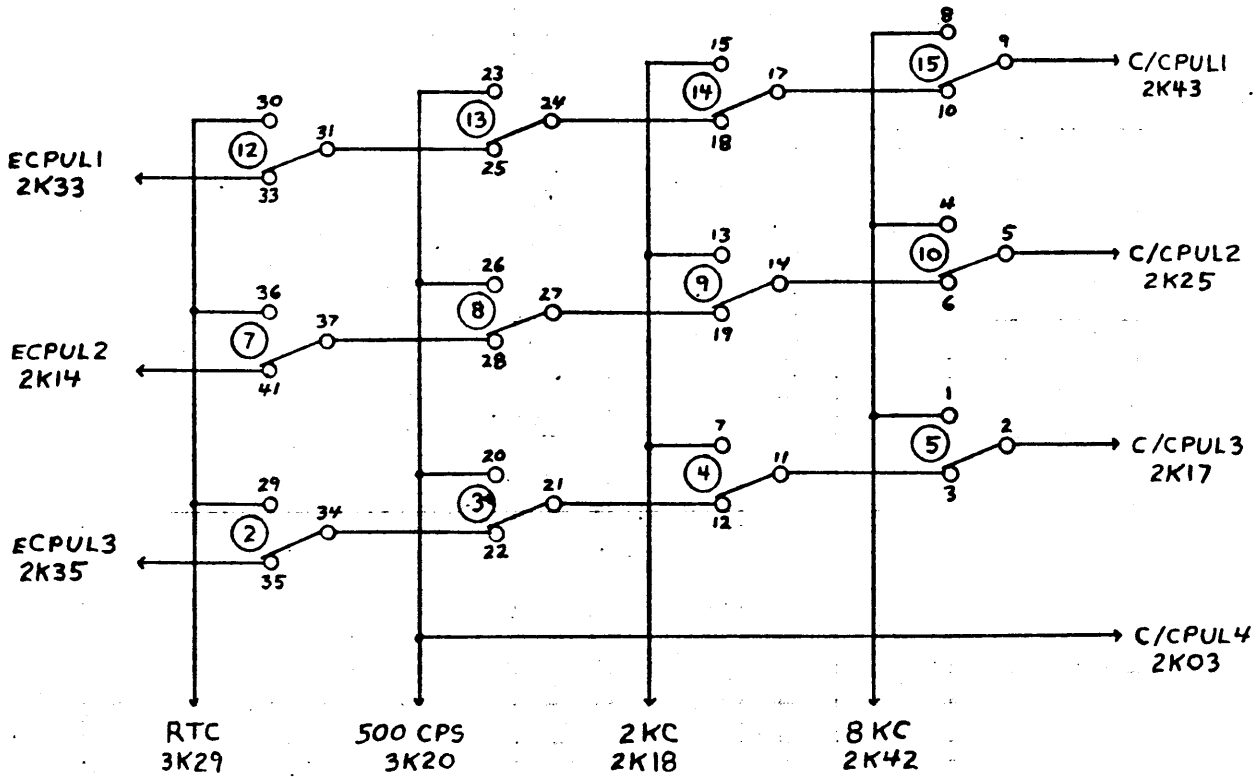
FPO	15B37
1	15B33
2	15B34
3	15B35
4	15B18
5	15B13
6	15B14
7	15B15
8	16B37
9	16B33
10	16B34
11	16B35
12	16B18
13	16B13
14	16B14
15	16B15
16	17B37
17	17B33
18	17B34
19	17B35
20	17B18
21	17B13
22	17B14
23	17B15
24	18B37
25	18B33
26	18B34
27	18B35
28	18B18
29	18B13
30	18B14
FP31	18B15

S, BUS (FLOAT)

S0	8D17
1	8D19
2	9D17
3	9D19
4	11D17
5	11D19
6	13D17
7	13D19
8	14D17
9	14D19
10	15D17
11	15D19
12	17D17
13	17D19
14	18D17
15	18D19
16	21D17
17	21D19
18	22D17
19	22D19
20	24D17
21	24D19
22	25D17
23	25D19
24	26D17
25	26D19
26	27D17
27	27D19
28	30D17
29	30D19
30	31D17
S31	31D19
S46	11B17
47	11B19
48	10B17
49	10B19
50	9B17
51	9B19
52	7B17
53	7B19
54	6B17
55	6B19
56	5B17
57	5B19
58	4B17
59	4B19
60	2B17
61	2B19
62	1B17
63	1B19
64	1D17
65	1D19
66	2D17
67	2D19
68	6D17
69	6D19
70	7D17
S71	7D19

Σ5

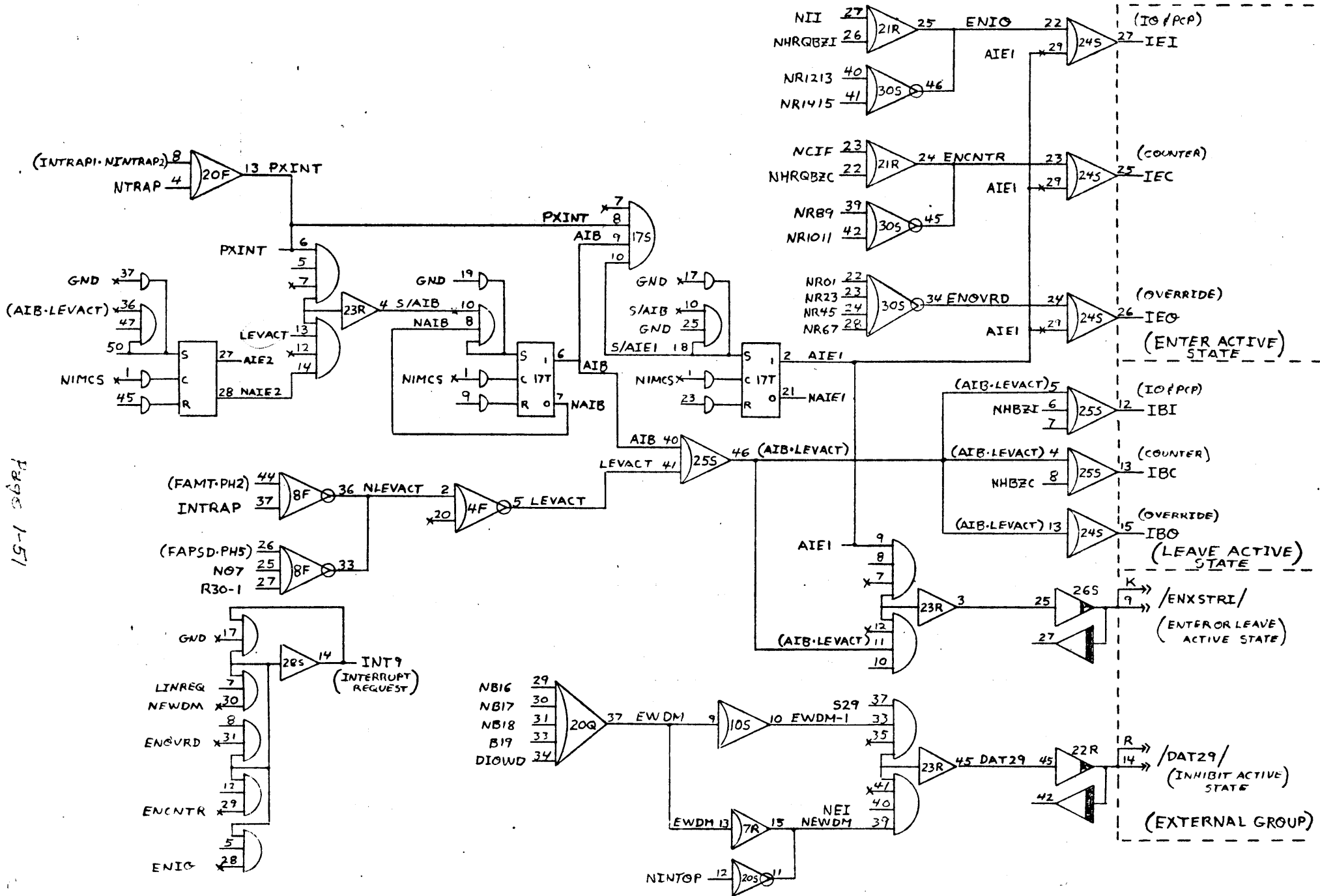
SW. REAL TIME CLOCK MODULE ST14 (3K)



Σ5 CPU INTERRUPT SERVICE LOGIC

TO 5 LEVEL

Brune



Figs 1-51

CPU INTERRUPT SERVICE LOGIC

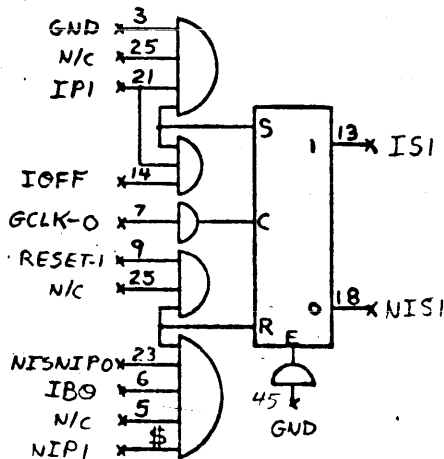
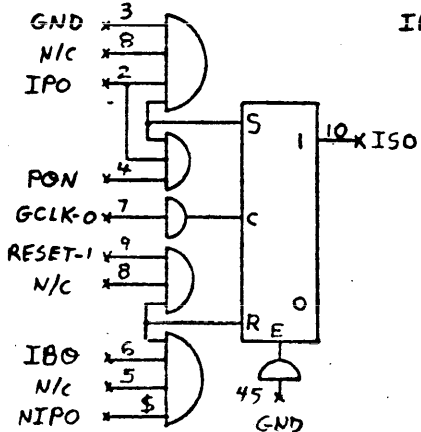
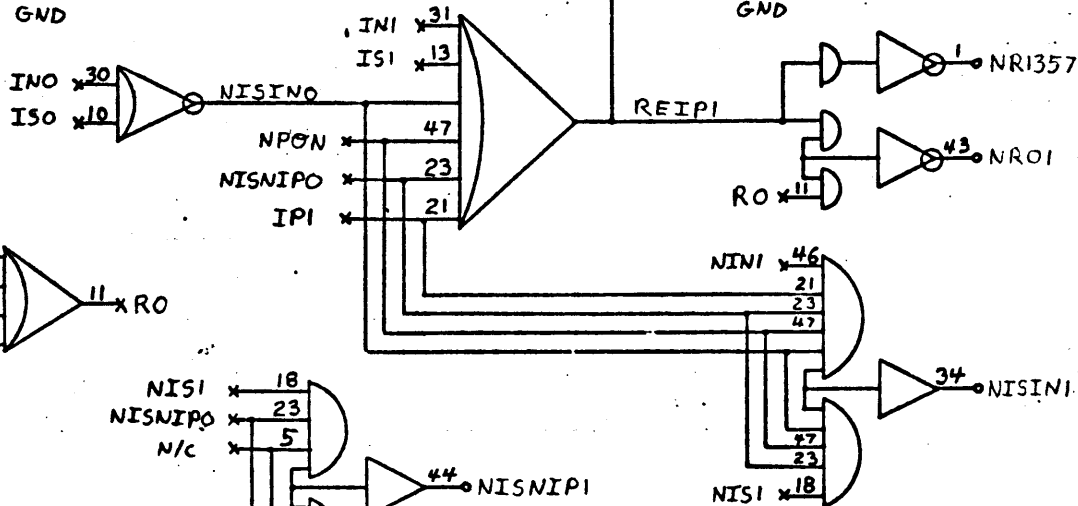
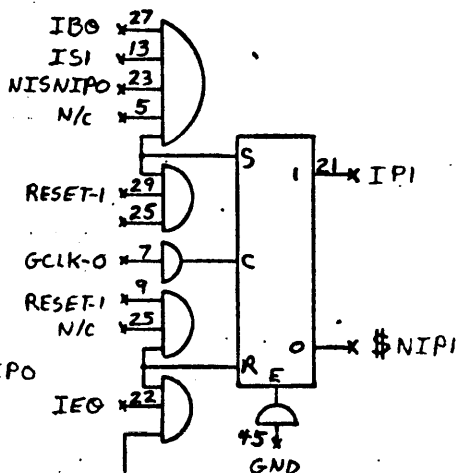
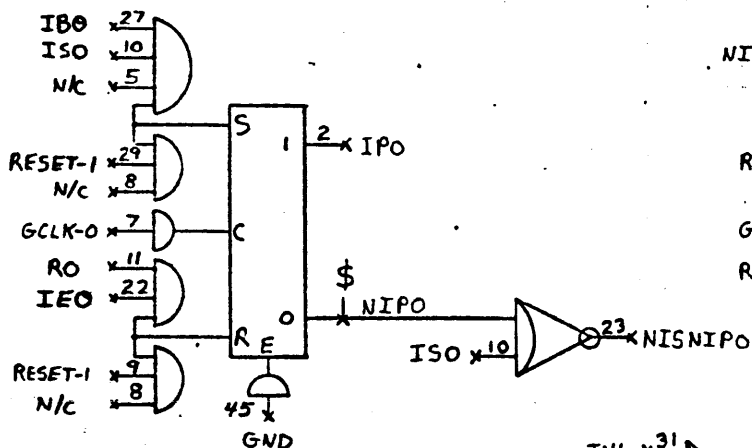
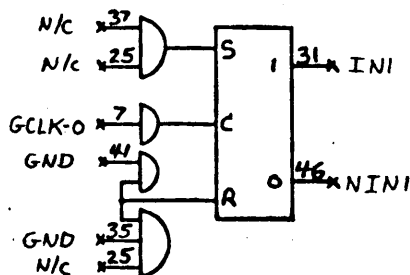
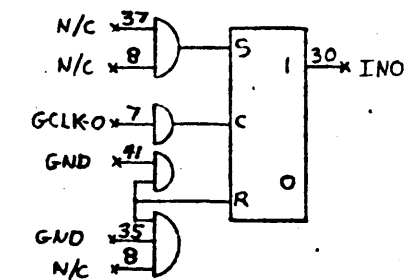
LT16 INTERRUPT

Σ5 (25R)

OVERIDE GROUP

POWER FAIL SAFE

W. J. ...
12/30/70



POWER ON
[50]

Σ5 (25R)

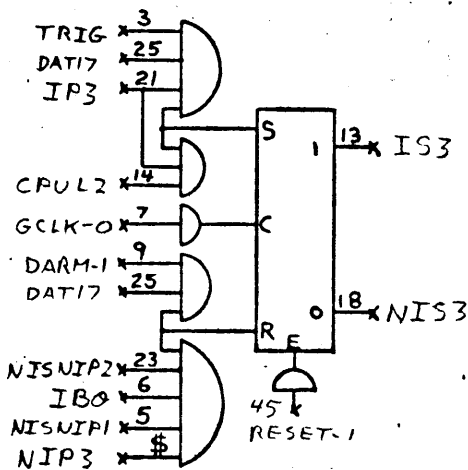
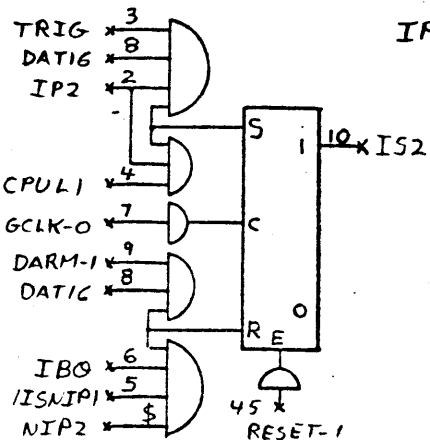
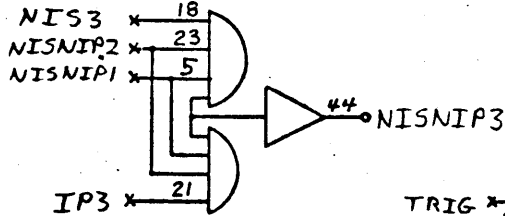
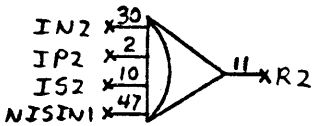
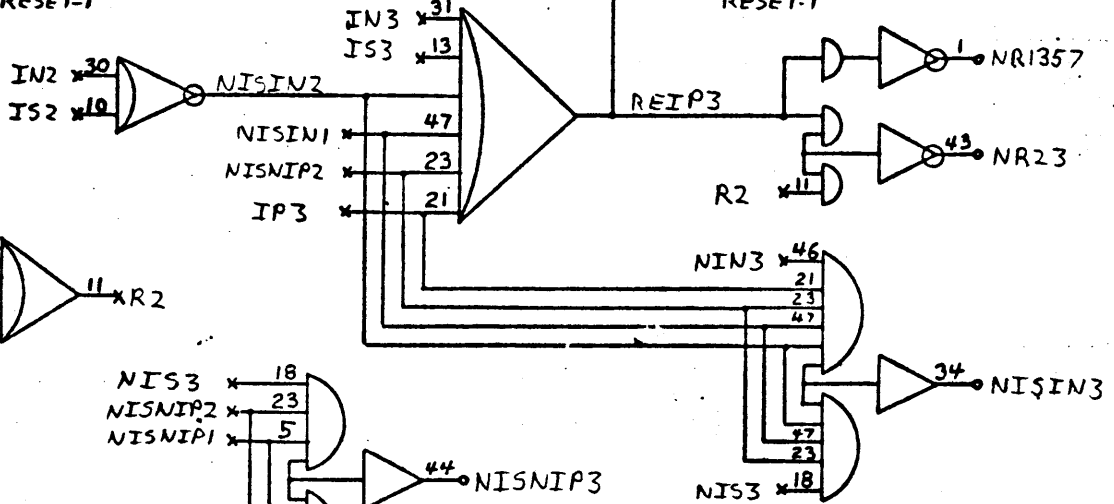
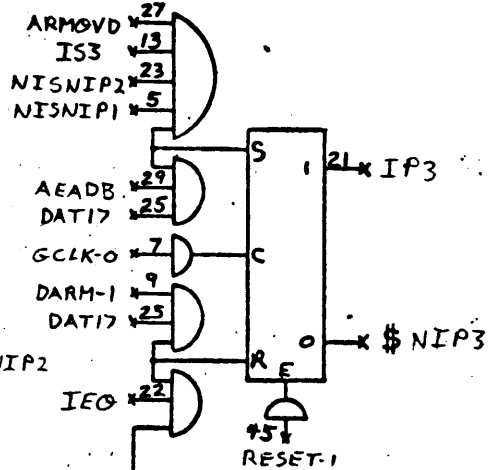
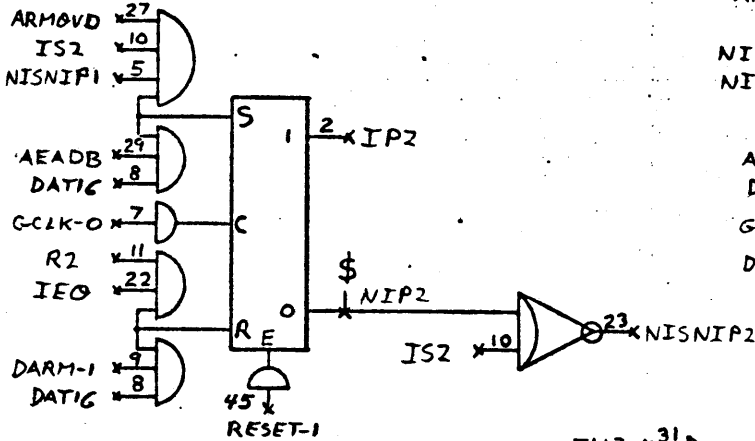
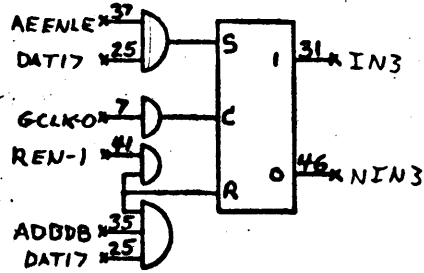
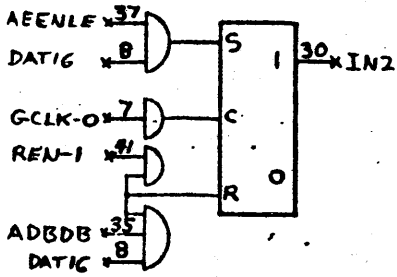
Page 1-50

POWER OFF
[51]

LT16 INTERRUPT $\Sigma 5(26R)$

OVERRIDE GROUP

Cochrane



COUNTER #1
[52]

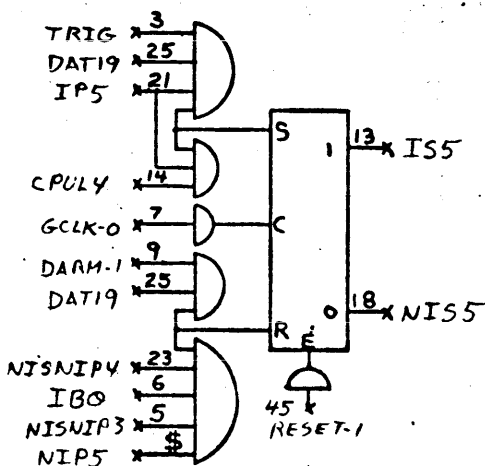
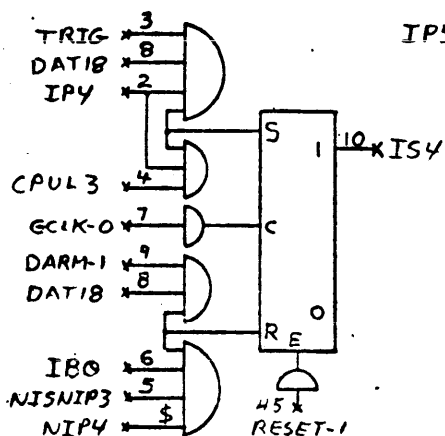
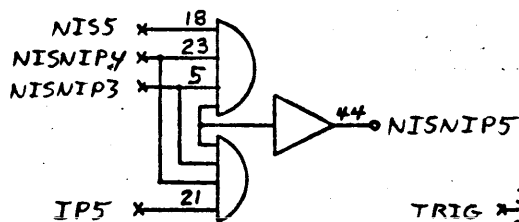
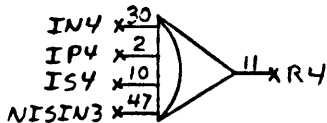
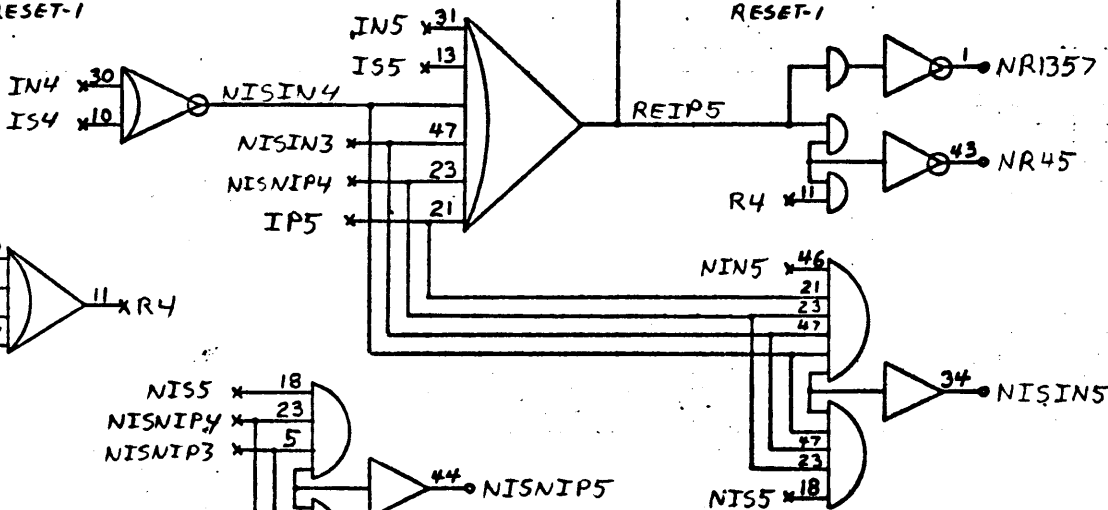
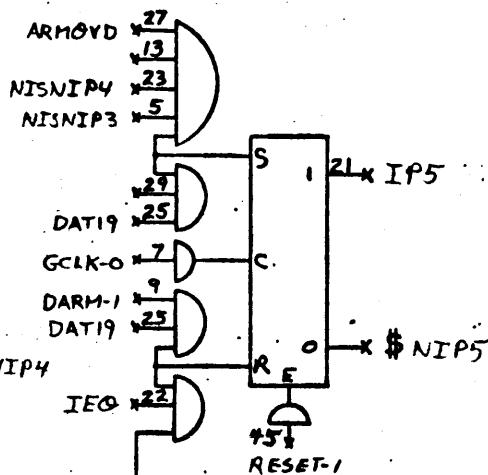
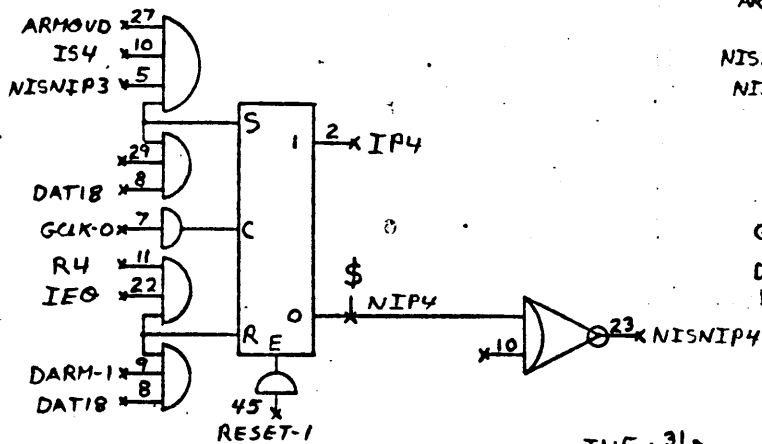
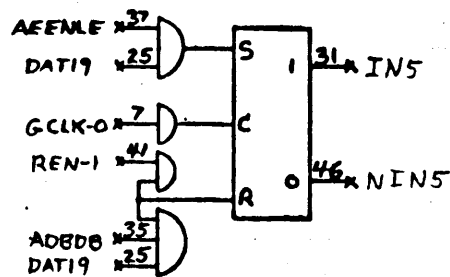
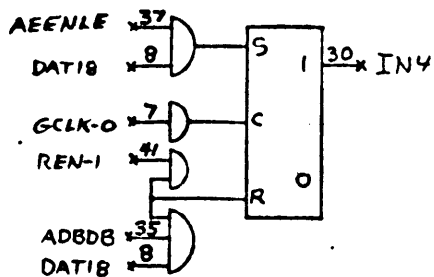
$\Sigma 5(26R)$
OPTIONAL

COUNTER #2
[53]

LT16 INTERRUPT $\Sigma 5 (27R)$

OVERRIDE GROUP

Adrian



COUNTER #3
[54]

$\Sigma 5 (27R)$

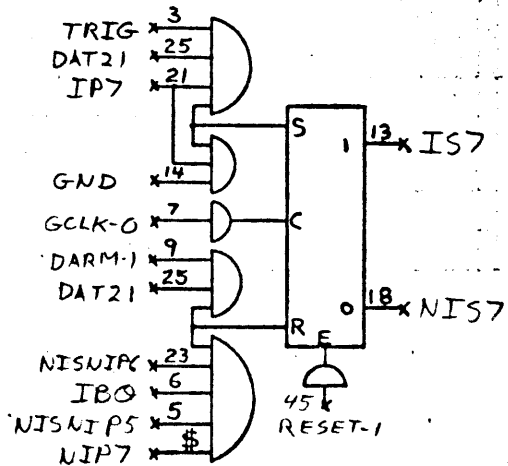
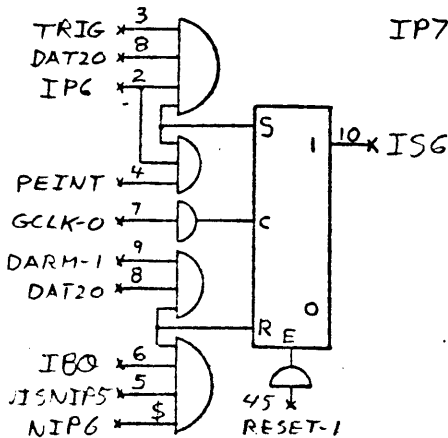
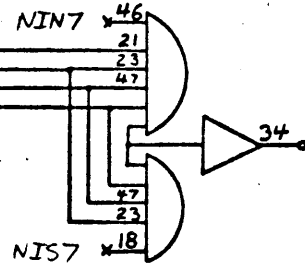
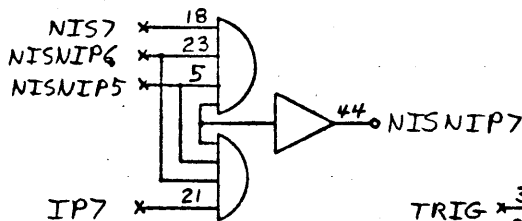
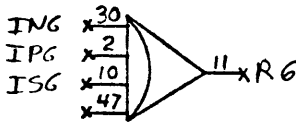
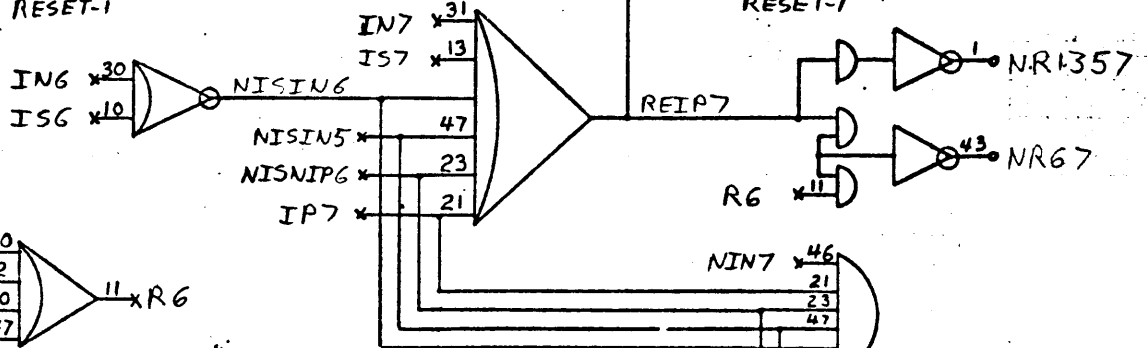
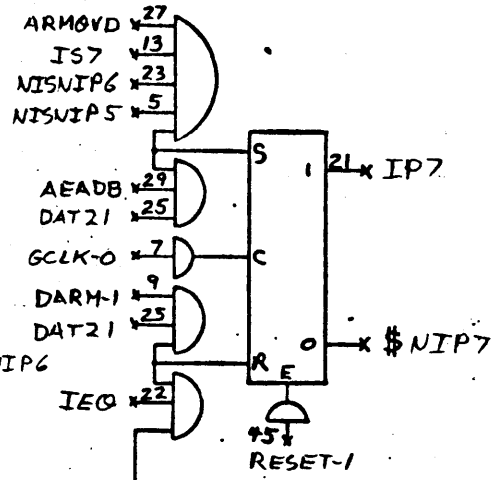
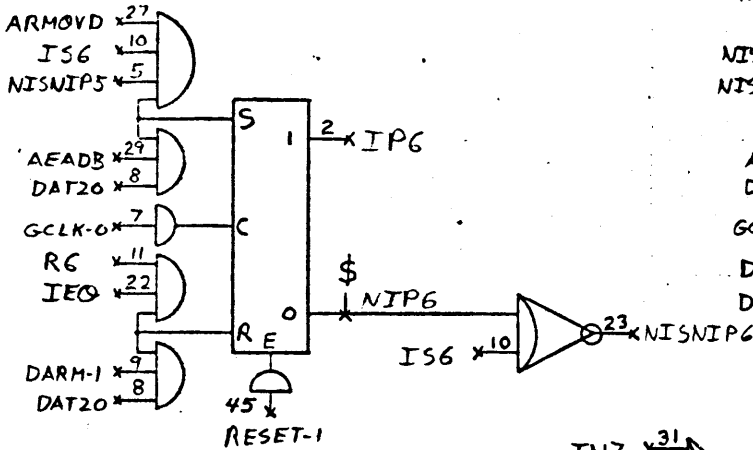
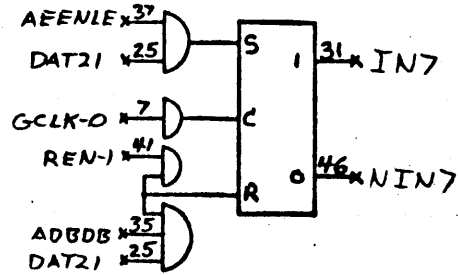
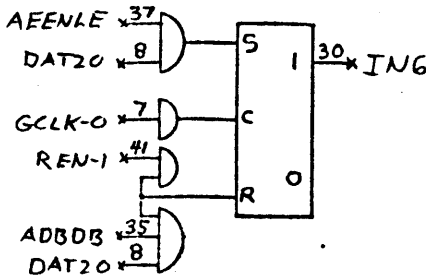
COUNTER #4
[55]

LT16 INTERRUPT

Σ5 (28R)

OVERWRITE GROUP

Lab 1



MEM. PARITY

[56]

Σ5 (28R)

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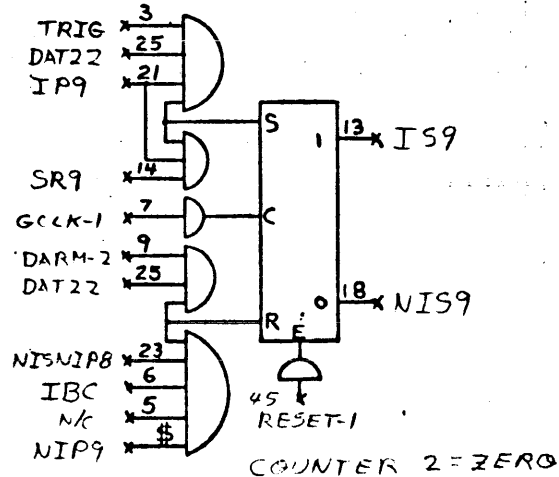
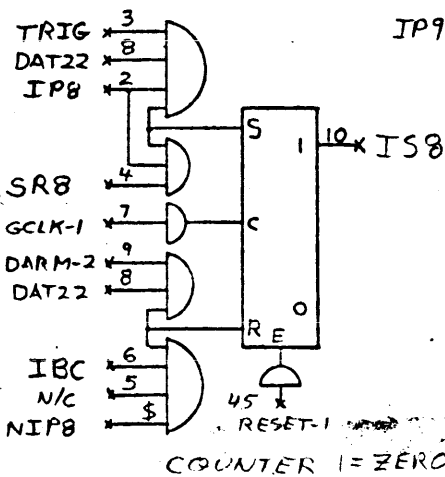
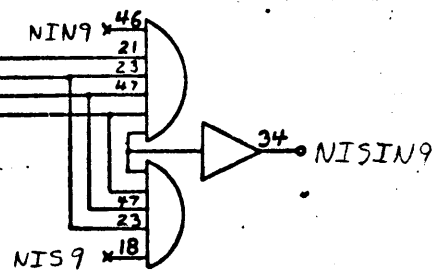
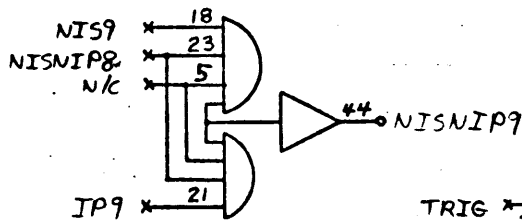
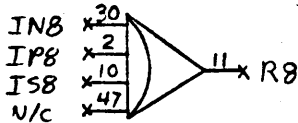
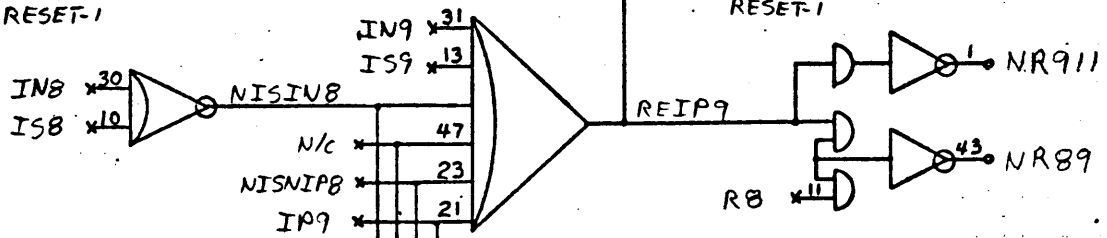
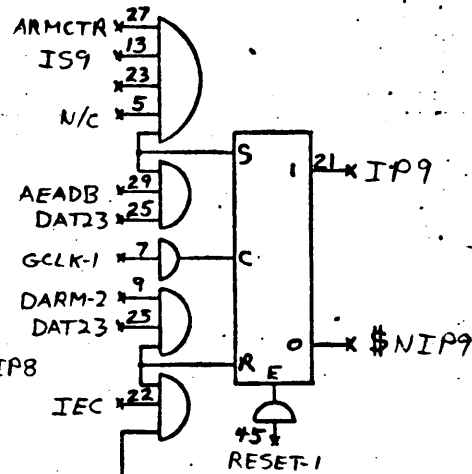
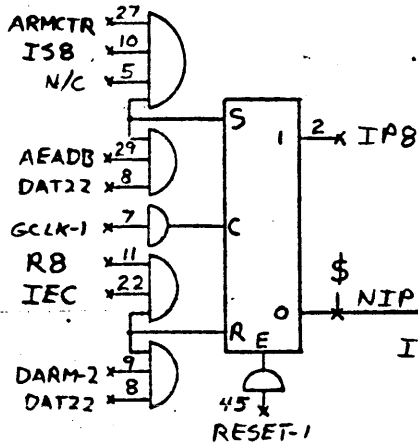
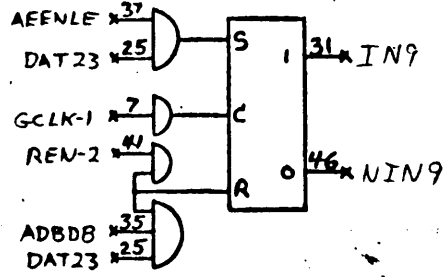
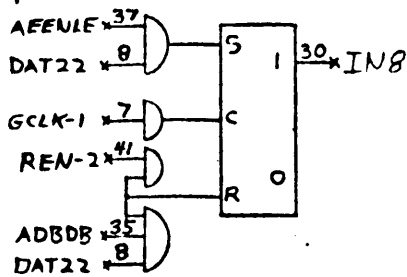
UNASSIGNED

[57]

LT16 INTERRUPT $\Sigma 5$ (29K)

COUNTER GROUP

Cochrane



[58]

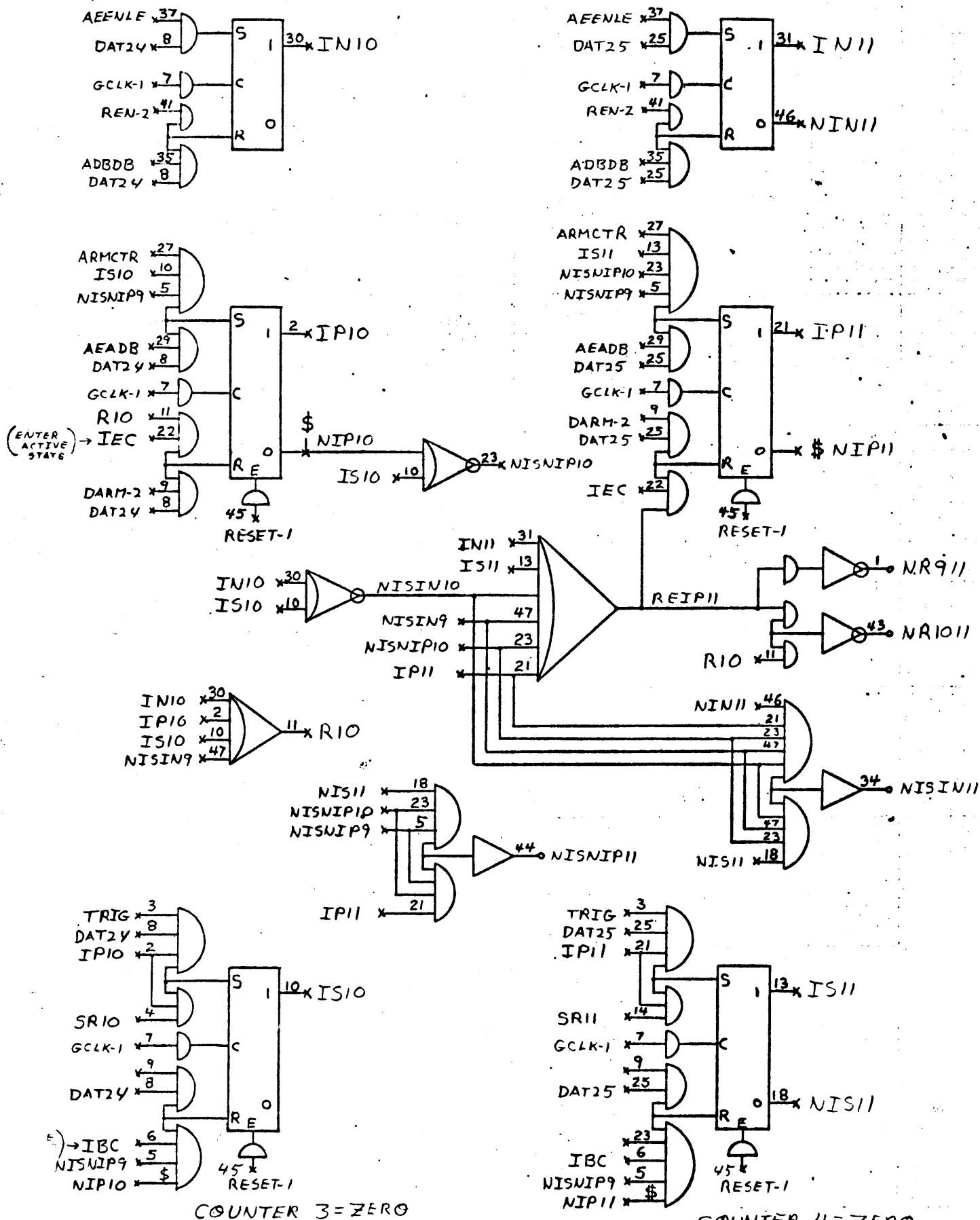
$\Sigma 5$ (29K)
OPTIONAL

[59]

LT16 INTERRUPT (COUNTER GROUP)

Σ5 (30R)

Cochrane



COUNTER 3=ZERO

COUNTER 4=ZERO

[5A]

Σ5 (30R)

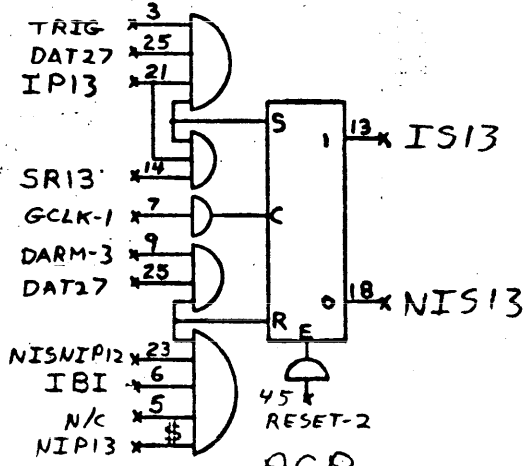
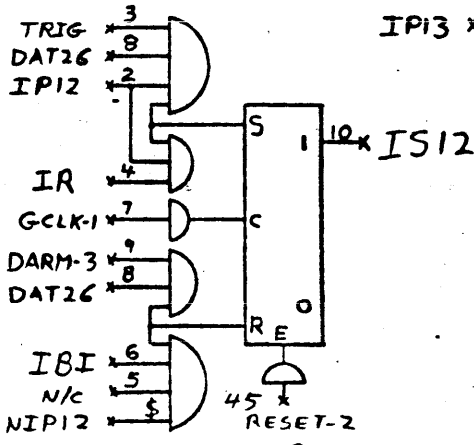
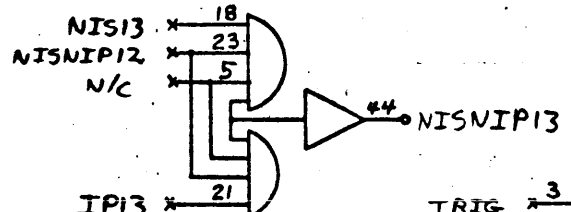
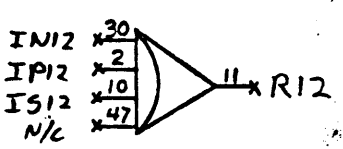
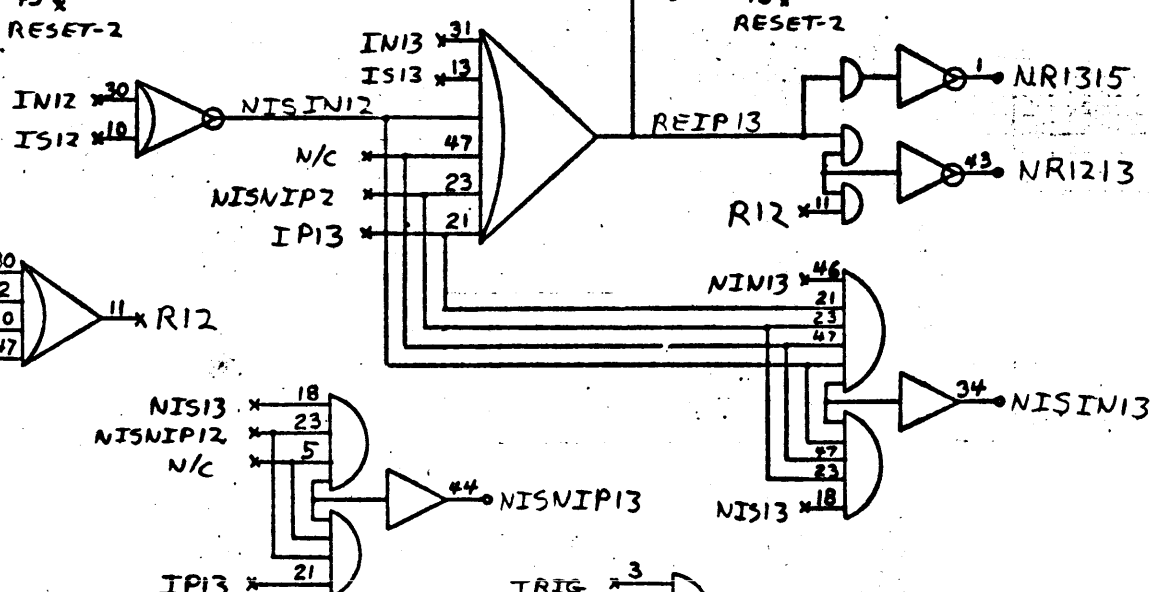
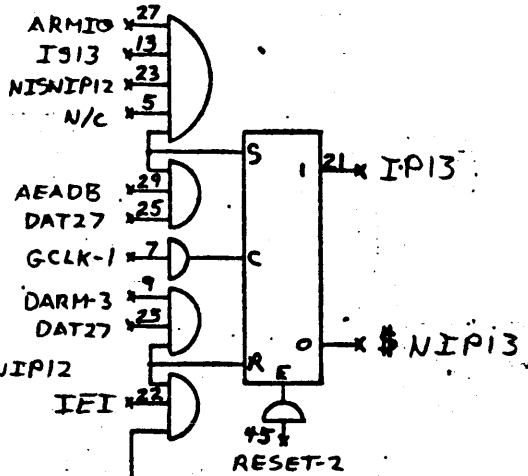
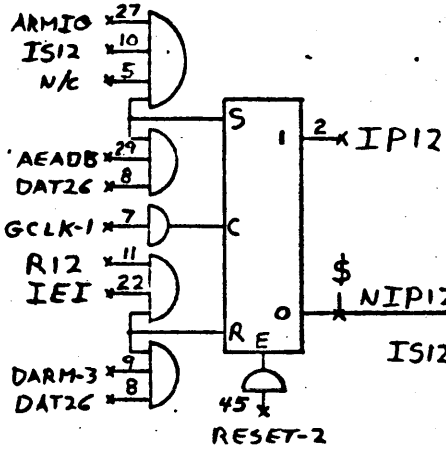
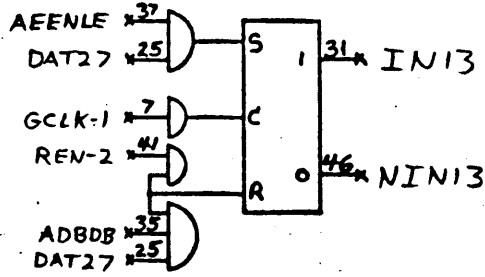
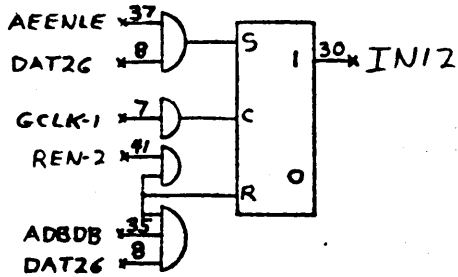
[5B]

LT16 INTERRUPT

Σ5 (31R)

INPUT/OUTPUT GROUP

Cochrane

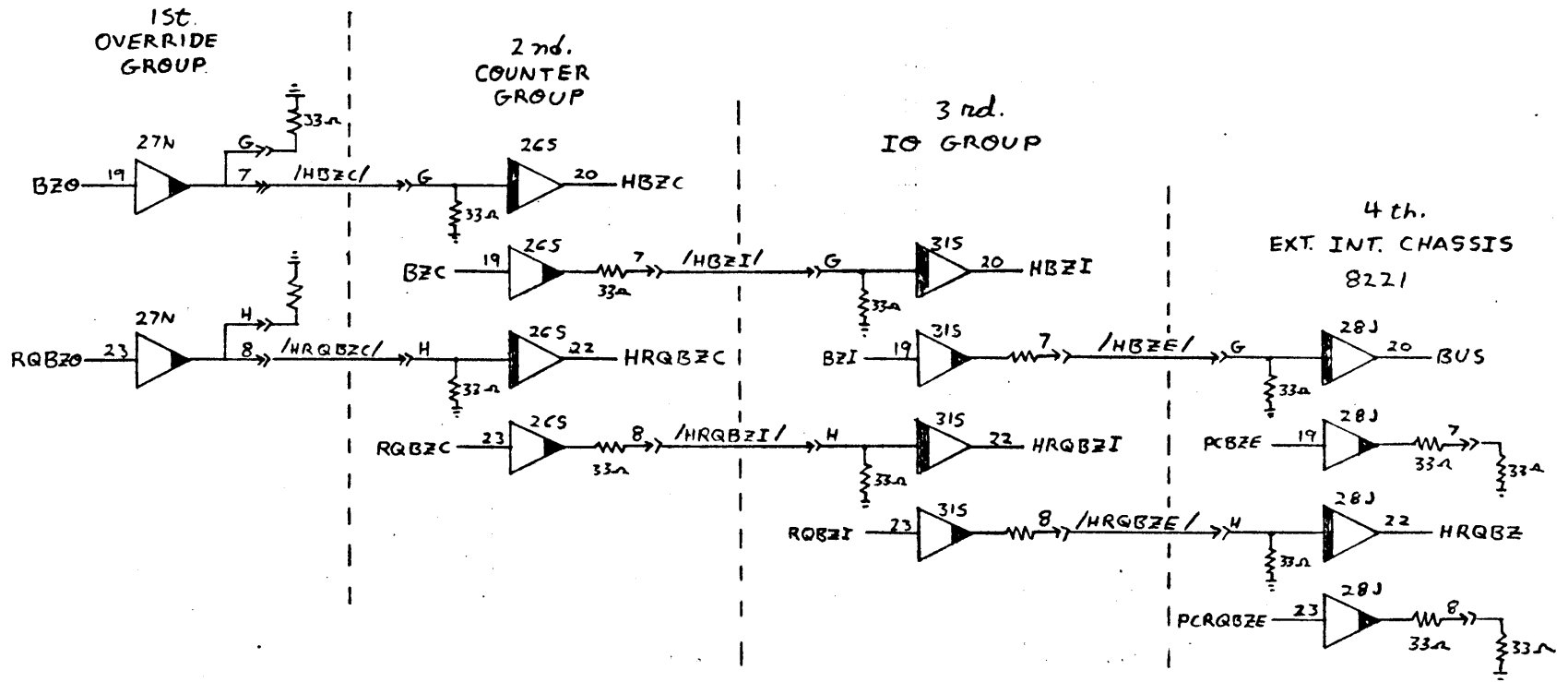


IO
[5C]

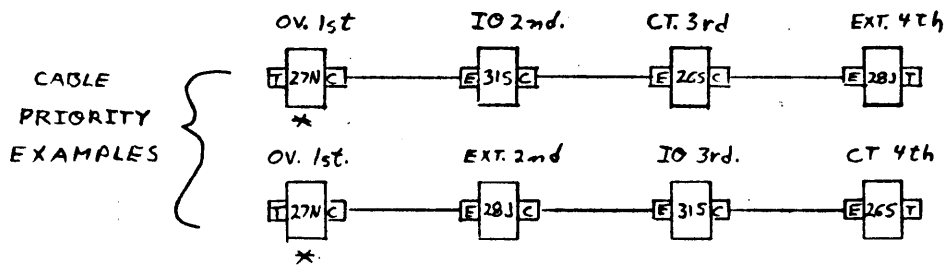
Σ5 (31R)

PCP
[5D]

INTERRUPT PRIORITY CHAIN 25



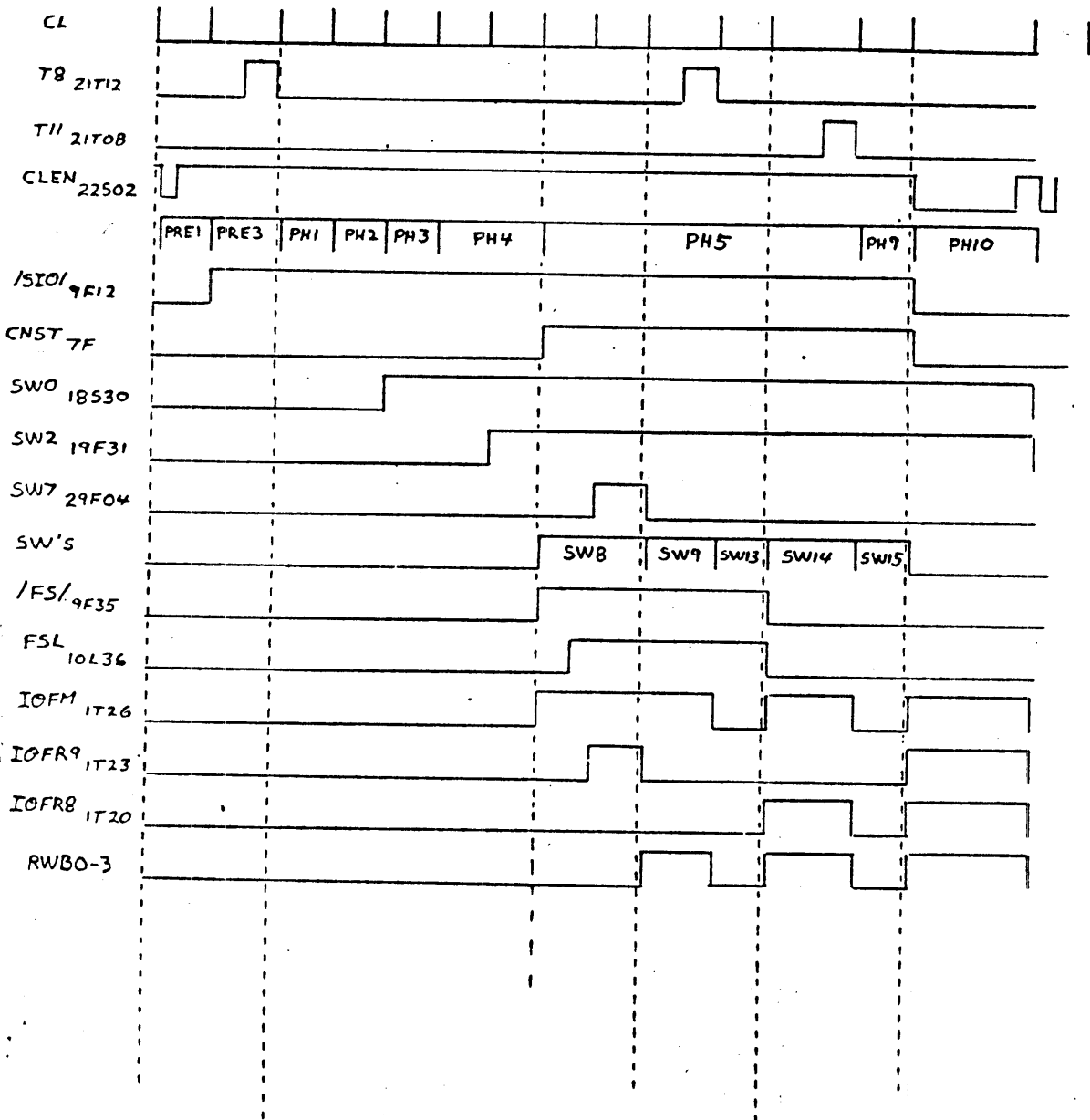
Page 1-57



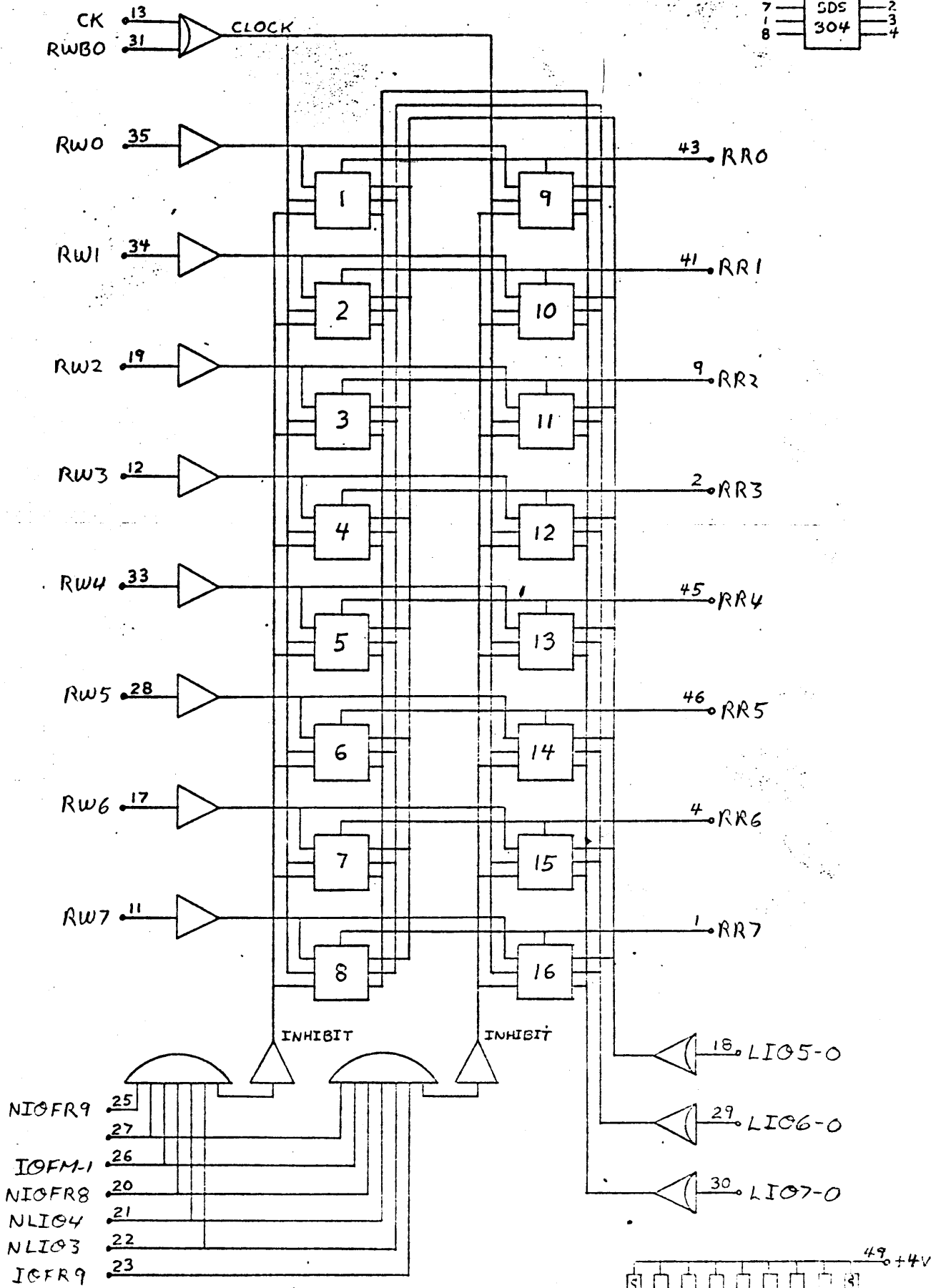
* NOTE
OVERRIDE GROUP
ALWAYS FIRST PRIORITY

Coelmann

Σ5 IIOP SIO TIMING



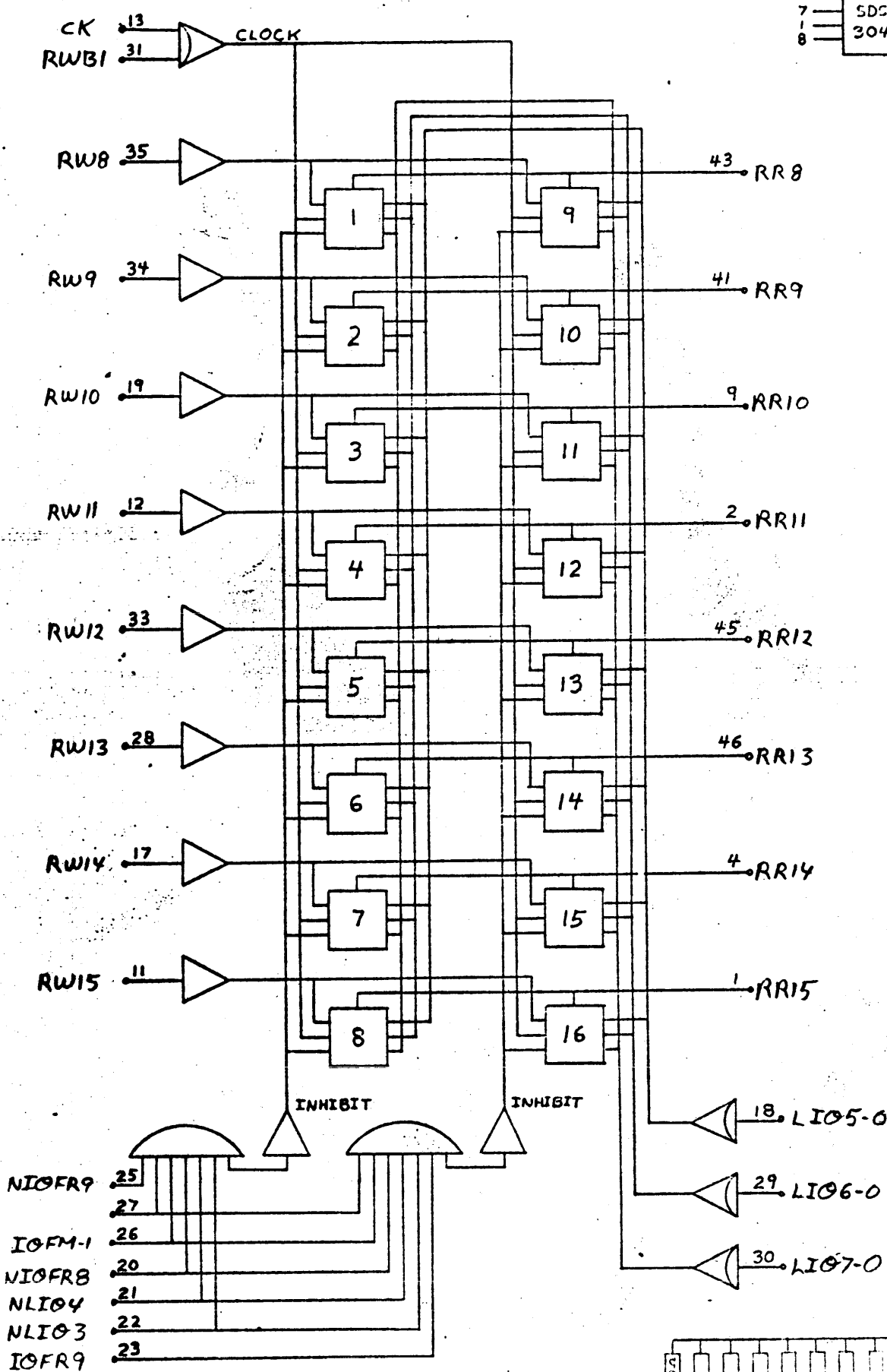
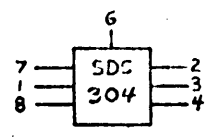
FT25 INTEGRAL IOP (5K)



Σ5 INTEGRAL IOP

(5K) NIOR9 = STATUS
IOFR9 = FLAGS

FT25 INTEGRAL IOP 23K

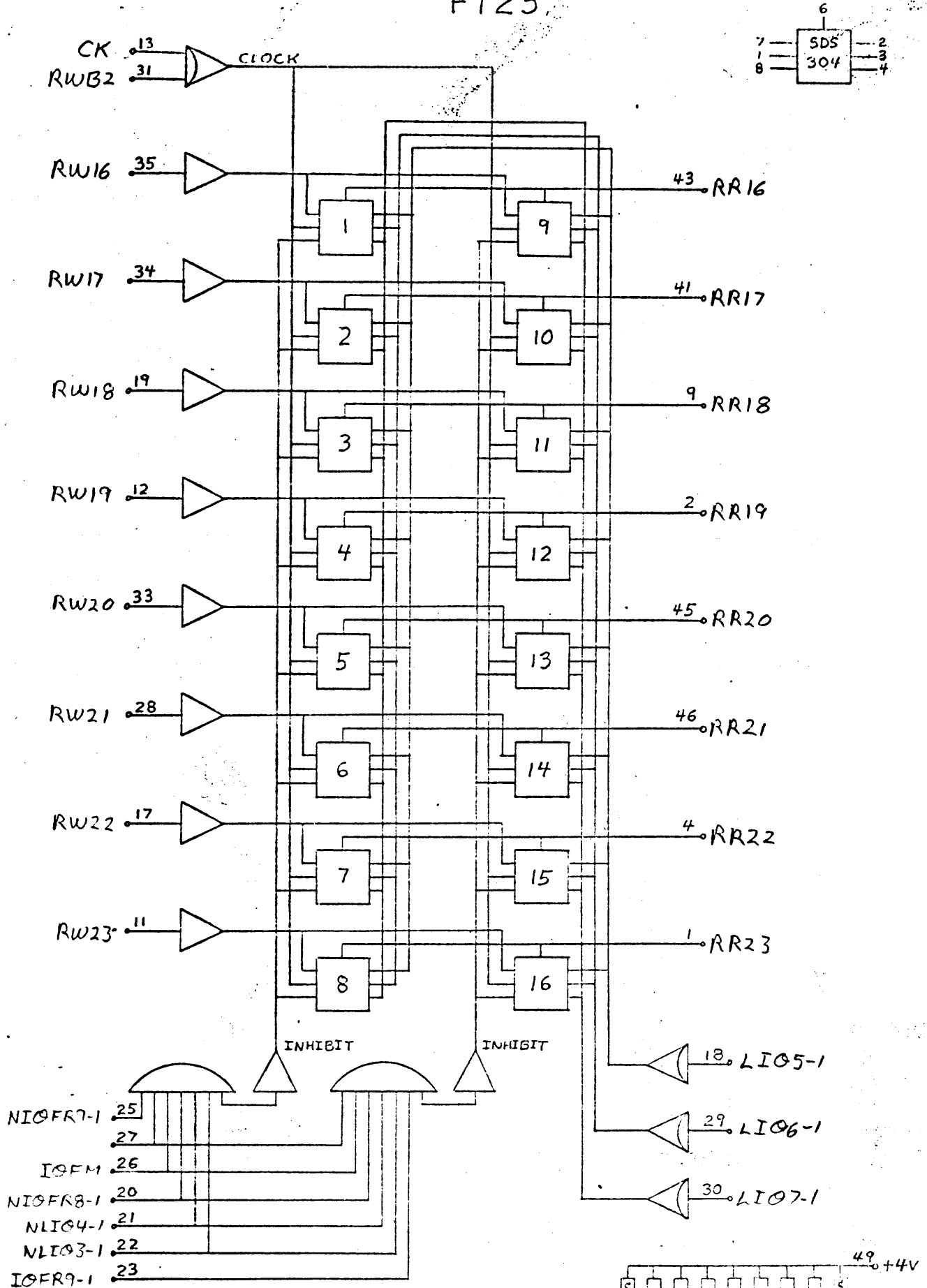


Σ5 INTEGRAL IOP

(23K)

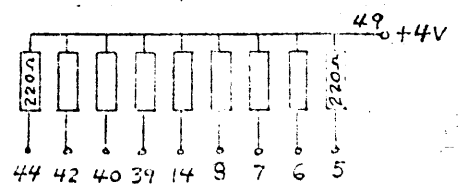
NIOFR9 = STATUS
 IOFR9 = LSB BYTE ADDR. BIT RR8/RR9 → P32 & P33

FT25 INTEGRAL IOP (15)



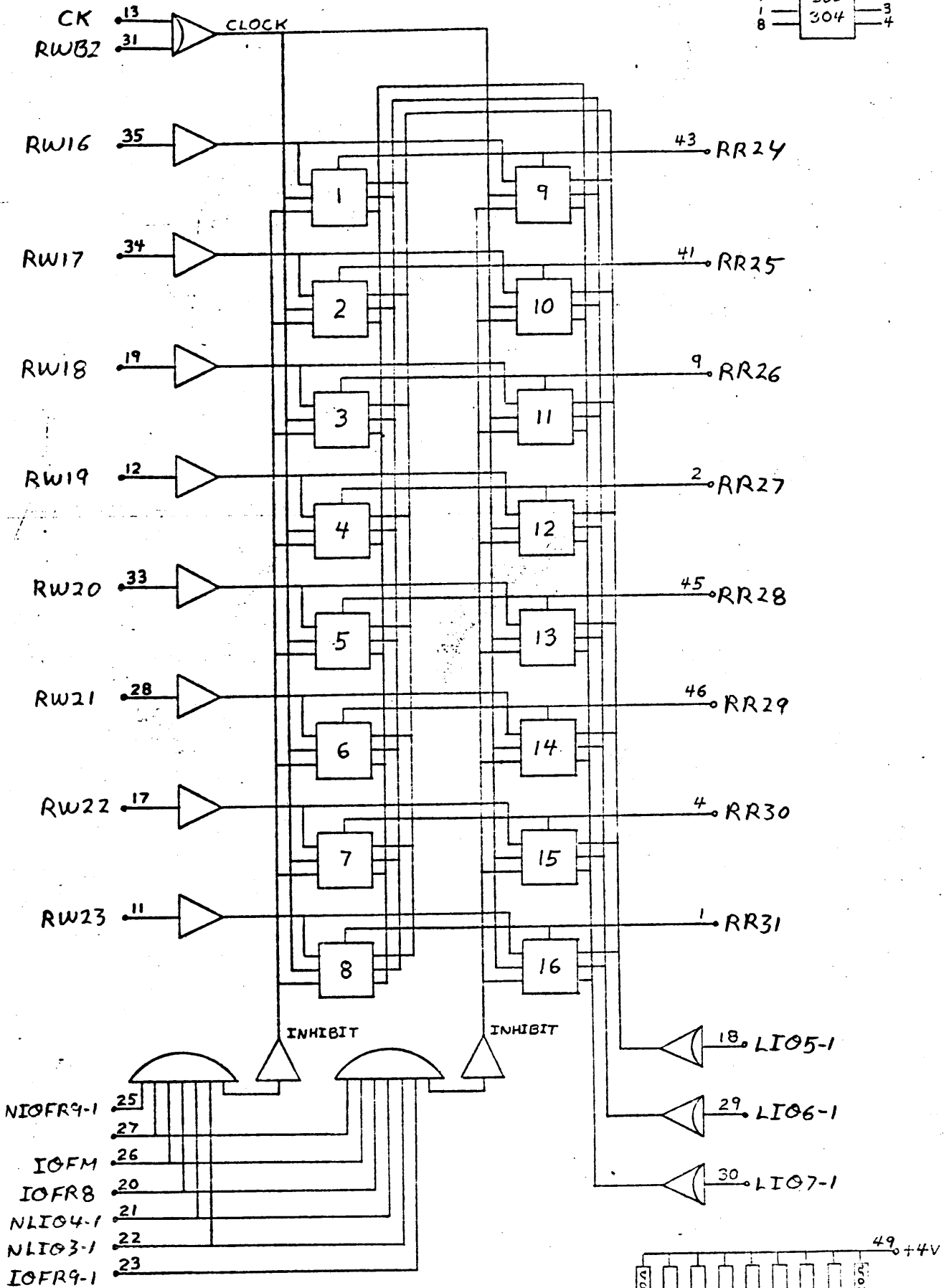
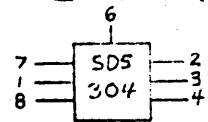
Σ5 INTEGRAL IOP

(15) NI0FR9 = BYTE ADDRESS
IOFR9 = BYTE COUNT



FT25

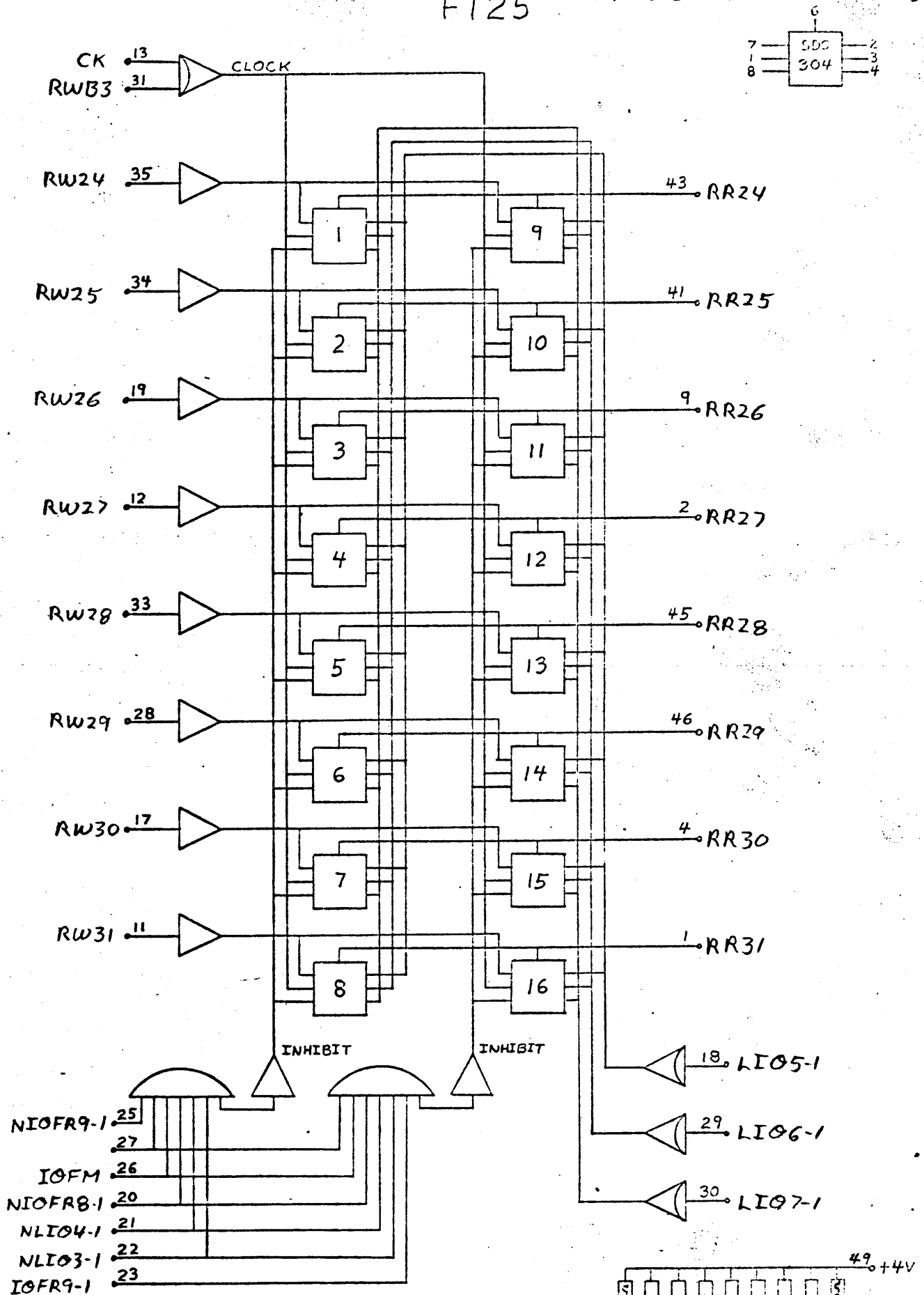
INTEGRAL IOP (IT)



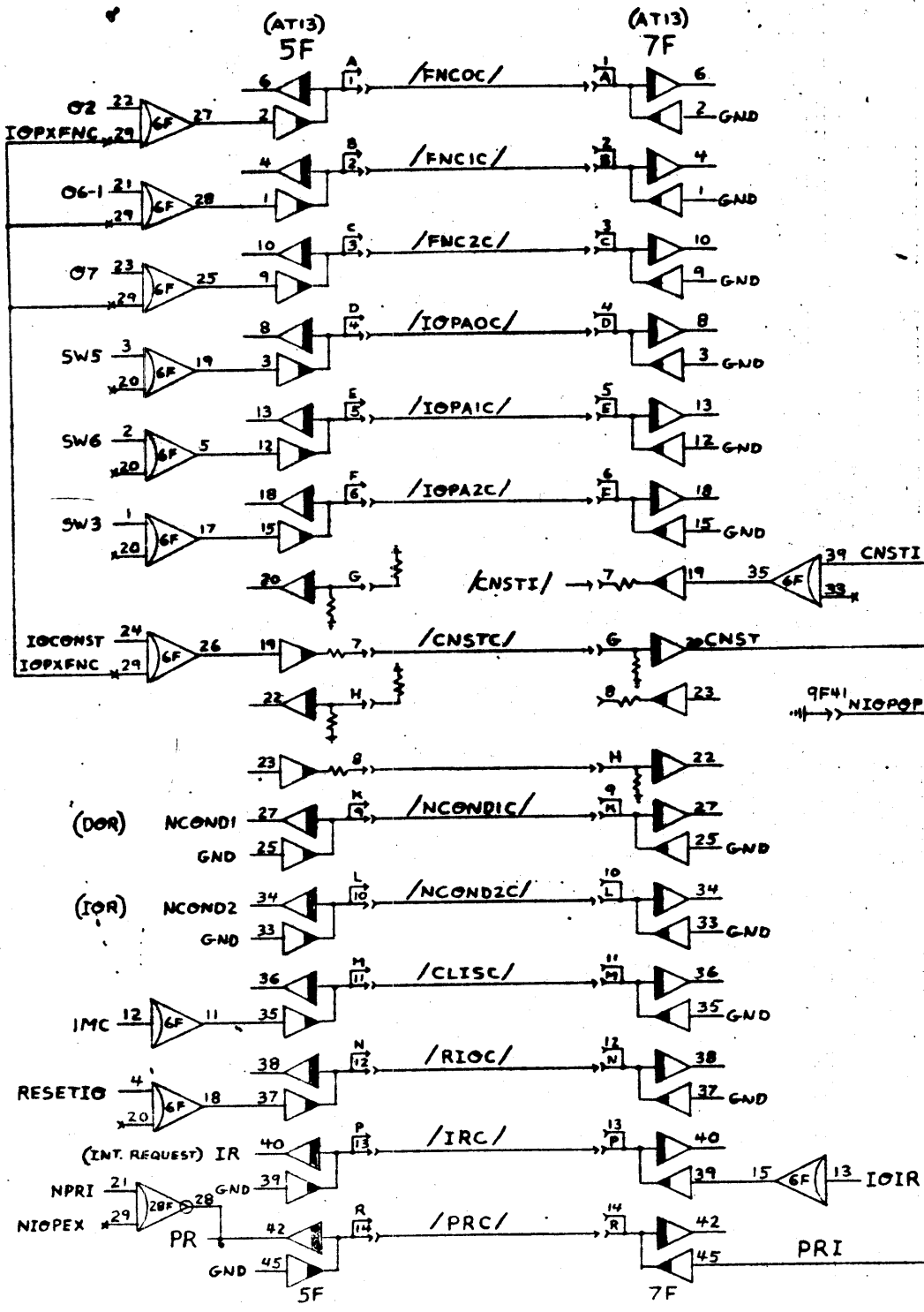
Σ5 INTEGRAL IOP

IOFR8 · NIOFR9 = MS BYTE COMMAND DBW ADDR
 IOFR8 · IOFR9 = LS " " " "

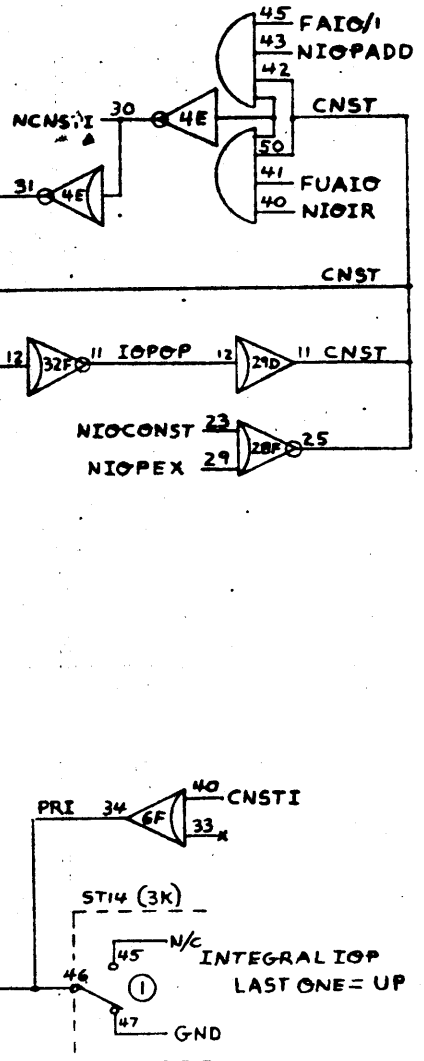
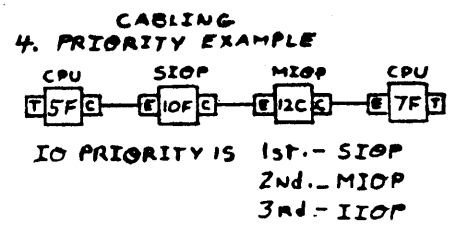
FT25 INTEGRAL IOP (5T)



Σ5 INTEGRAL IOP (5T)
 NIOFR9 = BYTE ADDRESS
 IOFR9 = BYTE COUNT



- NOTE**
1. INTEGRAL IOP ONLY.
5F & 7F REMOVE
 2. IIOP & MIIOP OR SIIOP
5F & 7F INSTALLED
 3. MIIOP ONLY
9F & 7F REMOVE
5F INSTALLED



COCHRANE
4/30/69

INTEGRAL IOP
LAST ONE = UP

FRI 27

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	BT 18	IT 16	BT 16	GT 11	GT 11	FT 22	FT 22	XT 10	FT 22	GT 11	GT 11	GT 11	FT 22	FT 22	FT 22	GT 11	LT 14	LT 14	IT 16	IT 16	IT 26	LT 20	IT 20	XT 10	LT 14	LT 20	IT 24	IT 20	IT 25	IT 25	BT 16	32 K	
B	32 H ↓	31 H ↓	IT 16	IT 26	LT 14	LT 14	LT 14	XT 10	LT 14	BT 10	BT 11	LT 14	BT 10	IT 26	BT 11	AT 21	IT 25	XT 23	LT 21	IT 16	LT 13	IT 25	IT 25	XT 10	IT 16	IT 25	BT 16	IT 11	XT 10	XT 10	32 U	32 L	
C	32 G ↓		IT 16	IT 26		LT 21	BT 18	BT 11	LT 14	XT 10	LT 14	IT 20		IT 20	BT 10		XT 10	IT 20		IT 26	IT 20		IT 26	XT 10		IT 26	LT 20		IT 20		LT 14	LT 14	
D			IT 16	IT 20		IT 20	IT 20	IT 26	LT 20	XT 10	LT 21	IT 16		LT 20	AT 11		BT 16	IT 20		XT 10	IT 20		XT 10	LT 14		IT 25	IT 16		IT 25		31 N	32 N	
E	AT 21		IT 25	IT 25	BT 11	BT 11	IT 16	XT 10	LT 20	LT 14	IT 26	FT 22	IT 16	BT 16	XT 23	XT 10	IT 16	LT 21	LT 13	LT 13	BT 17	BT 11	IT 25	XT 10	BT 11	IT 26	LT 13	FT 22	GT 11	FT 22	LT 13	31 U	
F		IT 16	IT 26		IT 20	IT 20	LT 20	IT 25	LT 13		LT 13			LT 14	LT 14		LT 14	LT 14		BT 11	GT 10		FT 22	XT 10		FT 22	GT 11		IT 25	LT 20		32 Q	
G	32 C ↑		BT 11		BT 11	IT 16	BT 11	XT 10	IT 16		IT 20			IT 25	BT 11		IT 16	IT 24		LT 14	LT 21		LT 20	XT 10		IT 25	LT 20		IT 20	IT 16		LT 21	
H	32 B ↑	31 B ↑	IT 25	LT 21	IT 16	LT 21	LT 21	LT 14	IT 25	BT 11	LT 20		IT 16	XT 10		IT 26	IT 20	LT 20	LT 20	IT 20	IT 20	LT 20	IT 24		LT 20	XT 10	IT 20	BT 11	BT 10	BT 16	30 S	31 S	32 S
I	BT 10	BT 16	BT 11	BT 11	BT 11	BT 11	BT 11	BT 11	BT 11	BT 10	BT 11	BT 11	BT 10	LT 14	XT 10	IT 16	IT 24	LT 20		IT 16	IT 20	IT 20	LT 20	IT 20	IT 20	XT 10	LT 20	IT 20	IT 20	BT 11	LT 21	32 T	
J	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Page 2-1

F = FLOATING POINT 8418
D = DECIMAL ARITHMETIC 8419

200

FR2 Σ7

K
L
M
N
O
P
Q
R
S
T

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
K	A	30 U	AT 11	IT 16	XT 10	IT 26	AT 21	IT 16	FT 22	FT 22	IT 16	IT 26	XT 10	FT 18	FT 18	FT 22	FT 22	FT 17	FT 17	FT 17	FT 17	LT 13	LT 18	LT 18	LT 18	IT 16	FT 17	FT 17	FT 22	XT 10	FT 17	FT 17		
L	B		IT 16	AT 11	BT 18	BT 16	XT 10	FT 18	GT 11	FT 18	FT 18	GT 11	FT 22	FT 17	FT 17	XT 10	FT 17	FT 17	GT 10	FT 17	FT 17	XT 10	FT 17	FT 17	BT 16	XT 10	LT 21	XT 10 AT/11	FT 25	FT 25	FT 25	FT 25 16-23		
M	32 R		LT 21	AT 21		BT 17			LT 17	LT 17		LT 17	LT 17	IT 16		BT 17	LT 17	LT 17			LT 17	LT 17		BT 17	LT 17	LT 17		LT 17	LT 17	XT 10	BT 18	BT 17	BT 17	
N	D	2 D		AT 11		AT 11	BT 16		BT 17	XT 10		IT 26	XT 10	IT 16		AT 21	IT 16	LT 21			LT 18	XT 10		LT 18	LT 18	FT 22		GT 11	GT 10	FT 17	FT 17	FT 17	FT 17	
O	ZT 23		AT 11	BT 16	AT 21	IT 16	XT 10	BT 16	LT 21	LT 20	BT 16	LT 13	LT 21	AT 11	XT 10	DT 16	FT 17	GT 11	FT 17	GT 11	GT 10	FT 17	GT 10	FT 17	FT 22	XT 10	LT 17	LT 17	LT 17	LT 17	IT 16	XT 10		
P			AT 11	IT 16		AT 11	IT 17	LT 17	IT 17		LT 13	BT 17	XT 10	BT 17		BT 17	IT 16	FT 18			BT 16	IT 16		XT 10	FT 22	FT 22		BT 16	AT 11	FT 25	FT 25	FT 25	FT 25 24-31	
Q	32 M		XT 10	AT 21		LT 17	LT 17	LT 17	LT 17		FT 17	FT 17	GT 11	LT 17		LT 17	LT 17	LT 17			XT 10	IT 16		BT 16	LT 17	LT 17		LT 17	LT 17	FT 17	FT 17	GT 11	FT 22	
R				IT 16	BT 18	XT 10	AT 21	FT 17	FT 17	AT 11	BT 16	AT 11	FT 17	FT 17	GT 11	FT 22	FT 22	FT 18	FT 18	BT 16	XT 10	BT 16	IT 16	IT 16	BT 16	FT 22	FT 17	FT 17	FT 11	FT 17	FT 17	XT 10		
S		2 H	3 H																															
T			BT 18	FT 22	IT 16	XT 10	FT 17	FT 17	FT 17	FT 17	FT 17	IT 26	LT 18	AT 11	FT 25	FT 25	FT 25	FT 25	IT 26	BT 18	IT 16	IT 26	LT 18	LT 18	XT 10	BT 17	IT 25	AT 11	FT 25	FT 25	FT 25	FT 25 0-7		
	J																																	

F = FLOATING POINT 8418 D = DECIMAL UNIT 8419
 F REGISTER EXTENSION 8416
 RX REGISTER EXTENSION INTERFACE

fpp

U
V
W
Y
J
A
B
C
D

U
V
W
Y
J
A
B
C
D

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
RC 2 B	RC 1 E	RC 31 K	AT 23 RX	ZT 23 RX	AT 23	ZT 23	AT 23	ZT 23	AT 23	ZT 23	AT 23	HT 15	DT 14	DT 15	DT 14	HT 16	HT 15	HT 16	HT 15	DT 14	HT 16	LT 29	XT 10	FT 22	BT 17	LT 14	LT 14	DT 16	XT 10				
AT 10 Q 27		AT 11 J 26 PR3	LT 13	BT 16	AT 13	BT 16	FT 26	AT 12	IT 16	IT 16	IT 24	IT 24	BT 11	FT 22	BT 17	XT 10	BT 11	AT 11	DT 14	HT 15	LT 21	IT 25	BT 11	LT 21	LT 13	LT 13	IT 16	LT 21	IT 25	LT 21	XT 10		
AT 11 P 30	BT 17	ST 29		AT 13	BT 17	AT 12	XT 10	ST 14	LT 16	LT 16	LT 16	LT 16	BT 16	IT 25	LT 16	LT 16	LT 16	LT 16	LT 13	FT 28	FT 28	IT 25	IT 25	BT 11	IT 25	XT 10	CT 16	IT 25			IW		
FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	BT 10	AT 12	BT 16	XT 10	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	IT 24	IT 24	IT 16	IY		
AT 11		LT 26		AT 13		AT 11		BT 17	BT 16	IT 25	BT 17		AT 11		LT 16	LT 16	LT 16	LT 16		AT 11		LT 16	LT 16	LT 16	LT 16	IT 25	BT 18	XT 10			ST 14		
(PRIORITY INTERRUPT CHASSIS 8421)																14-15				12-15		10-11		8-9		6-7		4-5		2-3		0-1	
AT 11	FT 27	LT 13	IT 25	LT 12	IT 16	FT 27	FT 26	FT 26	FT 26	FT 26	FT 26	XT 10		AT 11	IT 16	AT 11	BT 11	AT 11	BT 11	AT 12	IT 25	AT 11	IT 25	LT 13	XT 10	FT 24	FT 24	IT 25		FT 24	FT 24		
(MULTIPLEXING IOP 8471)																																	
XT 10	FT 23	FT 23	FT 23	BT 11	FT 23	FT 23	XT 10	FT 24	FT 24	FT 27	FT 27	IT 16	IT 25	BT 11	IT 16	IT 25	BT 11	AT 10		FT 24	FT 24	BT 11	AT 24	FT 27	FT 27	LT 21	BT 11	XT 10	LT 21	BT 11			
32C	31C	FT 24	FT 24	FT 24	FT 24	FT 24	FT 24	FT 24	FT 24	FT 24	FT 24	BT 11	LT 13	IT 25	IT 25	IT 25	IT 25	XT 10	AT 12	LT 26	AT 13	IT 25	FT 24	9C	XT 10		FT 24	FT 24	LT 21	LT 13	IT 16	IT 25	
32D	31D	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	FT 25	XT 10	9D	HT 15	DT 11	HT 15	DT 11			AT 11		
		18-20	8-F	10-17	0-7	18-20	8-F	10-17	0-7	18-20	8-F	10-17	0-7	18-20	8-F	10-17	0-7	18-20	8-F	10-17	0-7	18-20	8-F	10-17	0-7								
		I	I	I	EA	I	I	I	BA	I	I	I	I	I	I	I	I	I	I	I	I	I	I	OF									

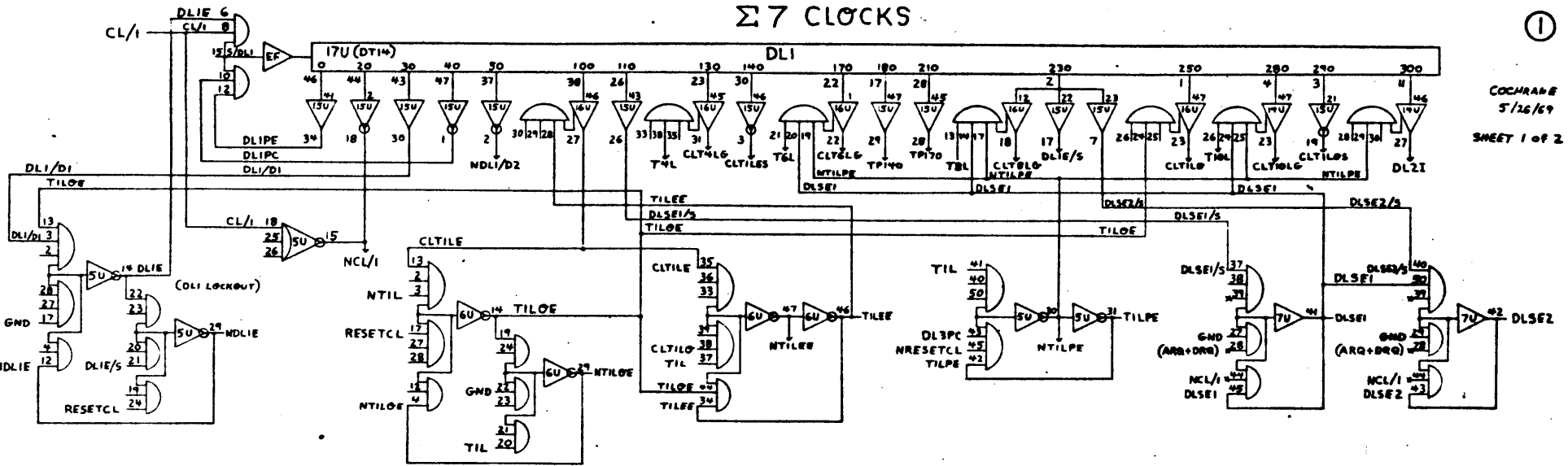
M = MAP 8415 XT19 CL. TERM. NO MAP
 MP = MEM. PROTECT 8414
 I = IO CHANNEL EXTENSION 8472
 C = COUNTER INTERRUPT
 P = PWR FAIL SAFE 8413
 RC = RIBBON CABLE
 RX = REGISTER EXTENTION INTERFACE UNIT

Page

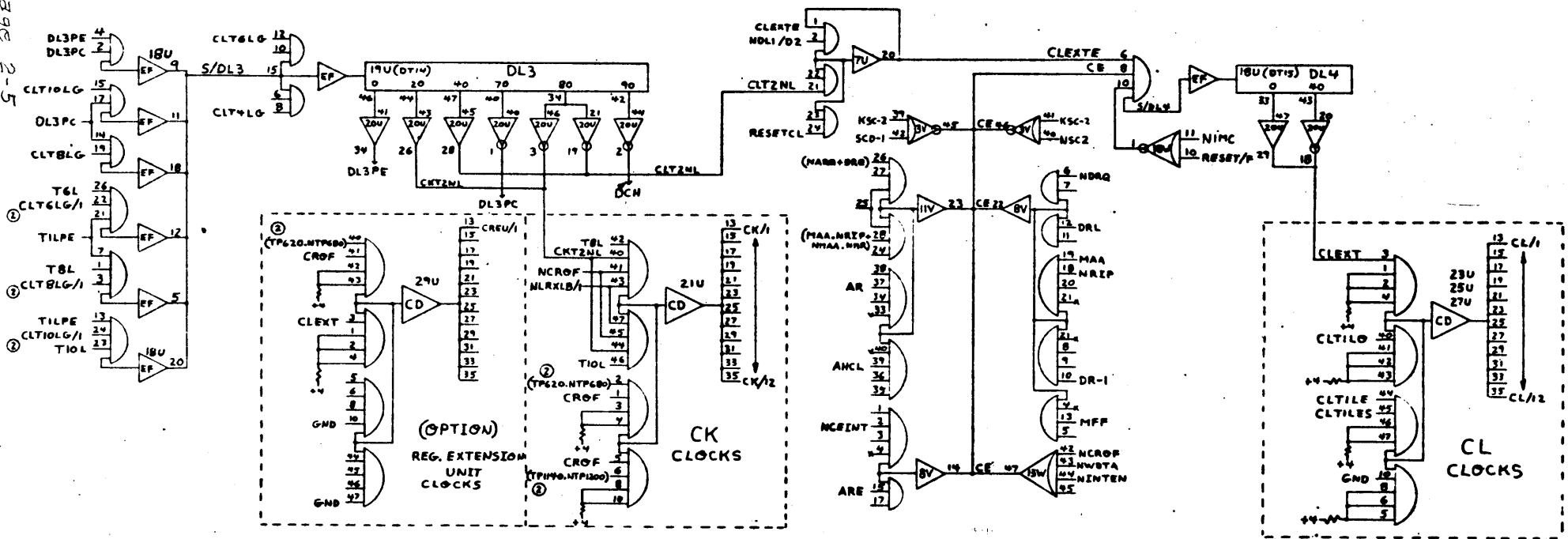
Σ 7 CLOCKS

①

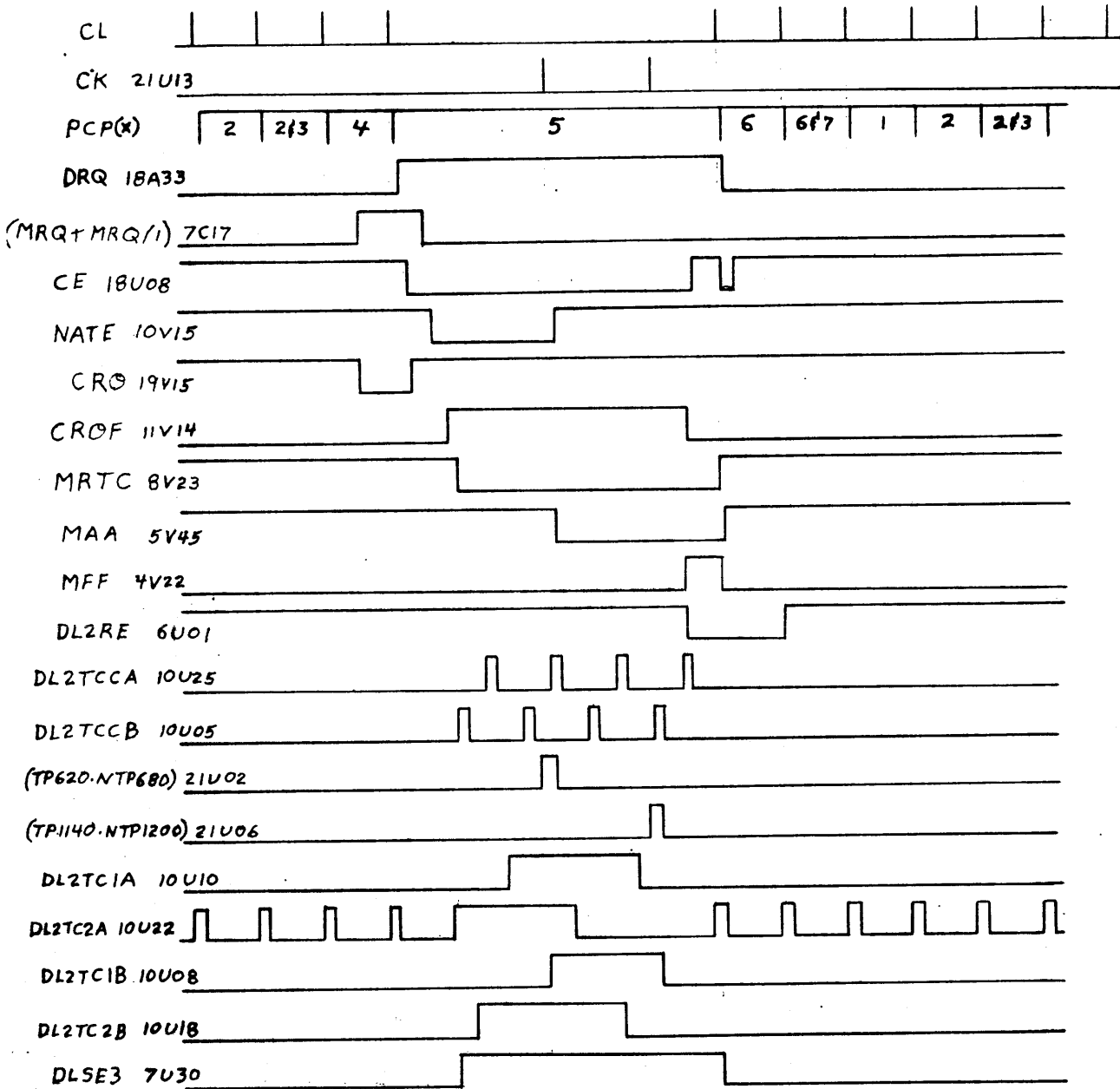
COCHRANE
5/26/69
SHEET 1 OF 2



Page 2-5



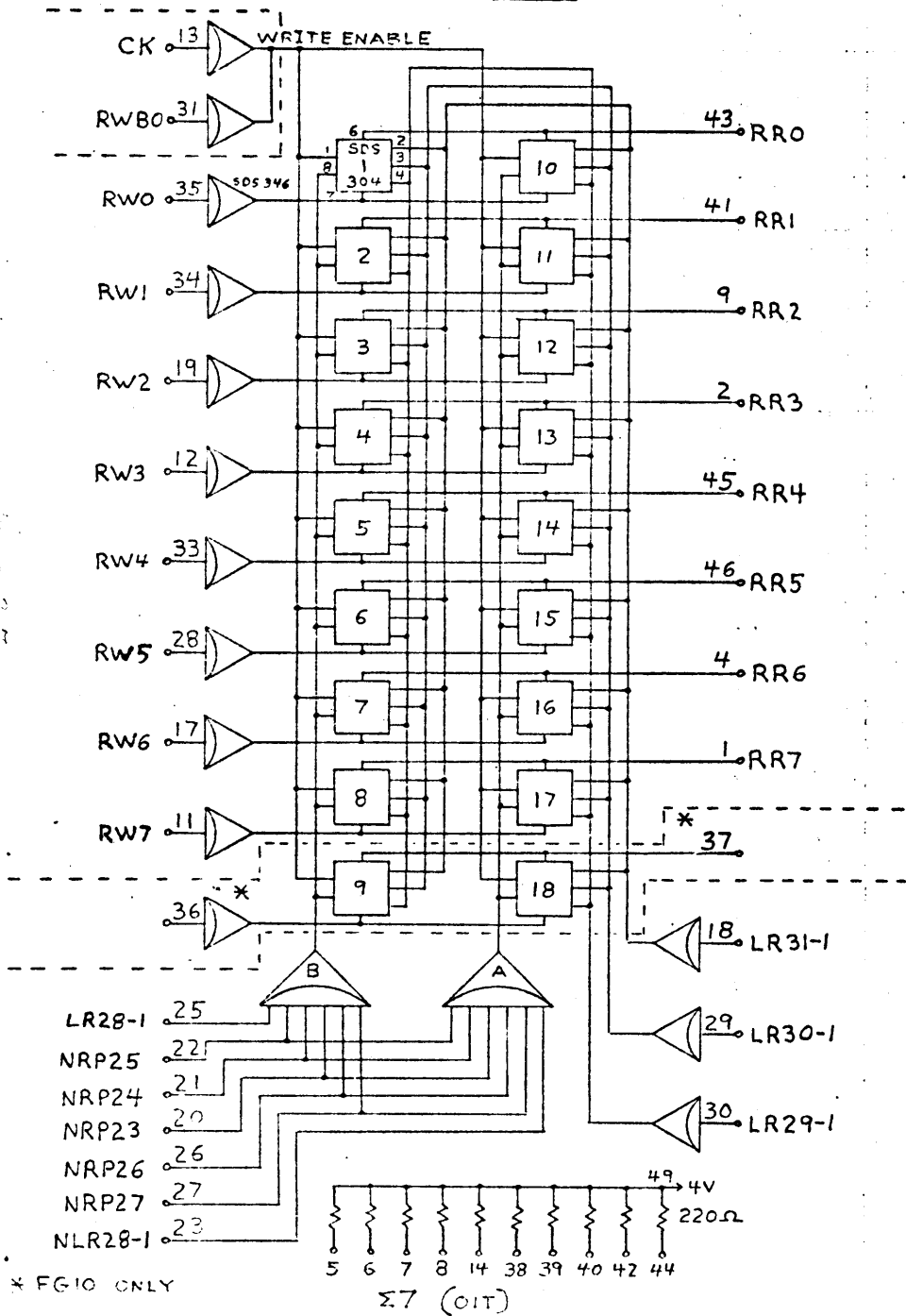
Σ7 CK GENERATION FOR FAST MEMORY



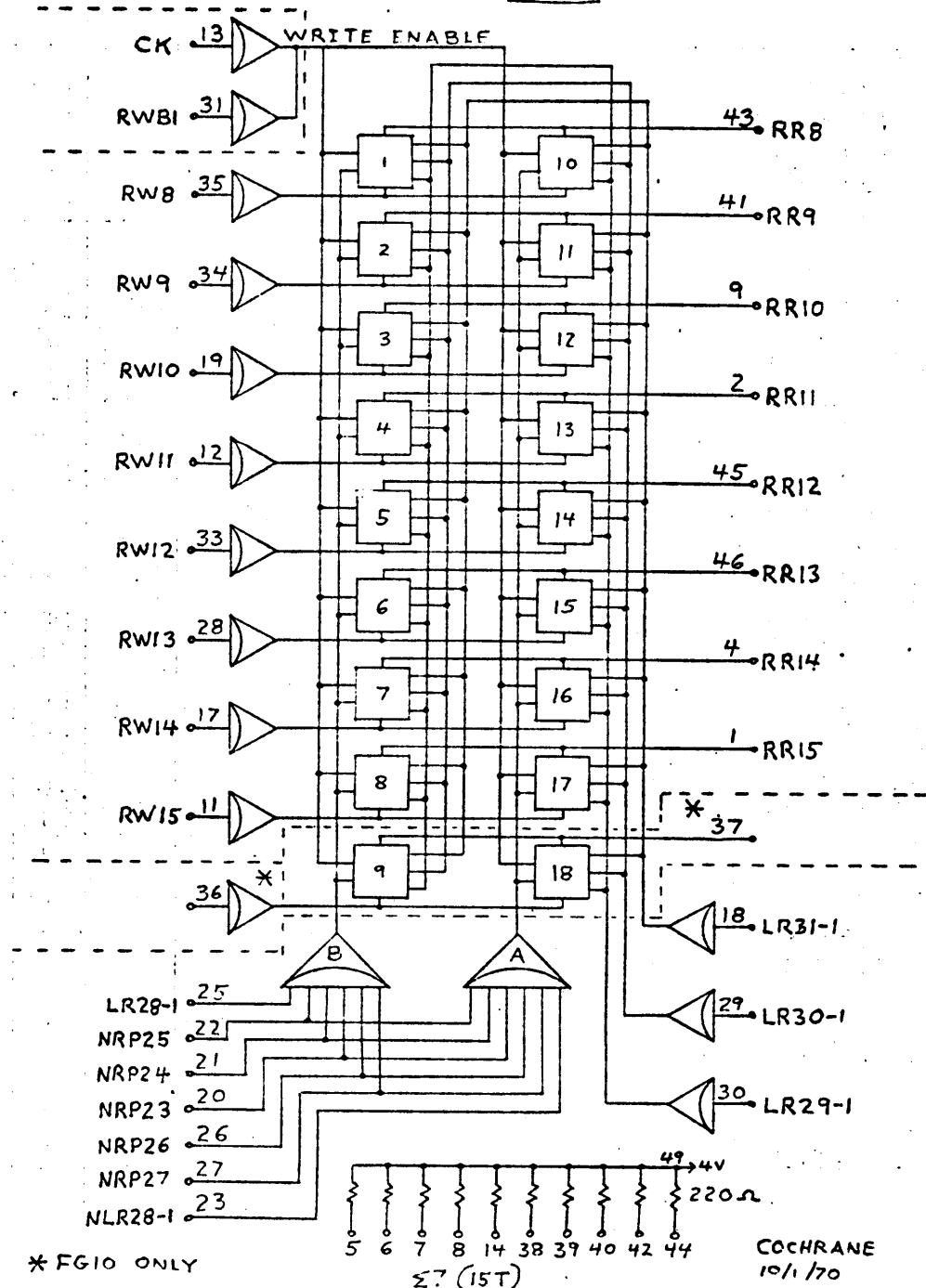
T6L-HIGH
 MBB, MCC, MDD, MEE - LOW
 MRQ/i - LOW

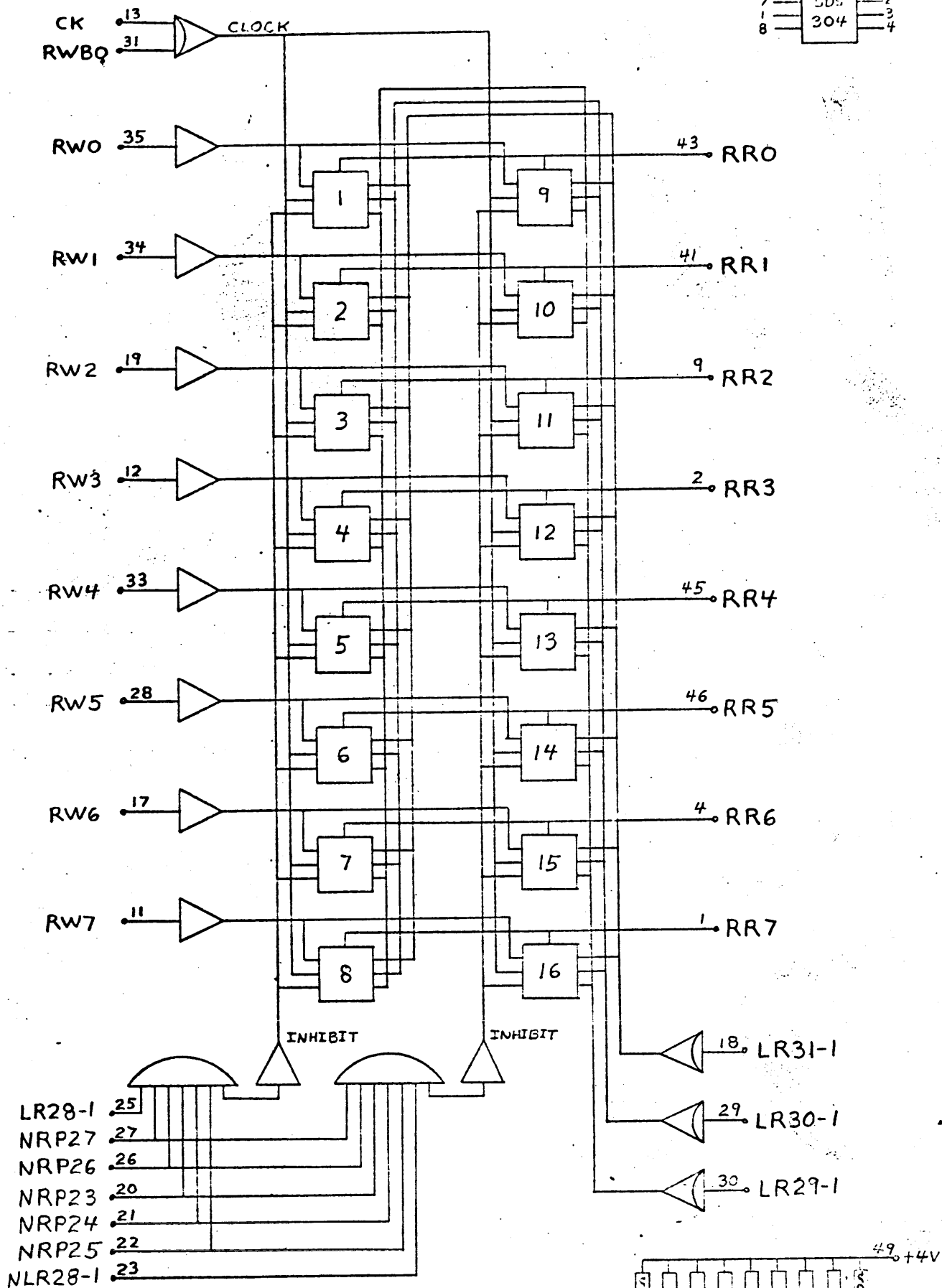
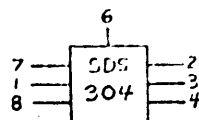
S/HALT 20A50 GND
 Q = 25
 SEL. ADD. SW'S = ZERO
 STORE SEL. ADD. SW. DOWN

Σ7 REGISTER (01T)
FG10/FT25



Σ7 REGISTER (15T)
FG10/FT25

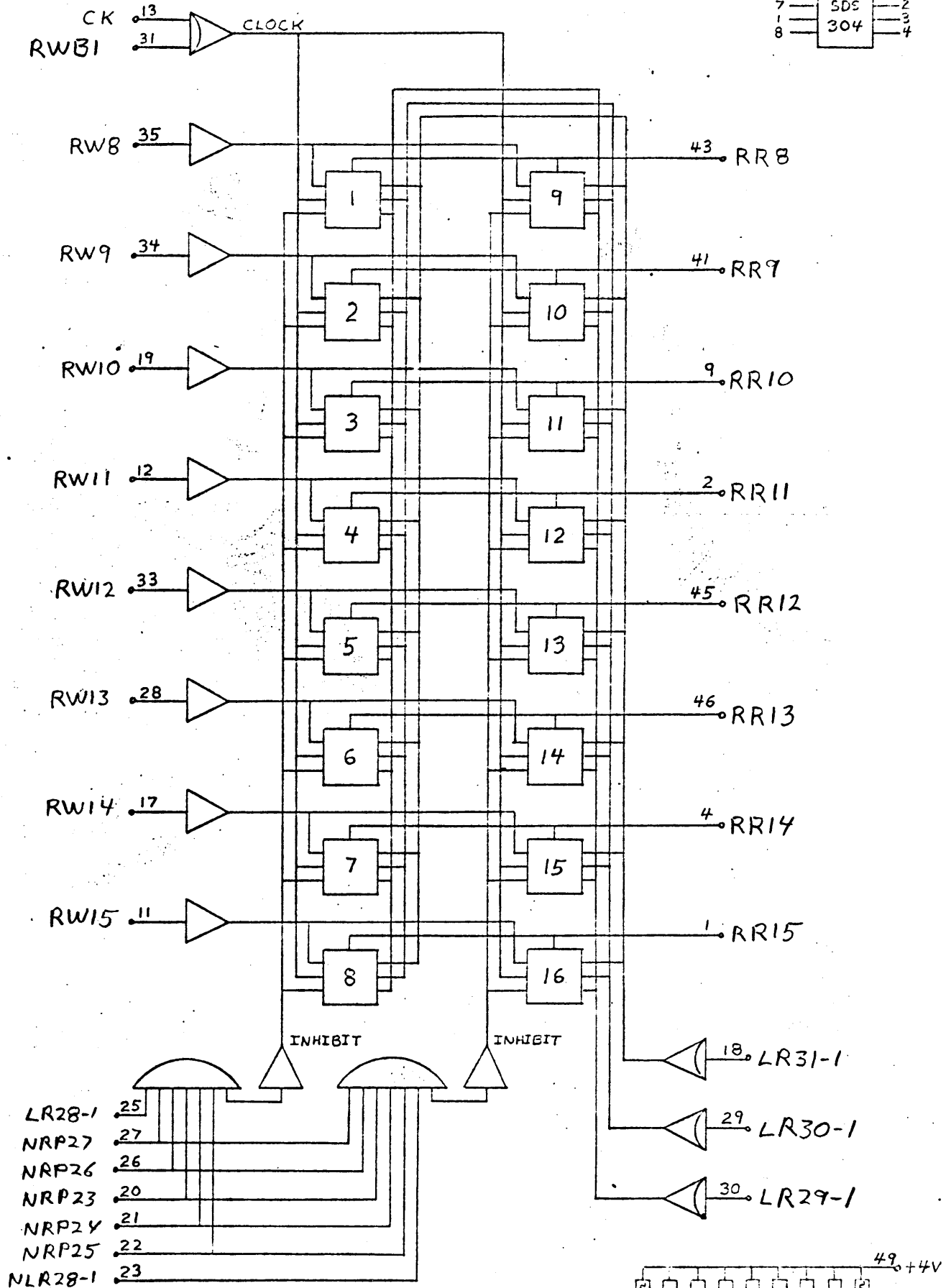
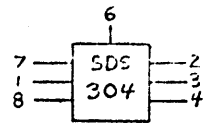




Σ7 REGISTER OIT RRO-RR7

FT25

15T

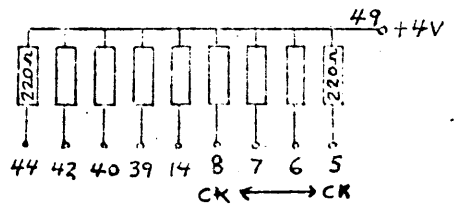


- LR28-1 25
- NRP27 27
- NRP26 26
- NRP23 20
- NRP24 21
- NRP25 22
- NLR28-1 23

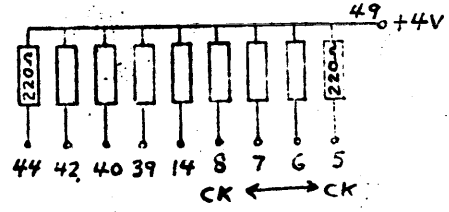
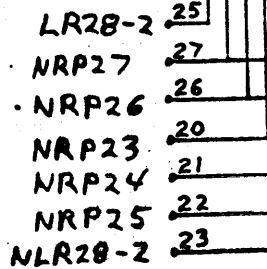
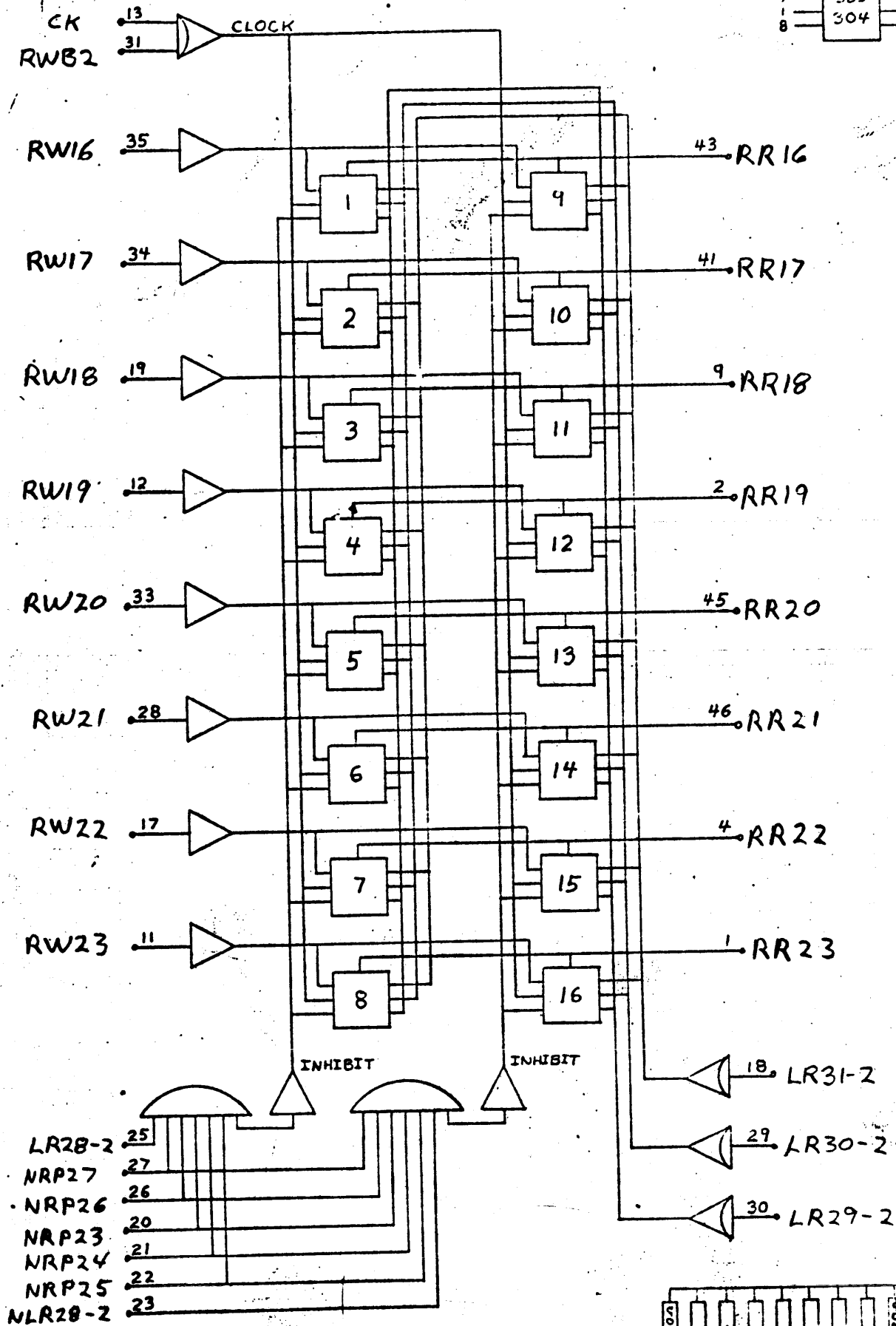
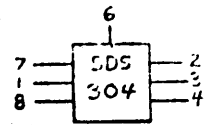
Σ7

REGISTER

15T RR8-RR15



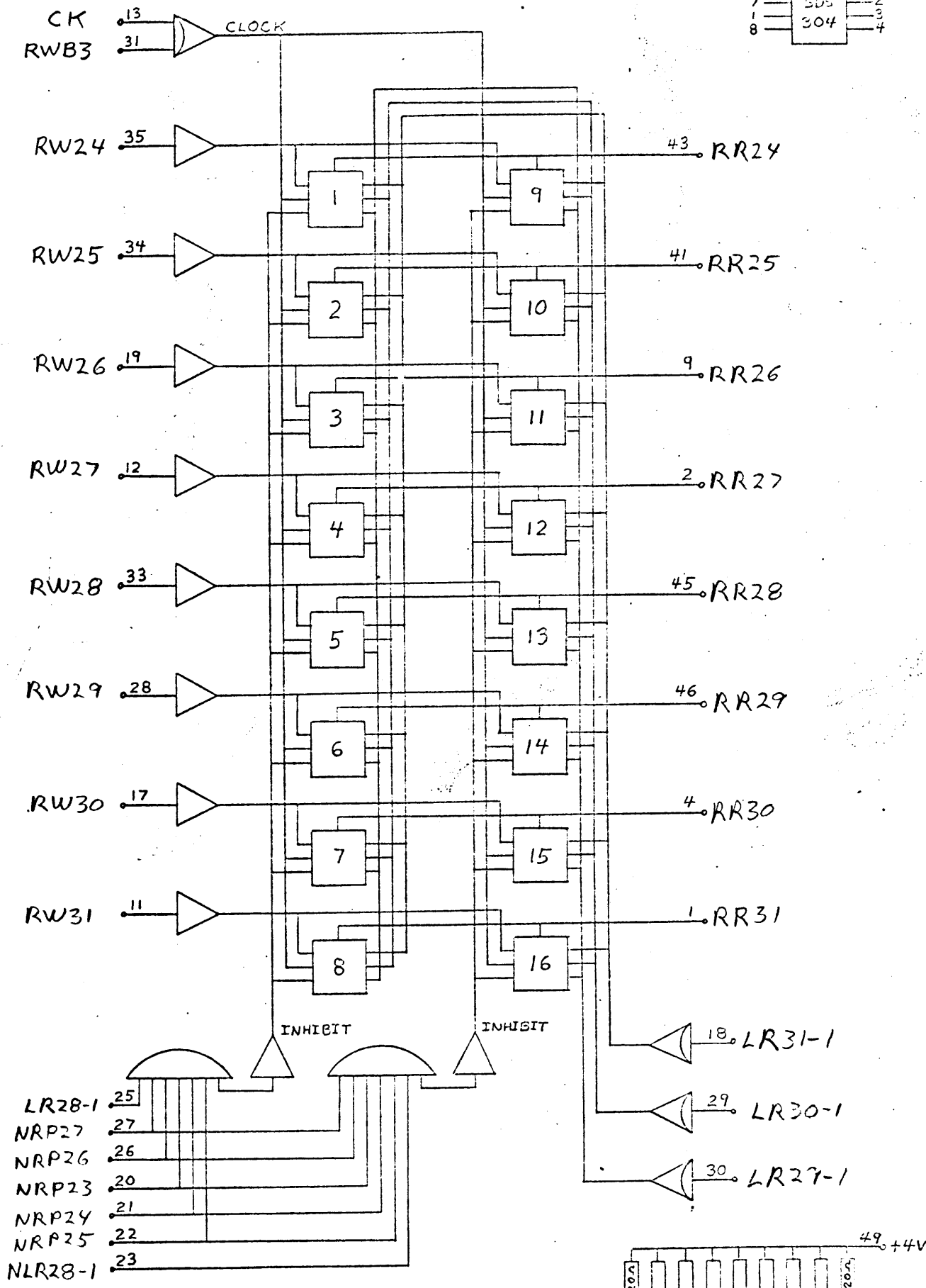
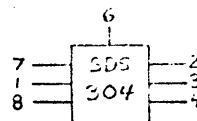
FT25 OIL



Σ7 REGISTER OIL RR16-RR23
Page 2-10

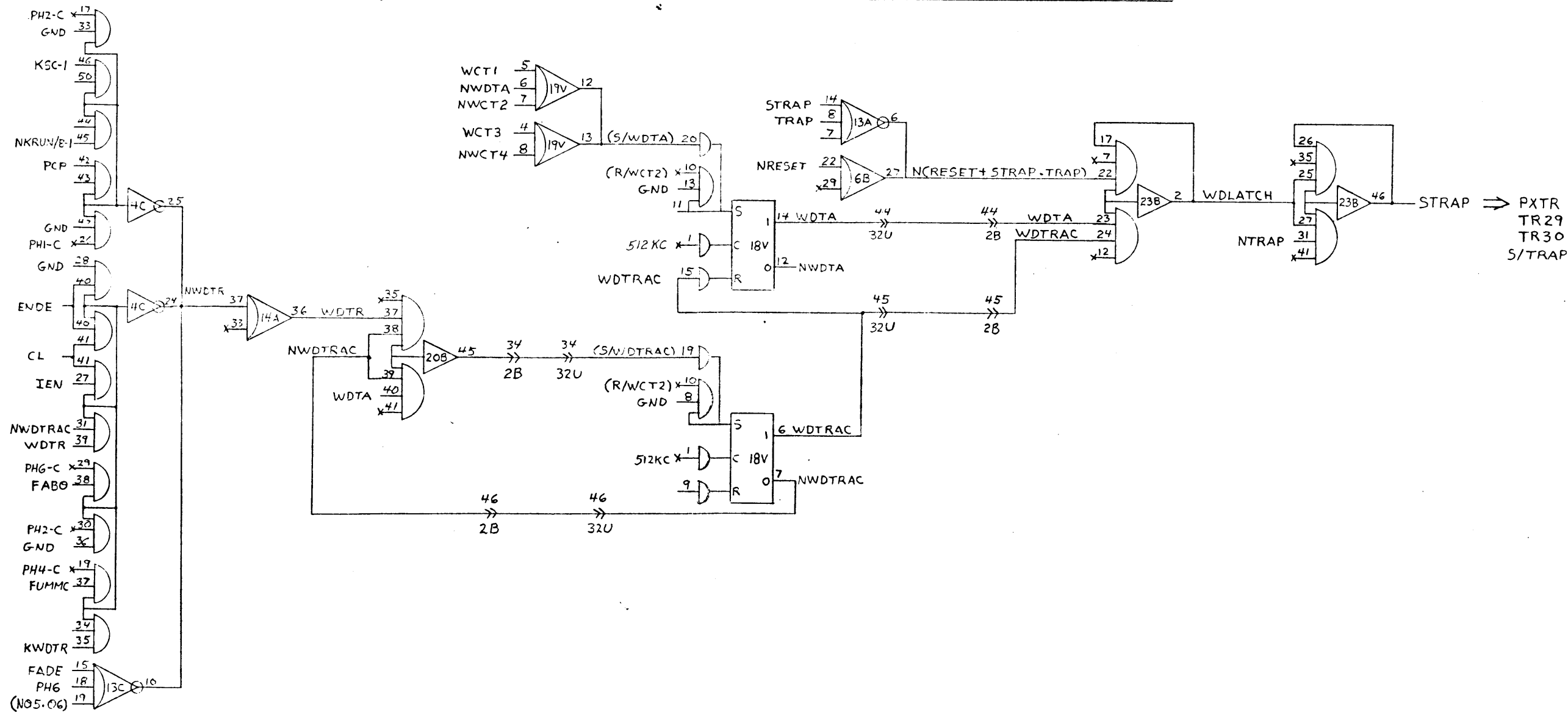
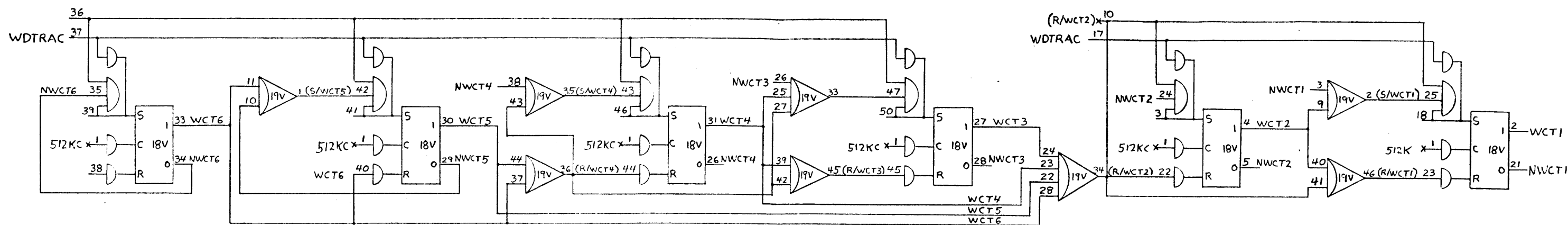
FT25

01Q

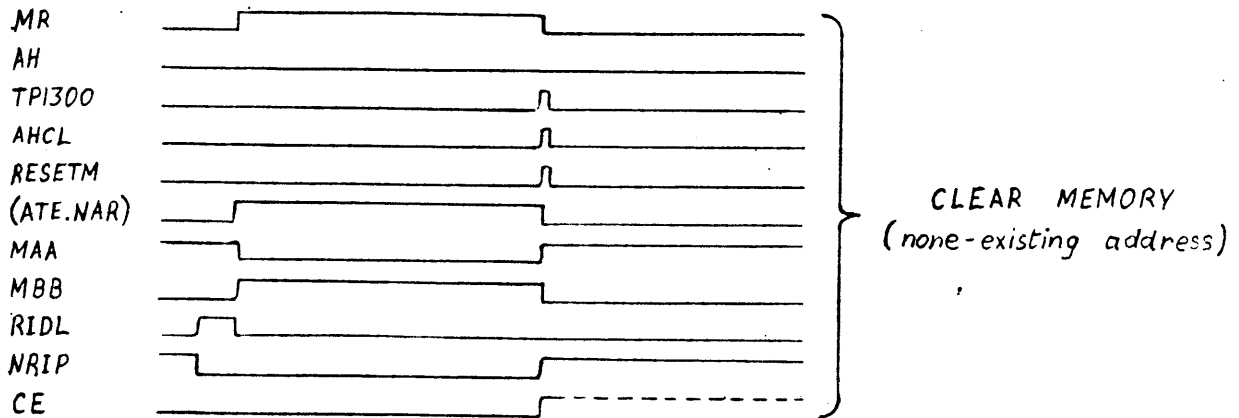
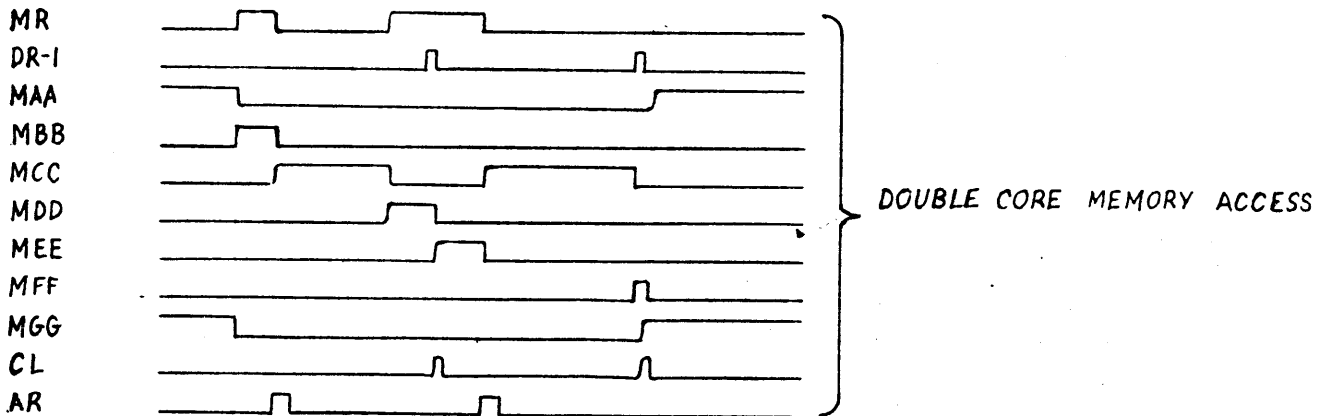
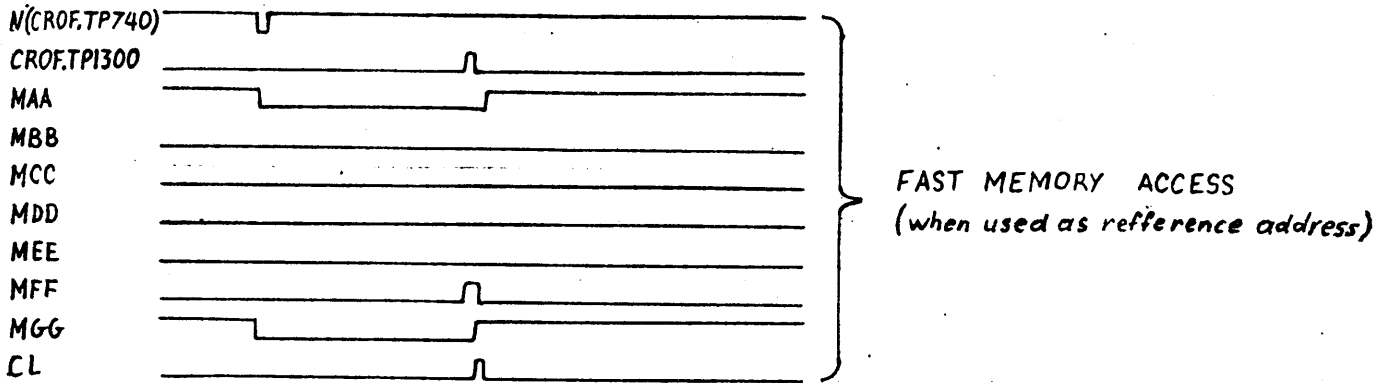
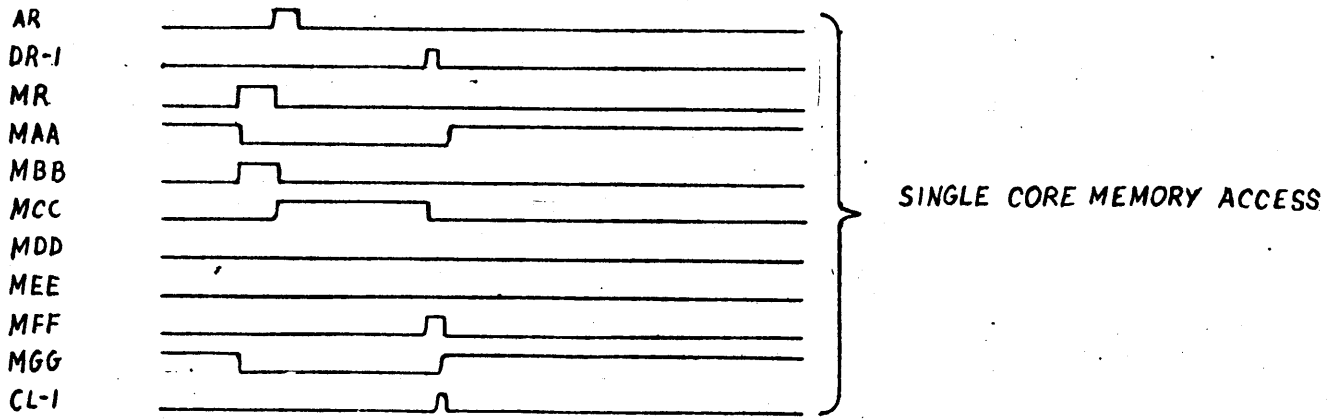


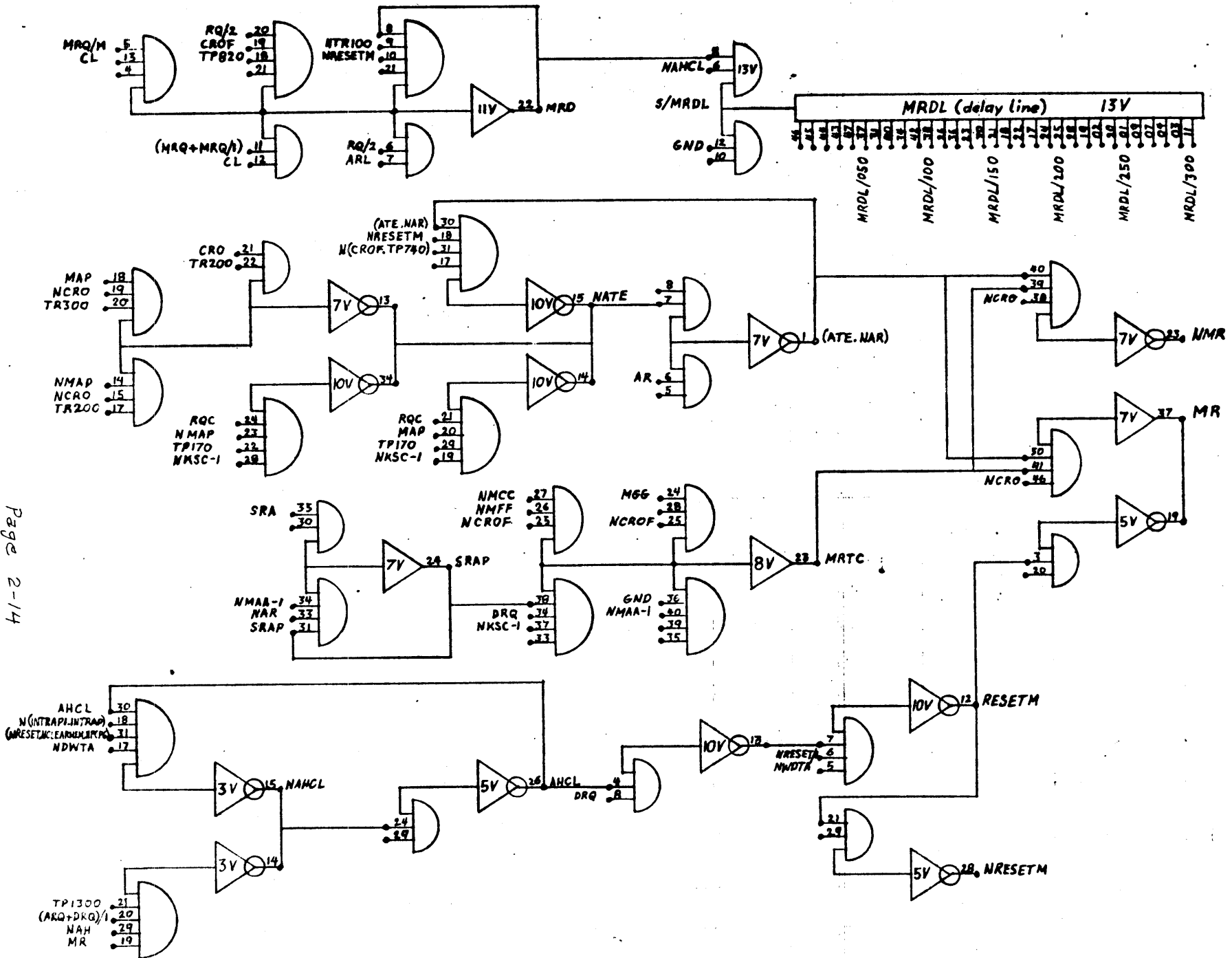
Σ7
REGISTER (01Q RR24-RR31)

Σ7 WATCHDOG TIMER TRAP (46)

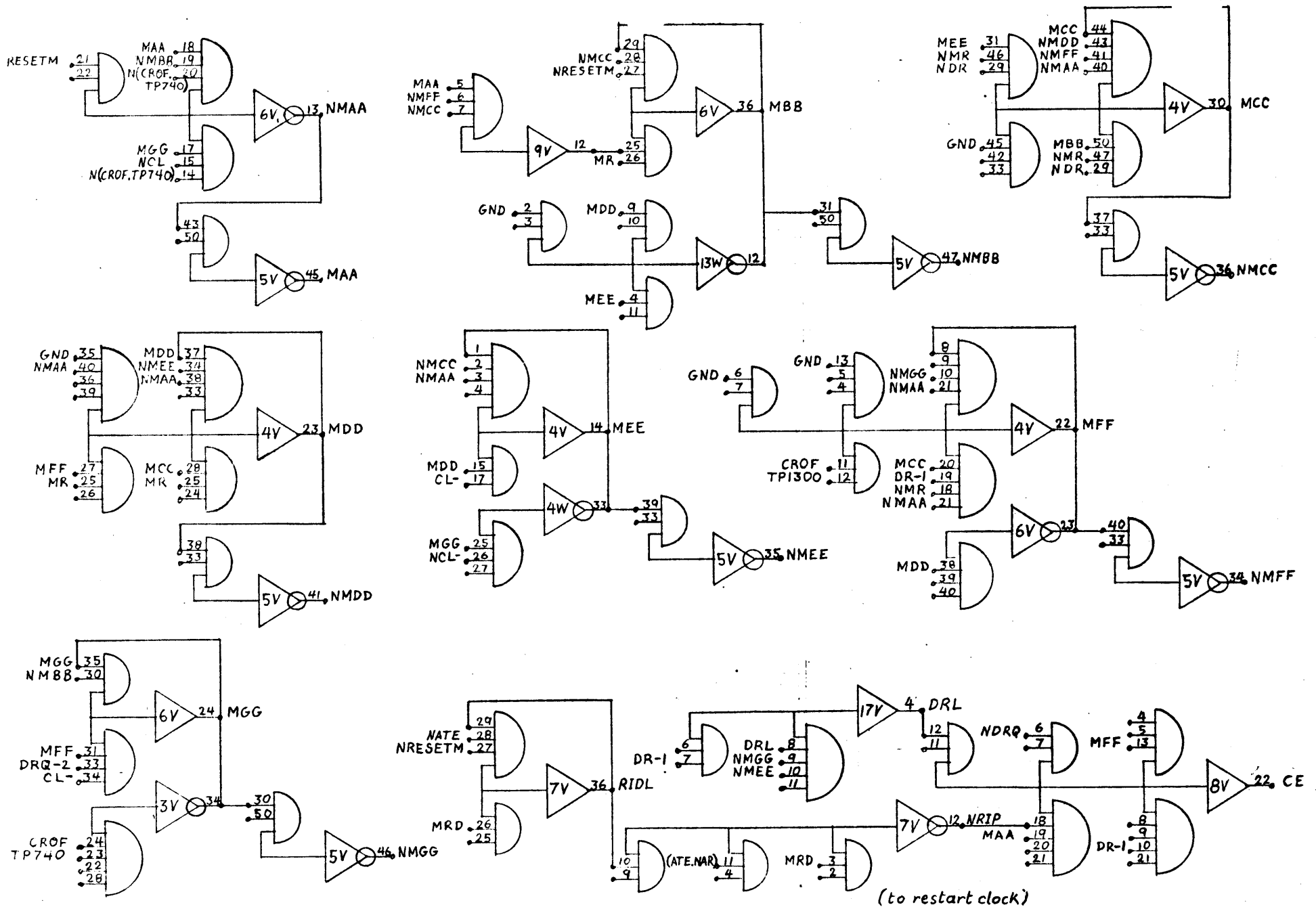


{7 MEMORY CYCLE CONTROL





7 MEMORY REQUEST



MEMORY CYCLE CONTROL

FAMILY TERMS

<u>SIGNAL NAME</u>	<u>TEST POINT</u>	<u>SIGNAL NAME</u>	<u>TEST POINT</u>
FABC	31J47	FAS4	
FABO	24J45	FAS5	
FABO/1	24J02	FAS6	32J46
FABO/2	24J46	FAS7	23J02
FABOA	24J35	FAS8	23J01
FABOA/1	30H02	FAS9	27H30
FABOA/2	22J01	FAS10	32J01
FABOX	23J47	FAS11	27H14
FABR	30Q15	FAS12	27H22
NFA BRANCH	25H01	FAS13	27J35
FABS	28H44	FAS14	23J03
FABSA	28H25	FAS15	23J44
FACAL	22J02	FAS16	23J45
FACV	22J13	FAS17	23J04
FADE	32J04	FAS18	25H46
FADIO	30H13	FAS19	30J46
FADIV	20J45	FAS21	20J04
FADIVH	6H36	FAS22	29H14
FADIVW	3J33	FAS23	29H30
FADW	32J45	FAS24	29H22
FAFL	25J13	FAS25	
FAFLM	25J46	FAS26	21J13
FAFLMD	25J02	FAST/1	26H30
FAFLAS	25J35	FAST	27J02
FAFRR	27Q17	FASTA	24J01
FAFRR/1	24H35	FATR	28H47
FAILL	28H15	FAW	29H23
FAIM	27J01	FUANLZ	31J41
FAIO	25H31	FUBAL	31J46
FAIO/1	22J35	FUCS	31J36
FAMDSF	16Q27	FUCVS	21J36
FAMDSE/D	20J03	FUEBS	20H11
FAMDSF/M	24H36	FUEBSA	28H28
FAMUL	19J46	FUEBS8	31J18
FAMULH	25J46	FUEBS9	31J19
FAMULI	26J01	FUEBS14	31J05
FAMULNH	26J35	FUEXU	31J45
FAMULW		FULAD	31J25
FANIMP	26H23	FULCD	31J27
FAPRIV	27J13	FULD	31J01
FAPSD	26J02	FULS	31J35
FARWD	28H05	FULRP	27J46
FASH	23H13	FUMMC	31J44
FASHFL	23H46	FUMTH	21J02
FASHFX	23H02	FUSID	31J26
FATR	28H47	FUSTH	21J46
FATRA	28H27	FUSTS	31J34
FATR5	24J13	FUWAIT	21J35
FAS1	30J35	FAFLD	25J45
FAS2	32J03	FUAD	28G46
FAS3	31J28	FUAND	
		FUAWM	28G45

PHASES

Register	FF	NFF	S/FF	R/FF	C/FF	FF/L
PCPI	20A31	26	46	44	1	17B
2	20A30	29	41	40	1	
3	20A33	34	39	38	1	
4	20A02	21	18	23	1	
5	20A04	5	3	22	1	
6	20A14	12	11	15	1	
7	20A06	7	\$	9	1	
PRE1	07F27	28	50	.	1	17B
2	07F31	26	46	.	1	
3	07F30	29	41	.	1	
4	07F33	34	39	.	1	
PH1	27A27	28	50	.	1	17B
2	27A31	26	46	.	1	17B
3	27A30	29	41	.	1	
4	27A33	34	39	.	1	17B
5	27A02	21	18	.	1	
6	27A04	5	3	.	1	
7	27A14	12	11	.	1	
8	27A06	7	\$.	1	17B
9	26A27	28	50	.	1	
10	26A31	26	46	.	1	
11	26A30	29	41	.	1	
12	26A06	7	\$.	1	
13	26A02	21	18	.	1	
14	26A04	5	3	.	1	
15	26A14	12	11	.	1	
PHA	26A33	34	39	38	1	

A- REGISTER

<u>REGISTER</u>	<u>FF</u>	<u>NFF</u>	<u>S/FF</u>	<u>R/FF</u>	<u>C/FF</u>
AO	05S23	25	12	2	1
1	05S19	21	28		1
2	05S31	29	37		1
3	05S27	22	35		1
4	06S23	25	12		1
5	06S19	21	28		1
6	06S31	29	37		1
7	06S27	22	35		1
8	19S23	25	12		1
9	19S19	21	28		1
10	19S31	29	37		1
11	19S27	22	35		1
12	20S23	25	12		1
13	20S19	21	28		1
14	20S31	29	37		1
15	12L23	22	35		1
16	12L23	25	12		1
17	12L31	21	28		1
18	12L31	29	37		1
19	12L27	22	35		1
20	13L23	25	12		1
21	13L19	21	28		1
A22	13L31	22	37		1
23	13L27	22	35		1
24	3N23	25	12		1
25	3N19	21	28	2	1
26	3N31	29	37		
27	3N27	22	35		
28	4N23	25	12		
29	4N19	21	28		
30	4N31	29	37		
31	4N27	22	35		
47	8N4	5	3		
48	22T23	25	12		
49	22T19	21	28		
50	22T31	29	37		
51	22T27	22	35		
52	23T23	25	12		
53	23T19	21	28		
54	23T31	29	37		
55	23T27	22	35		
56	12K23	25	12		
57	12K19	21	28		
58	12K31	29	37		
59	12K27	22	35		
A60	13K23	25	12		
61	13K19	21	28		
62	13K31	29	37		
63	13K27	22	35		
64	9L23	25	12		
65	9L19	21	28		
66	9L31	29	37		
67	9L27	22	35		
68	10L23	25	12		
69	10L19	21	28		
70	10L31	29	37		
71	10L27	22	35		

ADDER (PR)

Signal	Test Point	Signal	Test Point
PR0	5R17	PR29	5P31
PR1	5R31	PR30	6P17
PR2	6R17	PR31	6P31
PR3	6R31	PR32	19Q31
PR4	8R17	PR47	25Q31
PR5	8R31	PR48	24R17
PR6	9R17	PR49	24R31
PR7	9R31	PR50	25R17
PR8	15R17	PR51	25R31
PR9	15R31	PR52	26R17
PR10	16R17	PR53	26R31
PR11	16R31	PR54	27R17
PR12	17R17	PR55	27R31
PR13	17R31	PR56	20M17
PR14	19R17	PR57	20M31
PR15	19R31	PR58	21M17
PR16	12M17	PR59	21M31
PR17	12M31	PR60	23M17
PR18	13M17	PR61	23M31
PR19	13M31	PR62	24M17
PR20	15M17	PR63	24M31
PR21	15M31	PR64	5M17
PR22	16M17	PR65	5M31
PR23	16M31	PR66	6M17
PR24	3P17	PR67	6M31
PR25	3P31	PR68	8M17
PR26	4P17	PR69	8M31
PR27	4P31	PR70	9M17
PR28	5P17	PR71	9M31

ADDER (G)

Signal	Test Point	Signal	Test Point	Signal	Test Point
G0	5R19	G22	16M19	G59	21M29
G1	5R29	G23	16M29	G60	23M19
G2	6R19	G24	3P19	G61	23M29
G3	6R29	G25	3P29	G62	24M19
G4	8R19	G26	4P19	G63	24M29
G5	8R29	G27	4P29	G64	5M19
G6	9R19	G28	5P19	G65	5M29
G7	9R29	G29	5P29	G66	6M19
G8	15R19	G30	6P19	G67	6M29
G9	15R29	G31	6P29	G68	8M19
G10	16R19	G47	25Q29	G69	8M29
G11	16R29	G48	24R19	G70	9M19
G12	17R19	G49	24R29	G71	9M29
G13	17R29	G50	25R19		
G14	19R19	G51	25R29		
G15	19R29	G52	26R19		
G16	12M19	G53	26R29		
G17	12M29	G54	27R19		
G18	13M19	G55	27R29		
G19	13M29	G56	20M19		
G20	15M19	G57	20M29		
G21	15M29	G58	21M19		

ADDER (K)

Signal	Test Point	Signal	Test Point	Signal	Test Point
K0	9T26	K21	10K18	K57	9K27
K1	19T27	K22	10K20	K58	9K25
K2	9T25	K23	9N18	K59	13N19
K3	9N26	K24	10N26	K60	9K19
K4	9T19	K25	10N27	K61	9K18
K5	9T18	K26	10N25	K62	9K20
K6	9T20	K27	9N20	K63	13N18
K7	9N27	K28	10N19	K64	8K26
K8	10T26	K29	10N18	K65	8K27
K9	10T27	K30	10N20	K66	8K25
K10	10T25	K31	9N24	K67	13N20
K11	9N25	K47	13N26	K68	8K19
K12	10T19	K48	20T26	K69	8K18
K13	10T18	K49	20T27	K70	8K20
K14	10T20	K50	20T25		
K15	9N17	K51	13N27		
K16	10K26	K52	20T19		
K17	10K27	K53	20T18		
K18	10K25	K54	20T20		
K19	9N19	K55	13N25		
K20	10K19	K56	9K26		

B-REGISTER

<u>REGISTER</u>	<u>FF</u>	<u>NFF</u>	<u>S/FF</u>	<u>R/FF</u>	<u>C/FF</u>
B0	2S23	25	12	2	1
B1	2S19	21	28		
B2	2S31	29	37		
B3	2S27	22	35		
B4	3S23	25	12		
B5	3S19	21	28		
B6	3S31	29	37		
B7	3S27	22	35		
B8	24S23	25	12		
B9	24S19	21	28		
B10	24S31	29	37		
B11	24S27	22	35		
B12	25S23	25	12		
B13	25S19	21	28		
B14	25S31	29	37		
B15	25S27	22	35		
B16	15L23	25	12		
B17	15L19	21	28		
B18	15L31	29	37		
B19	15L27	22	35		
B20	16L23	25	12		
B21	16L19	21	28		
B22	16L31	29	37		
B23	16L37	22	35		
B24	1N23	25	12		
B25	1N19	21	28		
B26	1N31	29	37		
B27	1N27	22	35		
B28	2N23	25	12		
B29	2N19	21	28		
B30	2N31	29	37		
B31	2N27	22	35		
B47	8N14	12	11	15	
B48	24T23	25	12	2	
B49	24T19	21	28		
B50	24T31	29	37		
B51	24T27	22	35		
B52	25T23	25	12		
B53	25T19	21	28		
B54	25T31	29	37		
B55	25T27	22	35		
B56	14K23	25	12		
B57	14K19	21	28		
B58	14K31	29	37	2	1
B59	14K27	22	35		
B60	15K23	25	12		
B61	15K19	21	28		
B62	15K31	29	37		
B63	15K27	22	35		
B64	1K23	25	12		
B65	1K19	21	28		
B66	1K31	29	37		
B67	1K27	22	35		
B68	2K23	25	12		
B69	2K19	21	28		
B70	2K31	29	37		
B71	2K27	22	35		

C-REGISTER

<u>REGISTER</u>	<u>FF</u>	<u>NFF</u>
	C	NC
CO	5R18	5R10
1	5R28	36
2	6R18	10
3	6R28	36
4	8R18	10
5	8R28	36
6	9R18	10
7	9R28	36
8	15R18	10
9	15R28	36
10	16R18	10
11	16R28	36
12	17R18	10
13	17R28	36
14	19R18	10
15	19R28	36
16	12M18	10
17	12M28	36
18	13M18	10
19	13M28	36
20	15M18	10
21	15M28	36
22	16M18	10
23	16M28	36
24	3P18	10
25	3P28	36
26	4P18	10
C27	4P28	36
28	5P18	10
29	5P28	36
30	6P18	10
31	6P28	36

CS-REGISTER

<u>REGISTER</u>	<u>FF</u>	<u>N/FF</u>	<u>S/FF</u>	<u>R/FF</u>
CS0	7S27	28	50	
1	7S31	26	46	
2	7S30	29	41	40
3	7S33	34	39	38
4	7S02	21	18	23
5	7S04	5	3	22
6	7S06	7	\$	9
7	7S14	12	11	15
8	1R27	28	50	45
9	1R31	26	46	44
10	1R30	29	41	40
11	1R33	34	39	38
12	1R02	21	18	23
13	1R04	5	3	22
14	1R06	7	\$	9
15	1R14	12	11	15
16	17K27	28	50	45
17	17K31	26	46	44
18	17K30	29	41	40
19	17K33	34	39	38
20	17K02	21	18	23
21	17K04	5	3	22
22	17K14	12	11	15
23	17K06	7	\$	9
24	9Q27	28	50	45
25	9Q31	26	46	44
26	9Q30	29	41	40
27	9Q33	34	39	38
28	9Q02	21	18	23
CS29	9Q04	5	3	22
30	9A06	7	\$	9
31	9Q14	12	11	15
32	8P02	21	18	23
47	8P06	7	\$	9
48	30T27	28	50	45
49	30T31	26	46	44
50	30T30	29	41	40
51	30T33	34	39	38
52	30T02	21	18	23
53	30T04	5	3	22
54	30T14	12	11	15
55	30T06	7	\$	9
56	15K27	28	50	45
57	16K31	26	46	44
58	16K30	29	41	40
59	16K33	34	39	38
60	16K02	21	18	23
61	16K04	5	3	22
62	16K14	12	11	15
63	16K06	7	\$	9
64	4K27	28	50	45
65	4K31	26	46	44
66	4K30	29	41	40
67	4K33	34	39	38
68	4K02	21	18	23
69	4K04	5	3	22
70	4K14	12	11	15
71	4K06	7	\$	9

D-REGISTER

<u>REGISTER</u>	<u>FF</u>	<u>NFF</u>	<u>S/FF</u>	<u>R/FF</u>	<u>C/FF</u>
D0	3R23	25	12	2	1
D1	3R19	21	28		
D2	3R31	29	37		
D3	3R27	22	35		
D4	4R23	25	12		
D5	4R19	21	28		
D6	4R31	29	37		
D7	4R27	22	35		
D8	21R23	25	12		
D9	21R19	21	28		
D10	21R31	29	37		
D11	21R27	22	35		
D12	22R23	25	12		
D13	22R19	21	28		
D14	22R31	29	37		
D15	22R27	22	35		
D16	14P23	25	12		
D17	14P19	21	28		
D18	14P31	29	37		
D19	14P27	22	35		
D20	16P23	25	12		
D21	16P19	21	28		
D22	16P31	29	37	2	1
D23	16P27	22	35		
D24	9P23	25	12		
D25	9P19	21	28		
D26	9P31	29	37		
D27	9P27	22	35		
D28	11P23	25	12		
D29	11P19	21	28		
D30	11P31	29	37		
D31	11P27	22	35		
D47	8P31	26	46	44	
D48	26T23	25	12	2	
D49	26T19	21	28		
D50	26T31	29	37		
D51	26T27	22	35		
D52	22T23	25	12		
D53	27T19	21	28		
D54	27T31	29	37		
D55	27T27	22	35		
D56	18L23	25	12		
D57	18L19	21	28		
D58	18L31	29	37		
D59	18L27	22	35		
D60	19L23	25	12		
D61	19L19	21	28		
D62	19L31	29	37		
D63	19L27	22	35		
D64	5K23	25	12		
D65	5K19	21	28		
D66	5K31	29	37		
D67	5K27	22	35		
D68	6K23	25	12		
D69	6K19	21	28		
D70	6K31	22	35		
D71	6K27	22	35		

E-REGISTER

<u>REGISTER</u>	<u>FF</u>	<u>NFF</u>	<u>S/FF</u>	<u>R/FF</u>	<u>C/FF</u>
E0	14S33	40	36	30	1
E1	14S25	26	31	24	
E2	14S19	21	20	17	
E3	14S05	22	12	3	
E4	15S33	40	36	30	
E5	15S25	26	31	24	
E6	15S19	21	20	17	
E7	15S05	22	12	3	

KNC DATA SWITCH

<u>SIGNAL</u>	<u>TEST POINT</u>
KNC0	29R1
KNC1	29R07
KNC2	29R23
KNC3	29R24
KNC4	29R47
KNC5	29R42
KNC6	29R09
KNC7	29R40
KNC8	29R08
KNC9	29R43
KNC10	29R46
KNC11	29R45
KNC12	28P01
KNC13	28P07
KNC14	28P03
KNC15	28P44
KNC16	28P04
KNC17	28P02
KNC18	29P02
KNC19	29R04
KNC20	32L33
KNC21	32L34
KNC22	32L35
KNC23	32L36
KNC24	28P09
KNC25	28P40
KNC26	28P42
KNC27	28P47
KNC28	28P08
KNC29	28P45
KNC30	28P46
KNC31	28P43

KS DATA SWITCH

<u>SIGNAL</u>	<u>TEST POINT</u>
KS0	26S1
KS1	26S01
KS2	26S03
KS3	26S04
KS4	26S07
KS5	26S08
KS6	26S09
KS7	26S40
KS8	26S42
KS9	26S43
KS10	26S44
KS11	26S45
KS12	26S46
KS13	26S47
KS14	26S46
KS15	32L29
KS16	17N40
KS17	17N46
KS18	17N47
KS19	26K43
KS20	26K45
KS21	26K46
KS22	29M02
KS23	29M04
KS24	17N01
KS25	17N02
KS26	17N03
KS27	17N04
KS28	17N07
KS29	17N08
KS30	32L30
KS31	32L31

KSP ADDRESS SELECT SWITCH

<u>SIGNAL</u>	<u>TEST POINT</u>
KSP15	26K01
KSP16	26K03
KSP17	26K07
KSP18	26K09
KSP19	26K40
KSP20	26K42
KSP21	26K44
KSP22	26K47
KSP23	29M01
KSP24	29M03
KSP25	29M07
KSP26	29M09
KSP27	29M40
KSP28	29M42
KSP29	29M44
KSP30	29M47
KSP31	17N44

KUA UNIT ADDRESS SWITCH

SIGNAL

TEST POINT

KUA21	29M08
KUA22	29M43
KUA23	29M45
KUA24	29M46
KUA25	17M09
KUA26	26K02
KUA27	17N42
KUA28	17N43
KUA29	17N45
KUA30	26K04
KUA31	26K08

O-REGISTER

Register	FF	NFF	S/FF	R/FF	C/FF
O1	8Q02	21	18	23	1
2	8Q27	28	50	45	1
3	8Q31	26	46	44	1
4	8Q30	29	41	40	1
5	8Q04	5	3	22	1
6	8Q33	34	39	38	1
7	8Q06	7	\$	9	1

P-REGISTER

Register	FF	NFF	S/FF	R/FF	C/FF
P15	18K33	40	36	30	1
16	18K25	26	31	24	1
17	18K19	21	20	17	1
18	18K05	22	12	3	1
19	19K33	40	36	30	1
20	19K25	26	31	24	1
21	19K19	21	20	17	1
22	19K05	22	12	3	1
23	22L25	26	31	24	1
24	22L19	21	20	17	1
25	22L05	22	12	3	1
26	23L33	40	36	30	1
27	23L25	26	31	24	1
28	23L19	21	20	17	1
29	23L05	22	12	3	1
30	25L33	40	36	30	1
31	25L25	26	31	24	1
32	25L19	21	20	17	1
33	25L05	22	12	3	1

Q-Register Test Point List

Register	FF	NFF	S/FF	R/FF	C/FF	FF/L
Q15	23K27	28	50	45	1	26K
16	23K31	26	46	44	1	26K
17	23K30	29	41	40	1	26K
18	23K33	34	39	38	1	26K
19	23K2	21	18	23	1	26K
20	23K4	5	3	2	1	26K
21	23K14	12	11	15	1	26K
22	23K6	7	\$	9	1	26K
23	24K27	28	50	45	1	26K
24	24K31	26	46	44	1	26K
25	24K30	29	41	40	1	26K
26	24K2	21	18	23	1	26K
27	24K6	7	\$	9	1	26K
28	24K33	34	39	38	1	26K
29	24K4	5	3	2	1	29M
30	24K14	12	11	15	1	
31	20L27	28	50	45	1	

FAST MEMORY

<u>REG.</u>	<u>RR</u>	<u>RW</u>	<u>HSM</u>	<u>HSM</u>	<u>HSM</u>	<u>HSM</u>
0	5T2	8S36	1T43	2T43	3T43	4T43
1	5T22	8S41	1T41	2T41	3T41	4T41
2	5T27	8S36	1T09	2T09	3T09	4T09
3	5T34	8S34	1T02	2T02	3T02	4T02
4	5T36	8S45	1T45	2T45	3T45	4T45
5	5T38	8S44	1T46	2T46	3T46	4T46
6	5T40	8S46	1T04	2T04	3T04	4T04
7	5T42	8S47	1T01	2T01	3T01	4T01
8	19T20	22S19	15T43	16T43	17T43	18T43
9	19T22	22S18	15T41	16T41	17T41	18T41
10	19T27	22S05	15T09	16T09	17T09	18T09
11	19T34	22S17	15T02	16T02	17T02	18T02
12	19T36	22S28	15T45	16T45	17T45	18T45
13	19T38	22S27	15T46	16T46	17T46	18T46
14	19T40	22S25	15T04	16T04	17T04	18T04
15	19T42	22S26	15T01	16T01	17T01	18T01
16	5L20	8L19	1L43	2L43	3L43	4L43
17	5L22	8L18	1L41	2L41	3L41	4L41
18	5L27	8L05	1L09	2L09	3L09	4L09
19	5L34	8L17	1L02	2L02	3L02	4L02
20	5L36	8L28	1L45	2L45	3L45	4L45
21	5L38	8L27	1L46	2L46	3L46	4L46
22	5L40	8L25	1L04	2L04	3L04	4L04
23	5L42	8L26	1L01	2L01	3L01	4L01
24	5Q20	6Q19	1Q43	2Q43	3Q43	4Q43
25	5Q22	6Q18	1Q41	2Q41	3Q41	4Q41
26	5Q27	6Q05	1Q09	2Q09	3Q09	4Q09
27	5Q34	6Q17	1Q02	2Q02	3Q02	4Q02
28	5Q36	6Q28	1Q45	2Q45	3Q45	4Q45
29	5Q38	6Q27	1Q46	2Q46	3Q46	4Q46
30	5Q40	6Q25	1Q04	2Q04	3Q04	4Q04
31	5Q42	6Q26	1Q01	2Q01	3Q01	4Q01

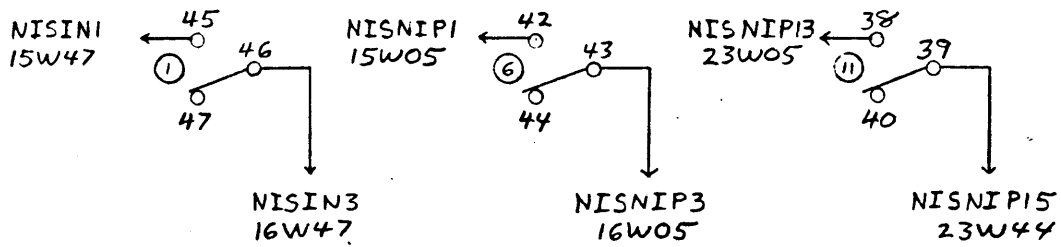
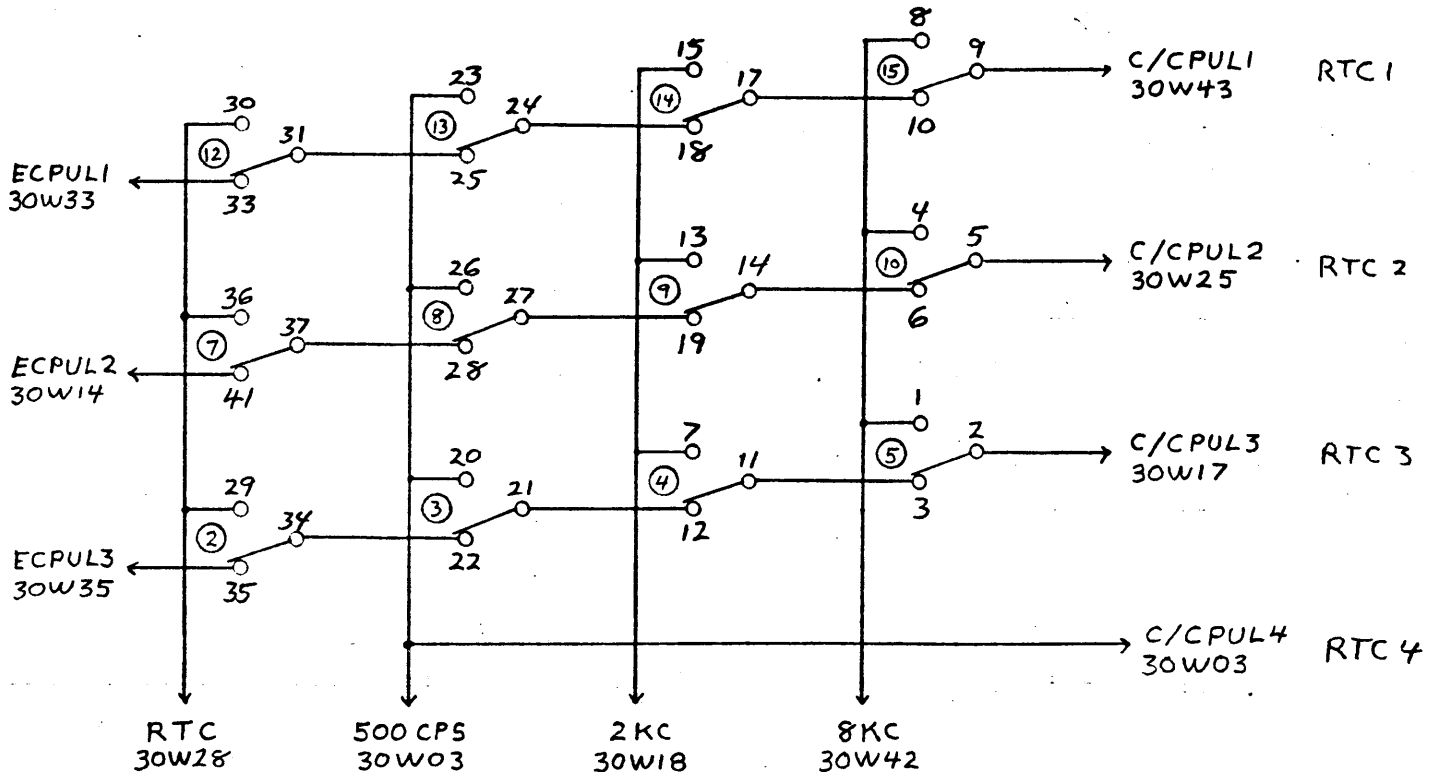
S-BUS

<u>NAME</u>	<u>S</u>
S0	5R15
1	5R33
2	6R15
3	6R33
4	8R15
5	8R33
6	9R15
7	9R33
8	15R15
9	15R33
10	16R15
11	16R33
12	17R15
13	17R33
14	19R15
15	19R33
16	12M15
17	12M33
18	13M15
19	13M33
20	15M15
21	15M33
22	16M15
23	16M33
24	3P15
25	3P33
26	4P15
27	4P33
28	5P15
29	5P33
30	6P15
31	6P33
47	25Q33
48	24R15
49	24R33
50	25R15
51	25R33
52	26R15
53	26R33
54	27R15
55	27R33
56	20M15
57	20M33
58	21M15
59	21M33
60	23M15
61	23M33
62	24M15
63	24M33
64	5M15
65	5M33
66	6M15
67	6M33
68	8M15
69	8M33
70	9M15
71	9M33

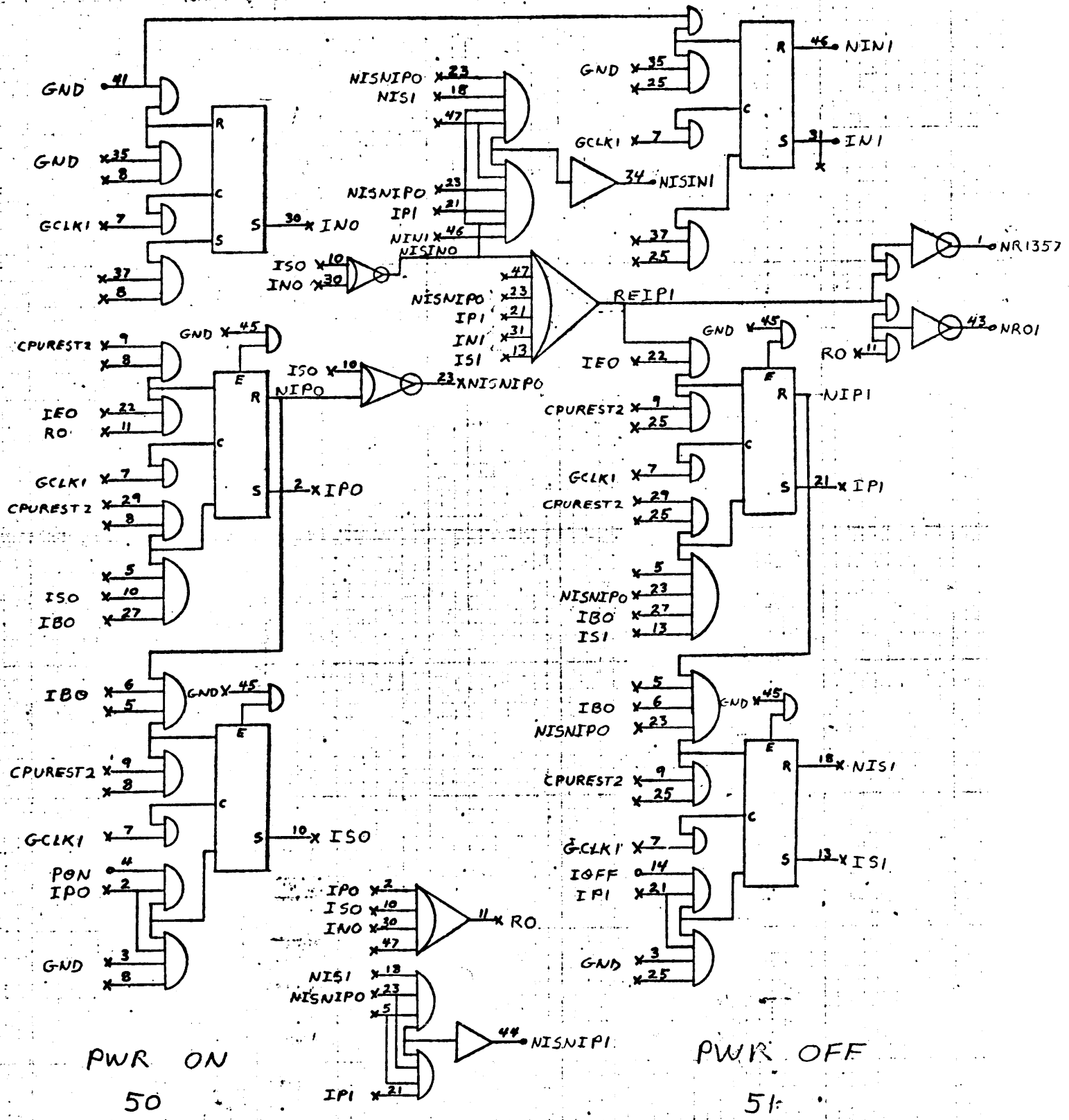
TRANSFER TERMS

INTERREGISTER

<u>FUNCTION</u>	<u>NAME</u>	<u>FRAME 1</u>	<u>NAME</u>	<u>FRAME 2</u>
O → A			NAX	31T35
E → A	NAXE	4J25		
PRR → A	NAXPRR	6J30		
R → A			AXR	16N18
RR → A			AXRR	10S25
S → A			AXS	22K26
O's → B			BXB	12T44
S → B			BXS	9S25
O's → CS			CSX1	29S06
O's → D			NDX	28S09
C → D			DXC	14T07
K → D			DXK	12T15
S → E	EXS	2J22		
S → MB	MBXS	2J23		
O's → O			OX	21N09
C → O			OXC	16Q06
S → PSW1	PSW1XS	22F24		
D → PSW2	PSW2XD	5H45		
1's → P	NPX/1	6A02		
2 → P	NPX/2	3A45		
20 → P			PX20	13A28
K → P			PXK	29K35
Q → P			RRWXS	22S10
S → P			PXS/1	29K45
P → Q			QXP-2	25K47
A → S			SXA	12Q26
ADD → S	NSXADD	19G15		
B → S			SXB	29S10
D → S			SXD	29T41
P → S			SXP	25K26
PR → S			SXPR	21T35

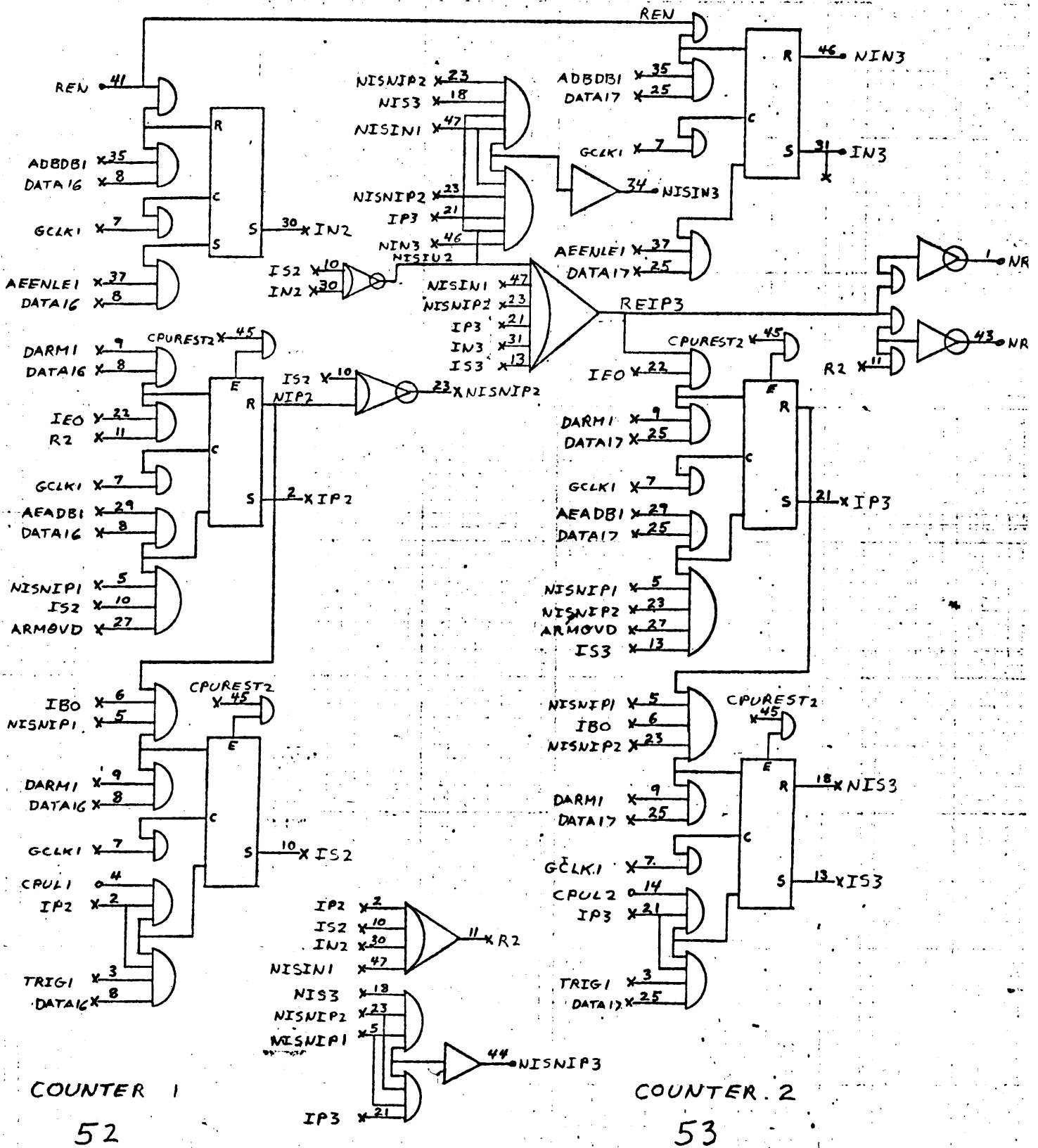


REAL TIME CLOCK MODULE (24W) ST14
Σ 7



PRIORITY INTERRUPT LT16

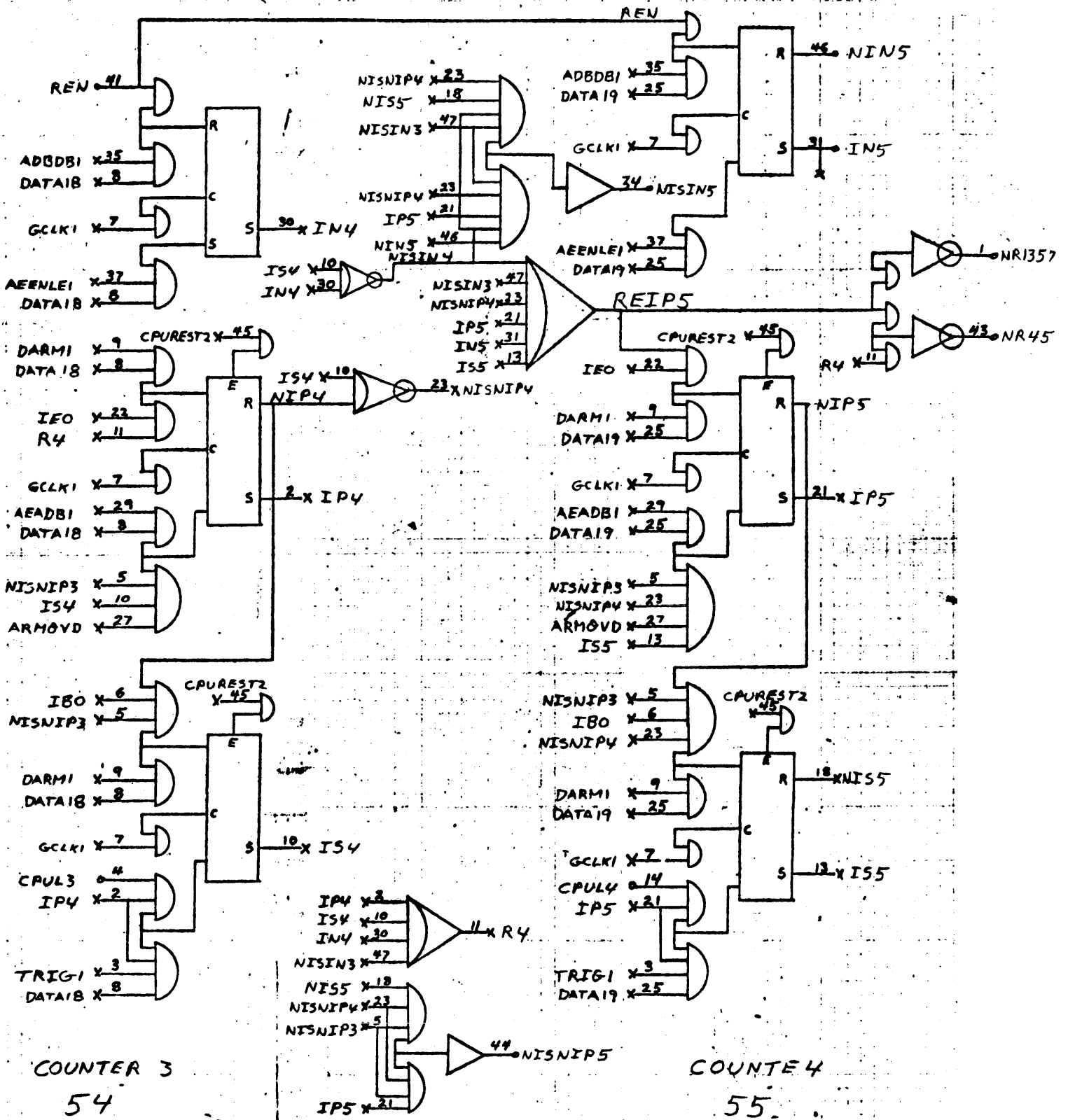
14W (OPTIONAL)
Σ7

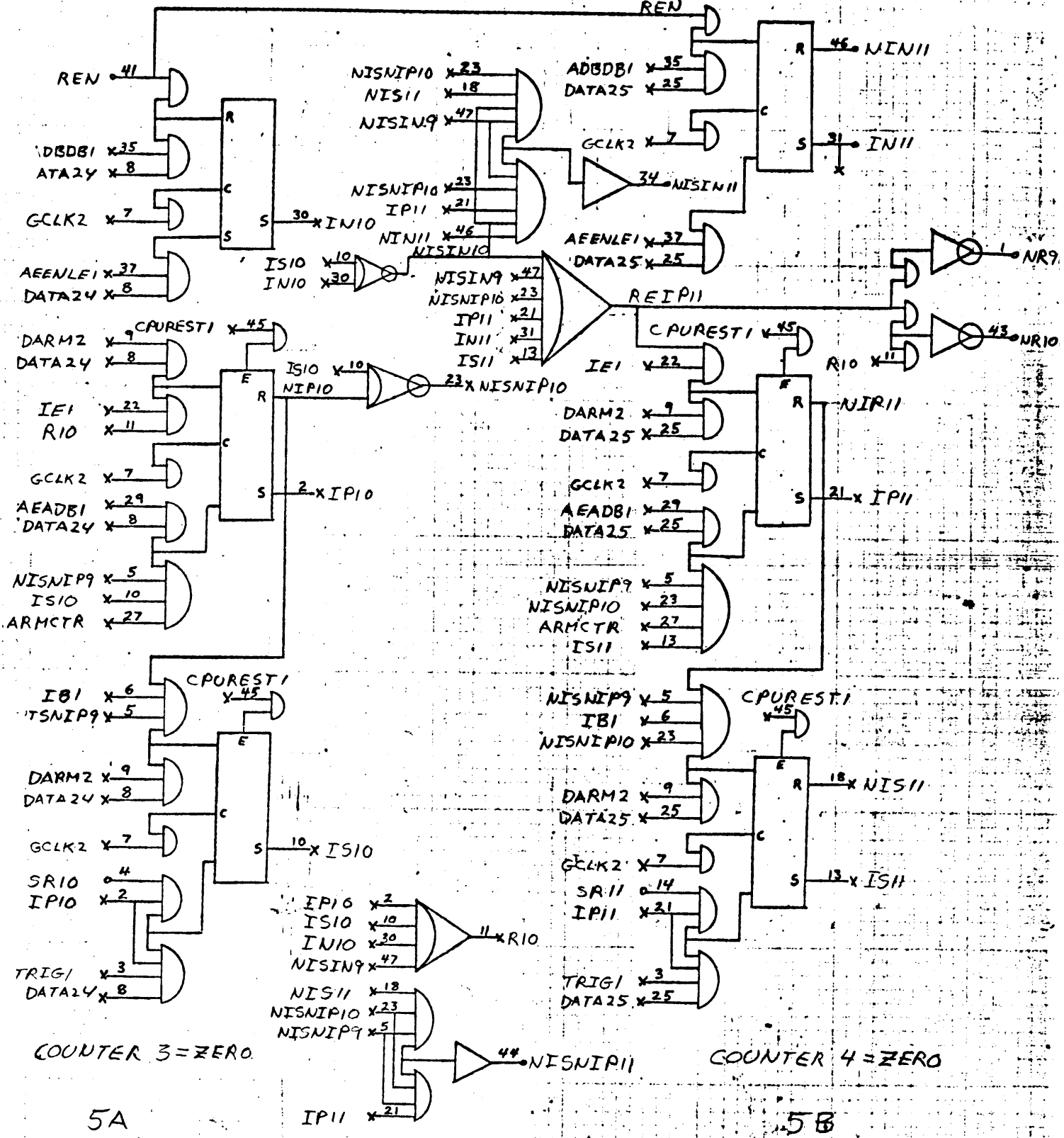


PRIORITY INTERRUPT LT16

15W (OPTIONAL)

Σ 7

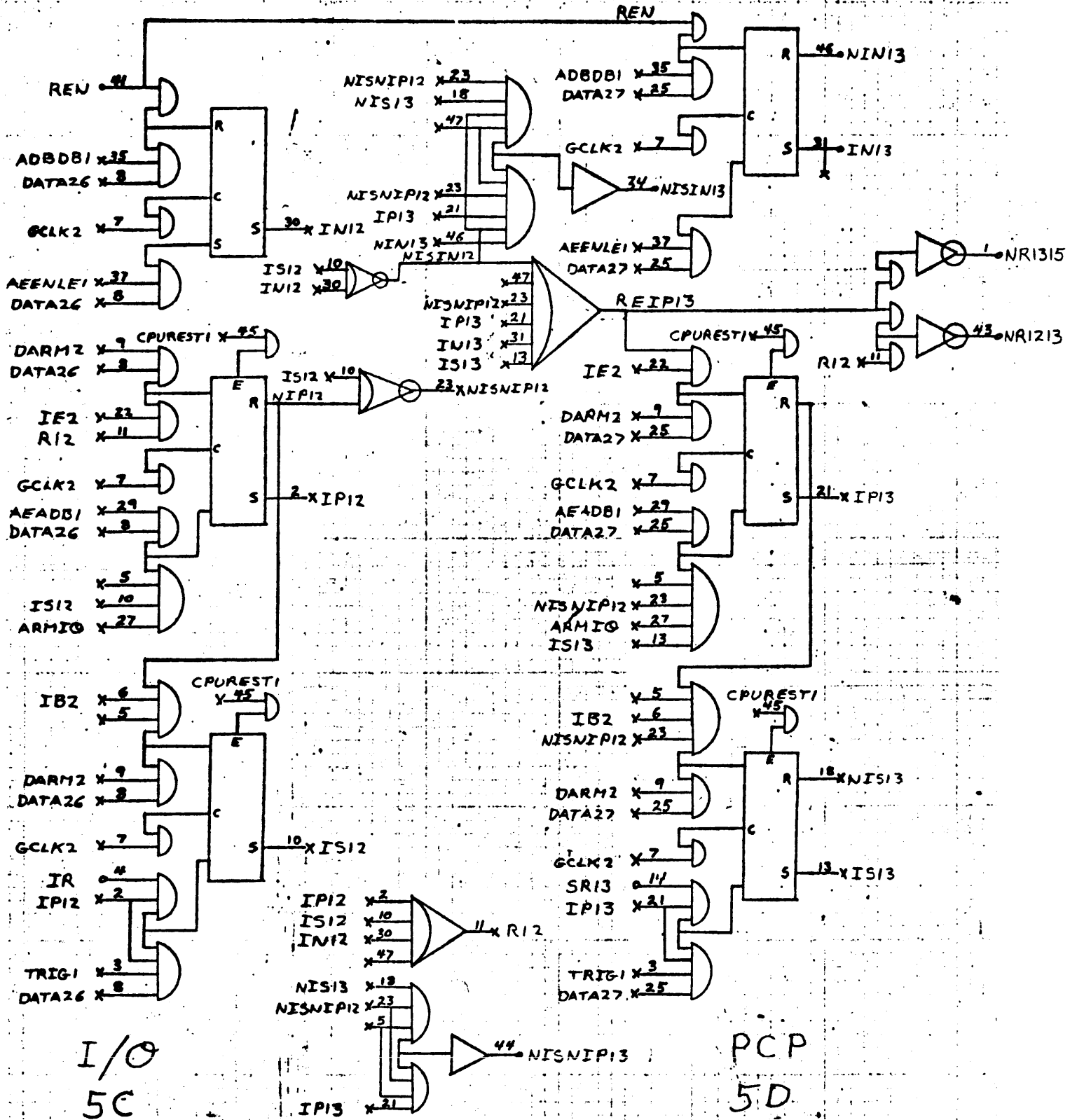




PRIORITY INTERRUPT LT16

21W

Σ7



PRIORITY INTERRUPT LT16

22W

Σ7

Σ 5/7 MEMORY 8251

(8251/7451)

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
A	XT 13 0-3	XT 13 4-7	XT 13 8-11	XT 13 12-15	XT 13 16-19 32	XT 14	XT 13 20-23 32	XT 13 24-27	XT 13 28-31	XT 13	XT 10	IT 25 NM22	LT 34	LT 34	LT 34	LT 34	LT 34	BT 22 M32	LT 34	LT 34	XT 10	BT 16	FT 37	AT 11	FT 37	AT 11 M300 M313	FT 37	AT 11 MA28 MA31	FT 37	AT 11 MA00 MA13	XT 10			
B	XT 10	ZT 25 Y	ZT 25 Y		IT 16	BT 22	BT 22	XT 10	IT 14 NM00 NM07	FT 38 M00 M07	IT 14 NM08 NM15	FT 38 M08 M15	BT 24	BT 24	IT 24	BT 24	FT 38 M16 M23	IT 14 NM16 NM23	FT 38 M24 M31	IT 14 NM24 NM31	XT 10	BT 16	ZT 25 Y	FT 37	AT 11 MC14 MC27	FT 37	AT 11 MB14 MB27	FT 37	AT 11 MB28 MB31	FT 37	AT 11 MA14 MA27	XT 10		
C	XT 10			BT 22		DT 11	HT 15	HT 15	DT 11	HT 15	XT 10	ST 14	ST 14	LT 20	LT 21	LT 20	LT 21	LT 21	LT 21	XT 10		LT 21	AT 11 MC28 MC31	FT 37	AT 11 MQA	BT 16	AT 10 LA15 LA28	BT 16	AT 31	XT 10				
D	XT 10	XT 10	BT 16	IT 16	AT 16	BT 22	BT 22	BT 22	BT 22	BT 22	BT 22	XT 10	IT 25	BT 25	BT 16	IT 16	FT 38 L26 L31	IT 14 NL26 NL31	LT 34	FT 38 L18 L25	IT 14 NL18 NL25	XT 10	LT 21	AT 11 MQC	BT 22	AT 10 LC15 LC28	LT 19	AT 11 MQB	FT 38	XT 10				
E	ST 21	ST 21	ST 21	ST 21	ST 21	ST 21	ST 10	ST 10	ST 10	ST 10	ST 10	ST 10	ST 10	ST 10	ST 10	ST 10	ST 10	ST 10	ST 10	ST 10	ST 10	ST 22	ST 22	ST 22	ST 22	ST 22	ST 22	ST 22	ST 10	ST 10	ST 10	ST 10		
F	0-5	6-9	10-15	16-21	22-25 32	26-31	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5		
F	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11	ST 11			
G	111549 4K	111549 12K	111549 8K	111549 16K	111549 4K	111549 12K	111549 8K	111549 16K	111549 4K	111549 12K	111549 8K	111549 16K	111549 4K	111549 12K	111549 8K	111549 16K	111549 4K	111549 12K	111549 8K	111549 16K	111549 4K	111550 12K	111550 8K	111550 16K	111550 4K	111550 12K	111550 8K	111550 16K	111550 4K	111550 12K	111550 8K	111550 16K		
H	BYTE 0 BITS 0-7				BYTE 1 BITS 8-15				BYTE 2 BITS 16-23				BYTE 3 BITS 24-32																					
J	HT 26	HT 26	HT 26	HT 26	HT 26	HT 11	HT 11	ST 34 STROB GEN BYT# 0-1	HT 11	HT 26	HT 26	HT 26	HT 26	HT 26	HT 26	ST 15	HT 26	HT 26	HT 26	HT 26	HT 26	HT 26	HT 26	HT 26	HT 11	HT 11	ST 34 STROB GEN BYT# 2-3	HT 11	HT 26	HT 26	HT 26	HT 26	HT 26	ST 17
	0-5	0-5 2	0-5 1	0-5 3	6-11	6-11 2	0-5	6-11	12-17	6-11 1	6-11 3	12-17	12-17 2	12-17 1	12-17 3	STACK SEL	18-23	18-23 2	18-23 1	18-23 3	24-29	24-29 2	24-29 1	18-21	22-26	27-32	27-32 1	27-32 3	30-32	30-32 2	30-32 1	VE -1.7		

1= 8K
2= 12K
3= 16K
4= OVER 4K
5= OVER 8K

6= 2-3 PORT EXP. } OPTION
7= 1-2 PORT EXP. } 8456

VM = 1/2 VD PIN21 STILL'S
* VD = 21.5 PINS1 F'ROW
VC = 24.00 27A45
VT = 0.35 TOP POT 7/20J15
VS = 3.00 BOTTOM POT 7/24J24
VE = 1 VOLT LESS THAN -B 1J38
-1.7V = 1J18

* Final VD setting should be mid-point of the Schmoö

Y DIRECTION ↑

STACK																
15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	XV	XC	YV	YC	YV	YV	XC									

ST21	ST21	ST21	ST21	ST21	ST21	ST10	ST10	ST10	ST10	ST10	ST10	ST10	ST10	ST10	ST10		
INHIBITS						X DRIVES											
BITS	BITS	BITS	BITS	BITS	BITS												
0-5	6-9	10-15	16-21	22-25,32	26-31	XV	XV	XV	XV	XV	XV	XV	XV	XV	XV		
						30-31	28-29	26-27	24-25	22-23	20-21	18-19	16-17	14-15	12-13		
0 YPIP 50 0 YNIN 26 1 YPIP 46 1 YNIN 23 2 YPIP 37 2 YNIN 12 3 YPIP 36 3 YNIN 13 4 YPIP 34 4 YNIN 11 5 YPIP 28 5 YNIN 01	6 YPIP 50 6 YNIN 12 7 YPIP 46 7 YNIN 13 8 YPIP 37 8 YNIN 11 9 YPIP 36 9 YNIN 01	10 YPIP 50 10 YNIN 26 11 YPIP 46 11 YNIN 23 12 YPIP 37 12 YNIN 12 13 YPIP 36 13 YNIN 13 14 YPIP 34 14 YNIN 11 15 YPIP 28 15 YNIN 01	16 YPIP 50 16 YNIN 26 17 YPIP 46 17 YNIN 23 18 YPIP 37 18 YNIN 12 19 YPIP 36 19 YNIN 13 20 YPIP 34 20 YNIN 11 21 YPIP 28 21 YNIN 01	22 YPIP 50 22 YNIN 26 23 YPIP 46 23 YNIN 23 24 YPIP 37 24 YNIN 12 25 YPIP 36 25 YNIN 13 26 YPIP 34 26 YNIN 11 27 YPIP 28 27 YNIN 01	26 YPIP 50 26 YNIN 26 27 YPIP 46 27 YNIN 23 28 YPIP 37 28 YNIN 12 29 YPIP 36 29 YNIN 13 30 YPIP 34 30 YNIN 11 31 YPIP 28 31 YNIN 01												
32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17		

E

Page 3-2

ST10	ST10	ST10	ST10	ST10	ST10	ST22	ST22	ST22	ST22	ST22	ST22	ST10	ST10	ST10	ST10
X DRIVES						PREDRIVES						BIT 32 Y DRIVES			
XV	XV	XV	XY	XV											
10-11	8-9	6-7	4-5	2-3								YV	YV	YV	
												0-1	2-3	4-5	
XC	XC	XC	XC	XC											
10-11	8-9	6-7	4-5	2-3								YC	YC	YC	
												2-3	2-3	4-5	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

E

Page 3-3

ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	
							Y DRIVES									
YV+YC 0-1 Bits 0-3	YV+YC 0-1 Bits 4-7	YV+YC 2-3 Bits 0-3	YV+YC 2-3 Bits 4-7	YV+YC 4-5 Bits 0-3	YV+YC 4-5 Bits 4-7	YV+YC 6-7 Bits 0-3	YV+YC 6-7 Bits 4-7	YV+YC 0-1 Bits 8-11	YV+YC 0-1 Bits 12-15	YV+YC 2-3 Bits 8-11	YV+YC 2-3 Bits 12-15	YV+YC 4-5 Bits 8-11	YV+YC 4-5 Bits 12-15	YV+YC 6-7 Bits 8-11	YV+YC 6-7 Bits 12-15	
32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	

ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	ST11	
							Y DRIVES									
YV+YC 0-1 Bits 16-19	YV+YC 0-1 Bits 20-23	YV+YC 2-3 Bits 16-19	YV+YC 2-3 Bits 20-23	YV+YC 4-5 Bits 16-19	YV+YC 4-5 Bits 20-23	YV+YC 6-7 Bits 16-19	YV+YC 6-7 Bits 20-23	YV+YC 0-1 Bits 24-27	YV+YC 0-1 Bits 28-31	YV+YC 2-3 Bits 24-27	YV+YC 2-3 Bits 28-31	YV+YC 4-5 Bits 24-27	YV+YC 4-5 Bits 28-31	YV+YC 6-7 Bits 24-27	YV+YC 6-7 Bits 24-27	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

28 YV 6 48
 29 YV 6 50
 30 YV 6 47
 31 YV 6 49
 28 YV 7 46
 29 YV 7 45
 30 YV 7 40
 31 YV 7 39
 28 YC6 P 22
 28 YC6 N 10
 29 YC6 P 19
 29 YC6 N 11
 30 YC6 P 12
 30 YC6 N 09
 31 YC6 P 24
 31 YC6 N 08
 28 YC7 P 01
 28 YC7 N 00
 29 YC7 P 34
 29 YC7 N 02
 30 YC7 P 31
 30 YC7 N 04
 31 YC7 P 28
 31 YC7 N 06
 VM 21
 VP 51

Σ 5/7 MEMORY

HT26	HT26	HT26	HT26	HT26	HT26	HT11	HT11	ST34	HT11	HT26	HT26	HT26	HT26	HT26	HT26
4K	12K	8K	16K	4K	12K	BITS	BITS	STROBES	BITS	8K	16K	4K	12K	8K	16K
BITS	BITS	BITS	BITS	BITS	BITS	0-5	6-10	0-1	12-17	BITS	BITS	BITS	BITS	BITS	BITS
0-5	0-5	0-5	0-5	6-11	6-11					6-11	6-11	12-17	12-17	12-17	12-17
OUTPUT PINS	INPUT PINS					OUTPUT PINS	OUTPUT PINS	OUTPUT PINS	OUTPUT PINS						
SPA00P 37	45L00P 09	25L04P 21				MDO0 40	MDO6 40	SAST0 29	MD12 38						
SPA0CN 36	45L00N 08	25L04N 20				TURN00 43	TURN06 43	SAST1 18	TURN012 39						
SPA01P 35	55L00P 11	35L04P 13				MDO1 38	MDO7 38	VS 29	MD13 34						
SPA01N 34	55L00N 10	35L04N 12				TURN01 39	TURN07 39	VT 15	TURN013 33						
SPA02P 41	45L01P 25	25L05P 07				MDO2 34	MDO8 12		MD14 14						
SPA02N 40	45L01N 24	25L05N 06				TURN02 33	TURN08 14	INPUT PINS	TURN014 14						
SPA03P 39	55L01P 23	35L05P 15				MDO3 12	MDO9 08	NTSSTB 17	MD15 08						
SPA03N 38	55L01N 22	35L05N 14				TURN03 14	TURN09 06	NTSSTB 31	TURN015 06						
SPA04P 43	45L02P 03	PASL2 30				MDO4 08	MD10 04		MD16 04						
SPA04N 42	45L02N 02	PASL3 30				TURN04 06	TURN10 01		TURN016 01						
SPA05P 45	55L02P 05	PASL2 33				MDO5 04	MD11 34		MD17 40						
SPA05N 44	55L02N 04	PASL3 31				TURN05 01	TURN11 33		TURN017 43						
VE 28	45L03P 19					-1.7V 02	-1.7V 02		-1.7V 02						
	45L03N 18					VC 30	VC 30		VC 30						
	55L03P 27														
	55L03N 26														

32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17

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ST15	HT26	HT26	HT26	HT26	HT26	HT26	HT11	HT11	ST34	HT11	HT26	HT26	HT26	HT26	ST17
PASL	4K	12K	8K	16K	4K	12K	BITS	BITS	STROBES	BITS	8K	16K	4-8K	12-16K	-1.7V
0-7	BITS	BITS	BITS	BITS	BITS	BITS	18-21	22-26	2-3	27-32	BITS	BITS	BITS	BITS	VE
	18-23	18-23	18-23	18-23	24-29	24-29					24-29	24-29	30-32	30-32	
OUTPUT PINS							OUTPUT PINS	OUTPUT PINS	OUTPUT PINS	OUTPUT PINS					OUTPUT PINS
PASL0 28							MD18 34	MD22 40	SAST2 29	MD27 40					-1.7V 18
PASL1 30							TURN018 33	TURN022 43	SAST3 18	TURN027 43					Ve 38
PASL2 26							MD19 12	MD23 38	VS 24	MD28 38					INPUT PINS
PASL3 24							TURN019 14	TURN023 39	VT 15	TURN028 39					VC 01
PASL4 20							MD20 08	MD24 12		MD29 34					VD 20
PASL5 18							TURN020 06	TURN024 14	INPUT PINS	TURN029 33					
PASL6 21							MD21 04	MD25 08	NTSSTB 17	MD30 12					
PASL7 03							TURN021 01	TURN025 06	NTSSTB 31	TURN030 14					
							-1.7V 02	MD26 04		MD31 08					
							VC 30	TURN026 01		TURN031 06					
								-1.7V 02		MD32 02					
								VC 30		TURN032 02					
										-1.7V 02					
										VC 30					

16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

5517 MEMORY

Bit Location.

TURNOVER = Strobe + Core turnover

To look at coreturnover only ground: 31D17

Strobe Loc.

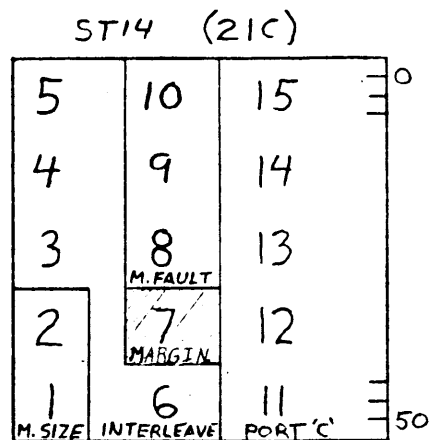
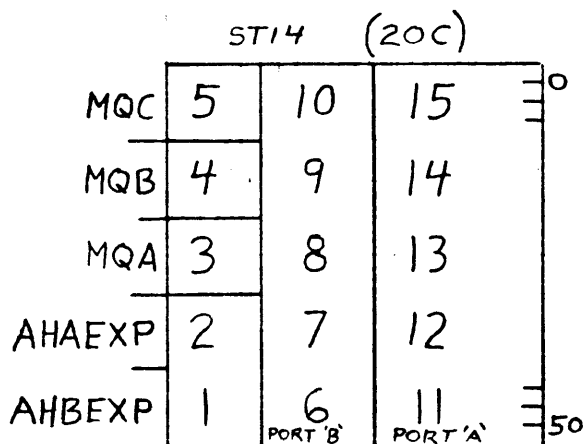
SAST 0	24 J 29
SAST 1	24 J 18
SAST 2	07 J 29
SAST 3	07 J 18

BIT #	TURNOVER	SENSE AMP OUTPUT			M Reg.	BIT #
0	26 J 43	26 J 40	23 B 45	23 B 37	0	
1	26 J 39	26 J 38	23 B 26	23 B 33	1	
2	26 J 33	26 J 34	23 B 41	23 B 34	2	
3	26 J 14	26 J 12	23 B 42	23 B 35	3	
4	26 J 06	26 J 08	23 B 19	23 B 18	4	
5	26 J 01	26 J 04	23 B 04	23 B 13	5	
6	25 J 43	25 J 40	23 B 07	23 B 14	6	
7	25 J 39	25 J 38	23 B 06	23 B 15	7	
8	25 J 14	25 J 12	21 B 45	21 B 37	8	
9	25 J 06	25 J 08	21 B 26	21 B 33	9	
10	25 J 01	25 J 04	21 B 41	21 B 34	10	
11	25 J 33	25 J 34	21 B 42	21 B 35	11	
12	23 J 39	23 J 38	21 B 19	21 B 18	12	
13	23 J 33	23 J 34	21 B 04	21 B 13	13	
14	23 J 14	23 J 12	21 B 07	21 B 14	14	
15	23 J 06	23 J 08	21 B 06	21 B 15	15	
16	23 J 01	23 J 04	16 B 45	16 B 37	16	
17	23 J 43	23 J 40	16 B 26	16 B 33	17	
18	09 J 33	09 J 34	16 B 41	16 B 34	18	
19	09 J 14	09 J 12	16 B 42	16 B 35	19	
20	09 J 06	09 J 08	16 B 19	16 B 18	20	
21	09 J 01	09 J 04	16 B 04	16 B 13	21	
22	08 J 43	08 J 40	16 B 07	16 B 14	22	
23	08 J 39	08 J 38	16 B 06	16 B 15	23	
24	08 J 14	08 J 12	14 B 45	14 B 37	24	
25	08 J 06	08 J 08	14 B 26	14 B 33	25	
26	08 J 01	08 J 04	14 B 41	14 B 34	26	
27	06 J 43	06 J 40	14 B 42	14 B 35	27	
28	06 J 39	06 J 38	14 B 19	14 B 18	28	
29	06 J 33	06 J 34	14 B 04	14 B 13	29	
30	06 J 14	06 J 12	14 B 07	14 B 14	30	
31	06 J 06	06 J 08	14 B 06	14 B 15	31	
32	06 J 01	06 J 04	14 A 13	14 A 07	32	

L Decode

18	19	20	21	22	23	24	25	26	27	28	29	30	31
XV	XC	YC	YV	YV	YV	XC					XV		
YV	YC												

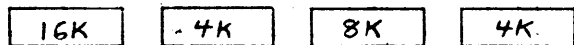
Not used for Volt. or Cur.



RULES FOR SETTING UP STARTING ADDRESS

1. MUST BE NO GAPS
2. STARTING ADDRESS MUST BE WHOLE MULTIPLE OF MEMORY SIZE
3. 12K MEMORY SIZE START AT MULTIPLES OF 16K (0, 16, 32, 48 ETC.)

0-16K-1 24-28K-1 16-24K-1 28-32K-1 → OK



20-28K-1 → NOT OK

STARTING ADD.	L15	L16	L17	L18	L19	20C PORT B
	SWG	7	8	9	10	(20C PORT A)(21C PORT C)
OK	0	0	0	0	0	
4K	0	0	0	0	1	
8K	0	0	0	1	0	
12K	0	0	0	1	1	
16K	0	0	1	0	0	
20K	0	0	1	0	1	
24K	0	0	1	1	0	
28K	0	0	1	1	1	
32K	0	1	0	0	0	
48K	0	1	1	0	0	
64K	1	0	0	0	0	
80K	1	0	1	0	0	
96K	1	1	0	0	0	
112K	1	1	1	0	0	
128K	1	1	1	1	1	

4K INCREMENTS

16K INCREMENTS

*NOTE ENDING ADDRESS DETERMINED BY MEMORY SIZE SWITCHS

Σ 5/7 MEMORY SWITCHS

21C

MEM SIZE	SW1	SW2
4K	0	0
8K	0	1
12K	1	0
16K	1	1

- INTERLEAVING SWITCHS
1. SET SAME VALUE ALL DOORS
 2. TOTAL MEM. SIZE MUST BE EQUAL TO 8K, 16K, 32K OR 64K

TOTAL M. SIZE	SW6	SW5	SW4	SW3
8K	0	0	0	1
16K	0	0	1	0
32K	0	1	0	0
64K	1	0	0	0

21C

MEMORY FAULT LIGHTS

21C

LITE	SW8	SW9	SW10
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

MEMORY TIMING MARGINS

21C

SW7	SPEED
0	SLOW
1	FAST

(DOWN)
(UP)

PORT EXPANDER CABLING (TYPICAL)

STARTING ADD. SW's

1st PORT EXPANDER

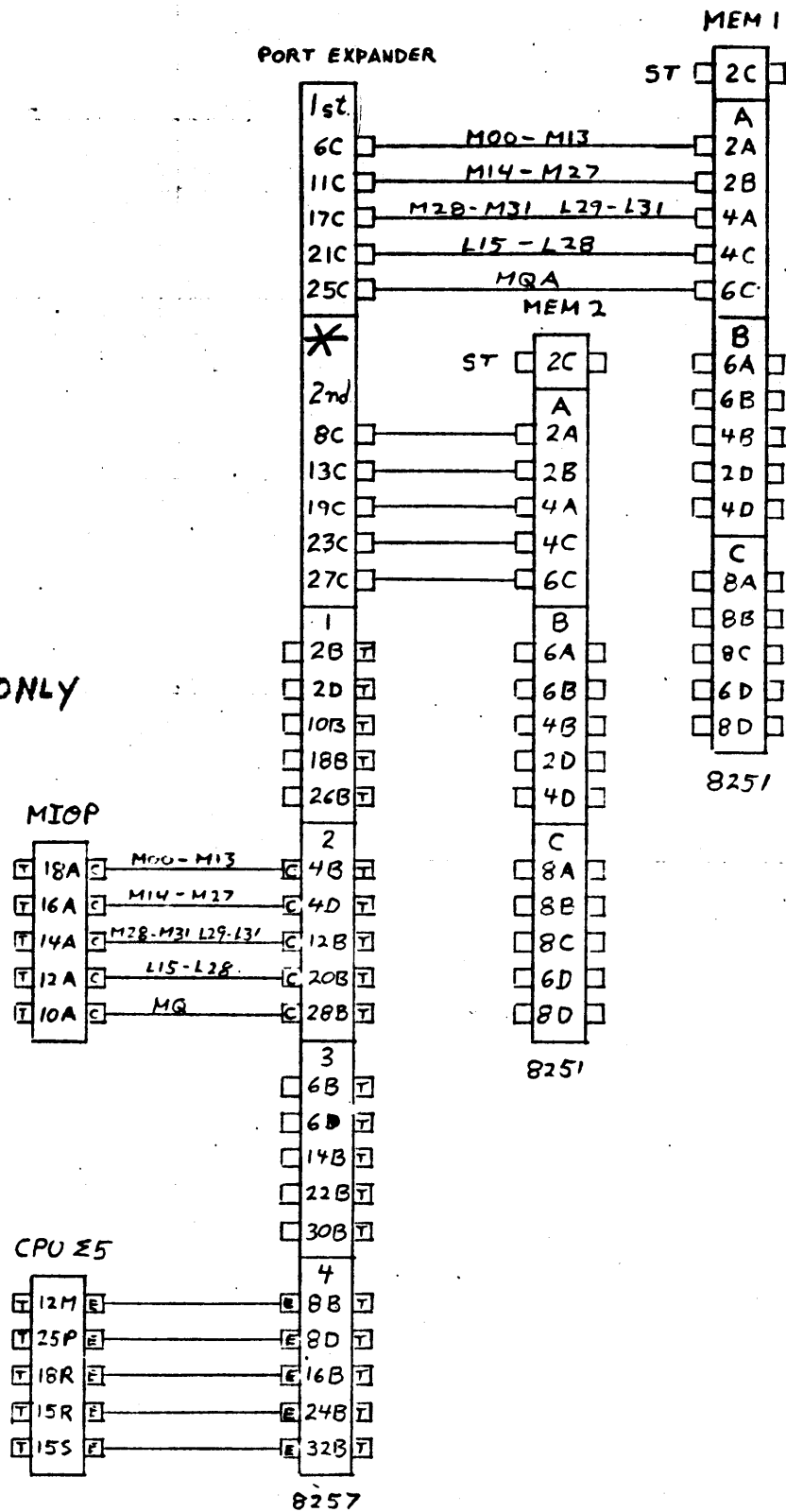
PORT	L15	L16	L17	L18	L19	
1	1	2	3	4	5	24D
2	6	7	8	9	10	
3	1	2	3	4	5	25D
4	6	7	8	9	10	

2d PORT EXPANDER

* PORT

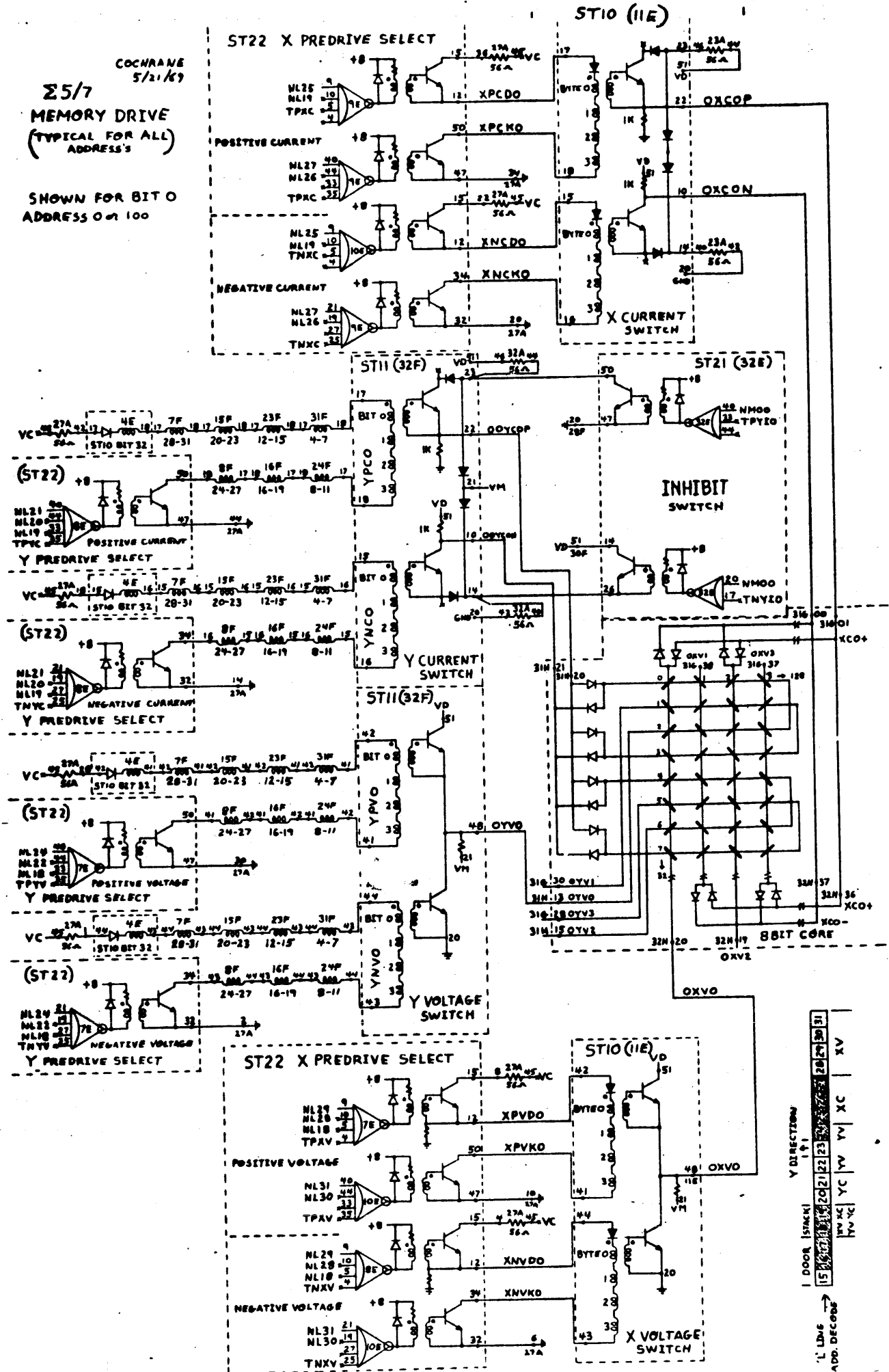
PORT	L15	L16	L17	L18	L19	
1	1	2	3	4	5	21E
2	6	7	8	9	10	
3	1	2	3	4	5	22E
4	6	7	8	9	10	

* DUAL EXPANDER ONLY



COCHRANE
5/21/69
Σ5/7
MEMORY DRIVE
(TYPICAL FOR ALL)
ADDRESS'S

SHOWN FOR BIT 0
ADDRESS 0 or 100



Y DIRECTION

15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

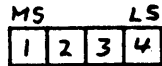
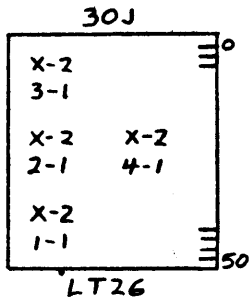
DOOR ISAKKI 1-1
L LINE
ADD. DECODE

PRIORITY INTERRUPT CHASSIS
MODEL 0421

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
AT 11		LT 26		AT 13		AT 11		BT 17	BT 16	IT 25	BT 17		AT 11		LT 16	LT 16	LT 16	LT 16		AT 11		LT 16	LT 16	LT 16	LT 16	IT 25	BT 18	XT 10	FT 10		ST 14

1 = OPTIONAL NO. OF LEVELS 8422
2 LEVELS PER LT16

LOGIC EQUATION 124470-001
WIRE LIST 124472-001
PIN INDEX 124472-925

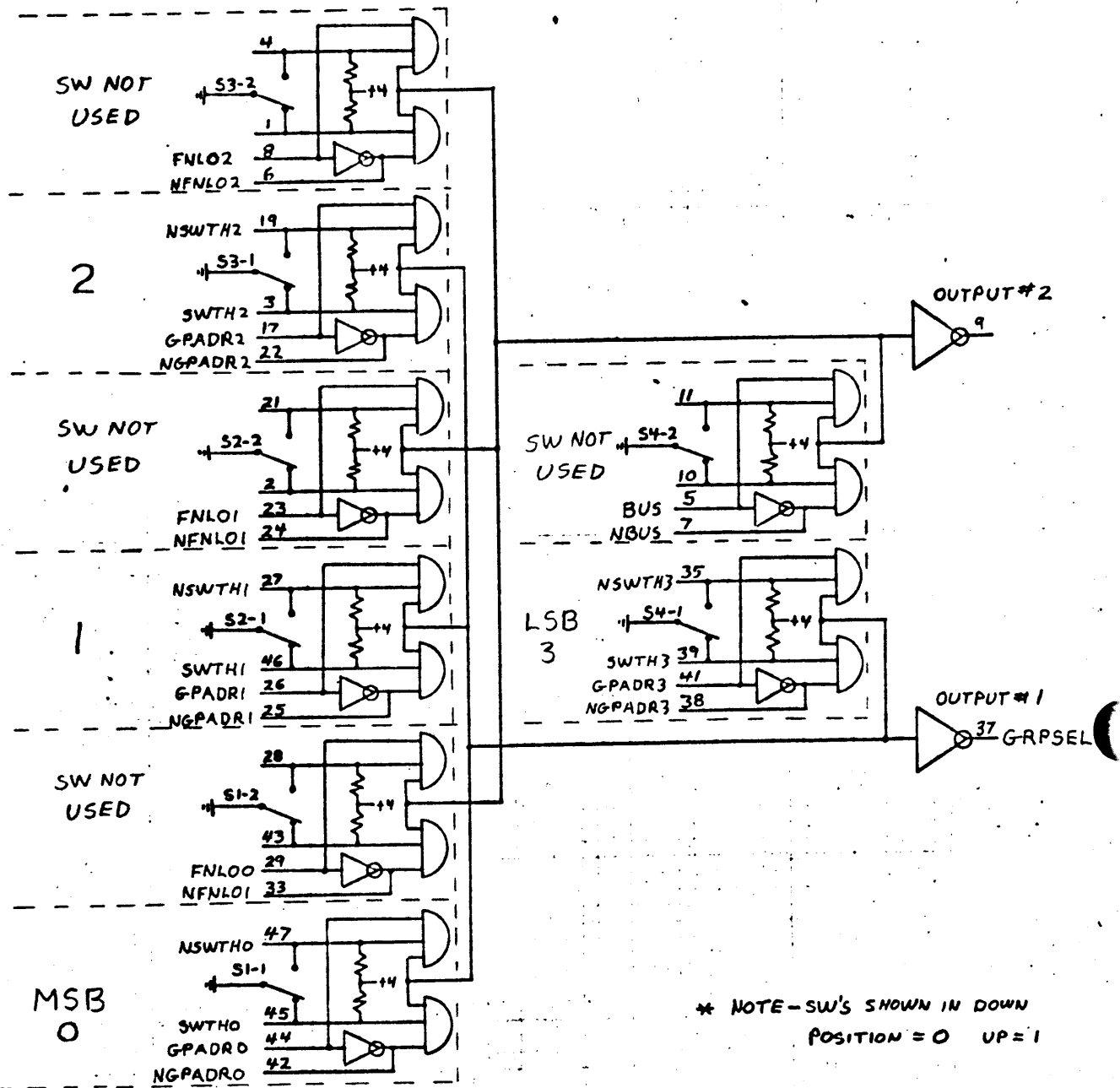


0 1 0 1 = GROUP 5

X = SW'S NOT USED

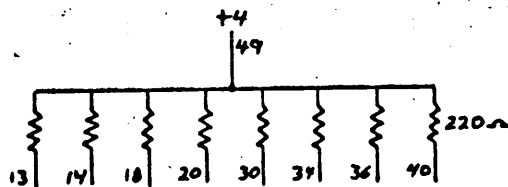
LT16	LEVEL	ST14 1J
7J	X0 X1	NONE
8J	X2 X3	SW1 SW2
9J	X4 X5	SW3 SW4
10J	X6 X7	SW5 SW6
14J	X8 X9	SW7 SW8
15J	XA XB	SW9 SW10
16J	XC XD	SW11 SW12
17J	XE XF	NONE SW13

SW'S TO 1 = UP
POSITION FOR
EACH LT16



MSB	1	2	LSB
0	1	2	3

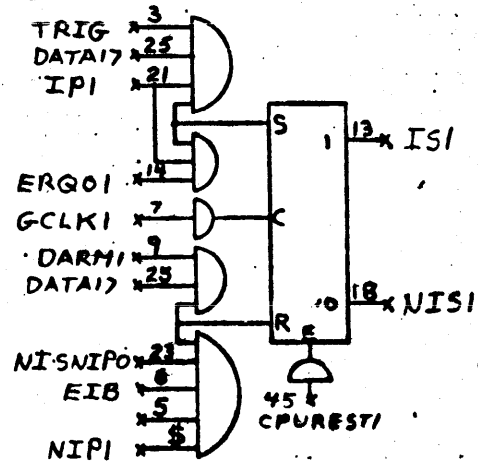
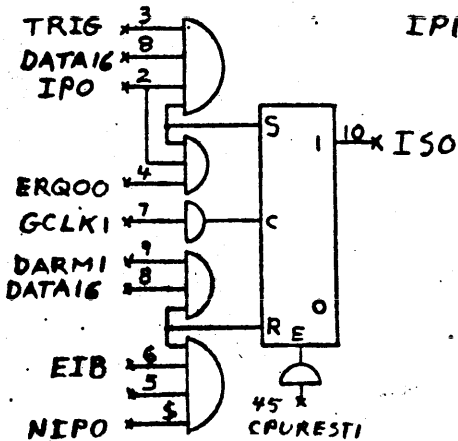
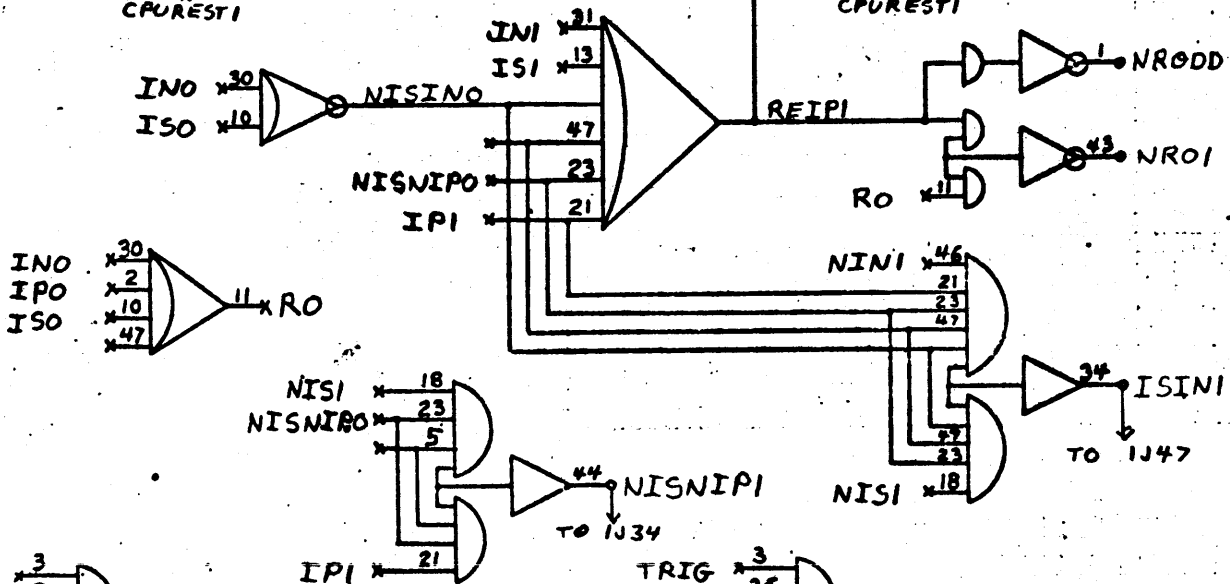
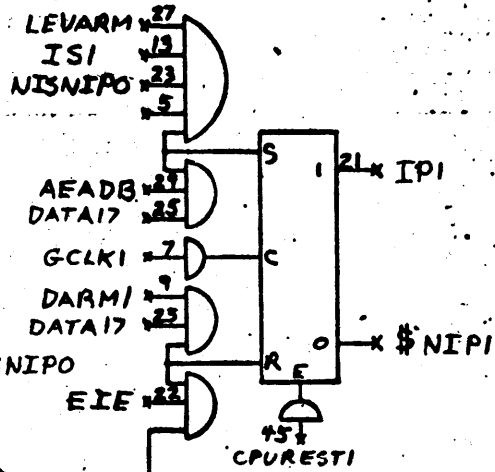
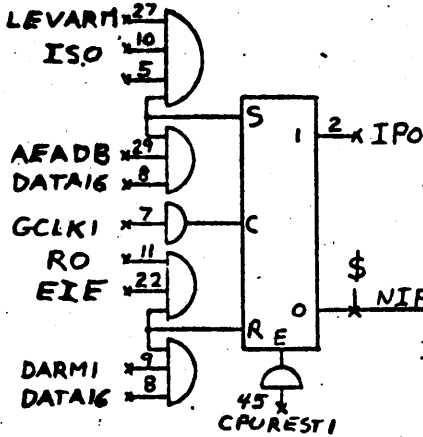
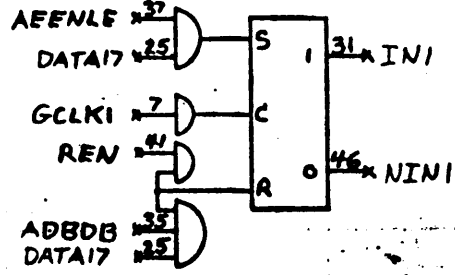
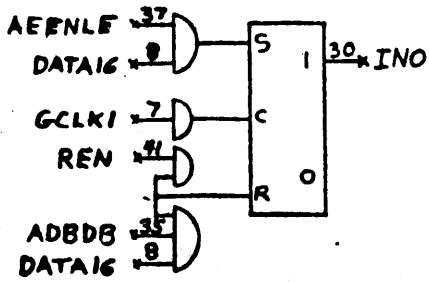
0 0 1 0 = GROUP 2

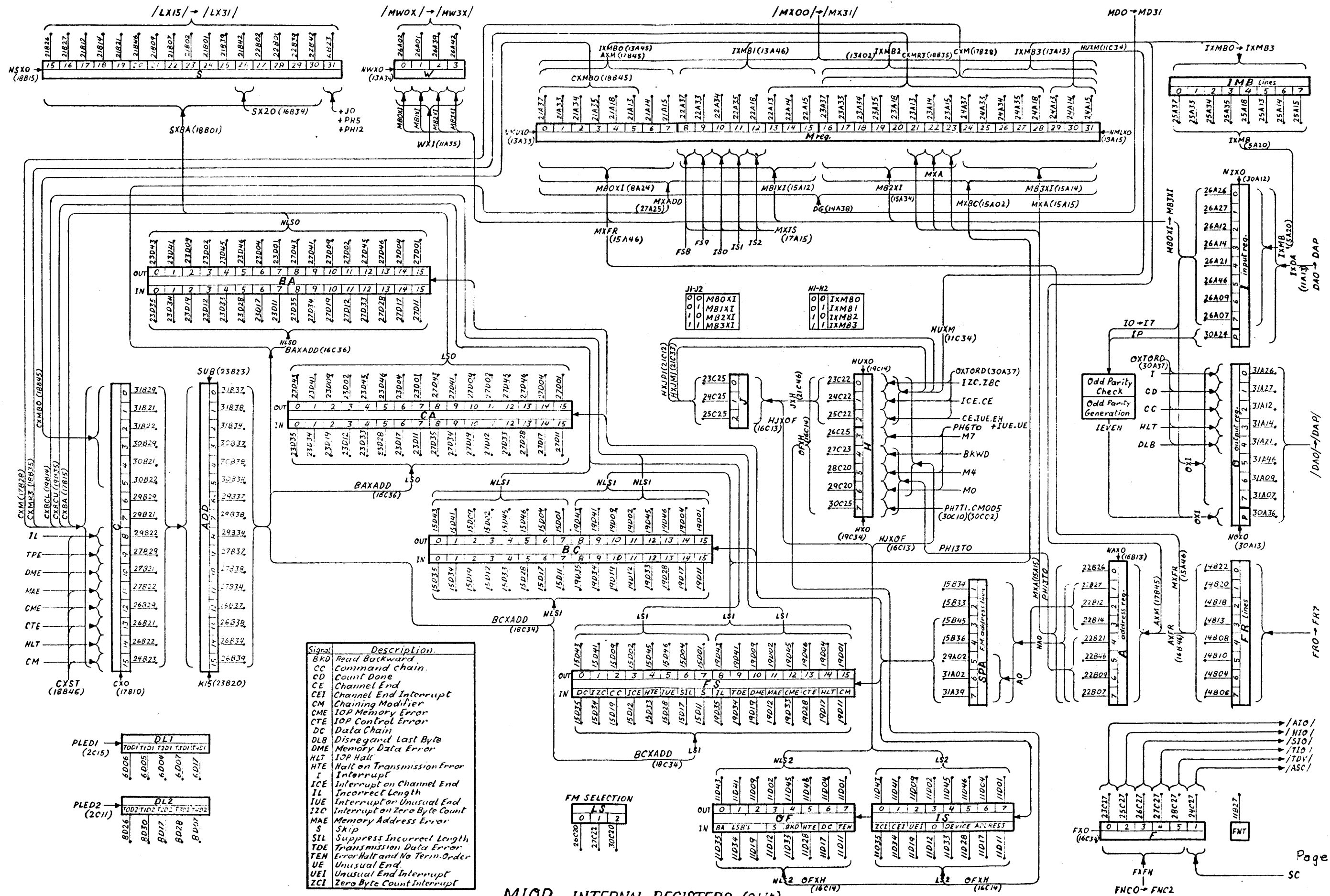


EXT. INTERRUPT LT26 (30J)
SWITCH SETTING

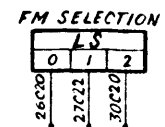
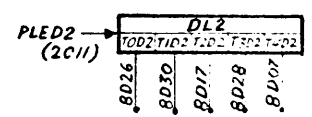
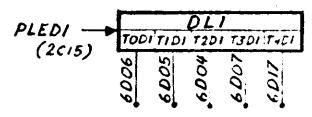
LT16 INTERRUPT

(7J) EXT. PRI. INT. CHASSIS
Σ 5/7-12



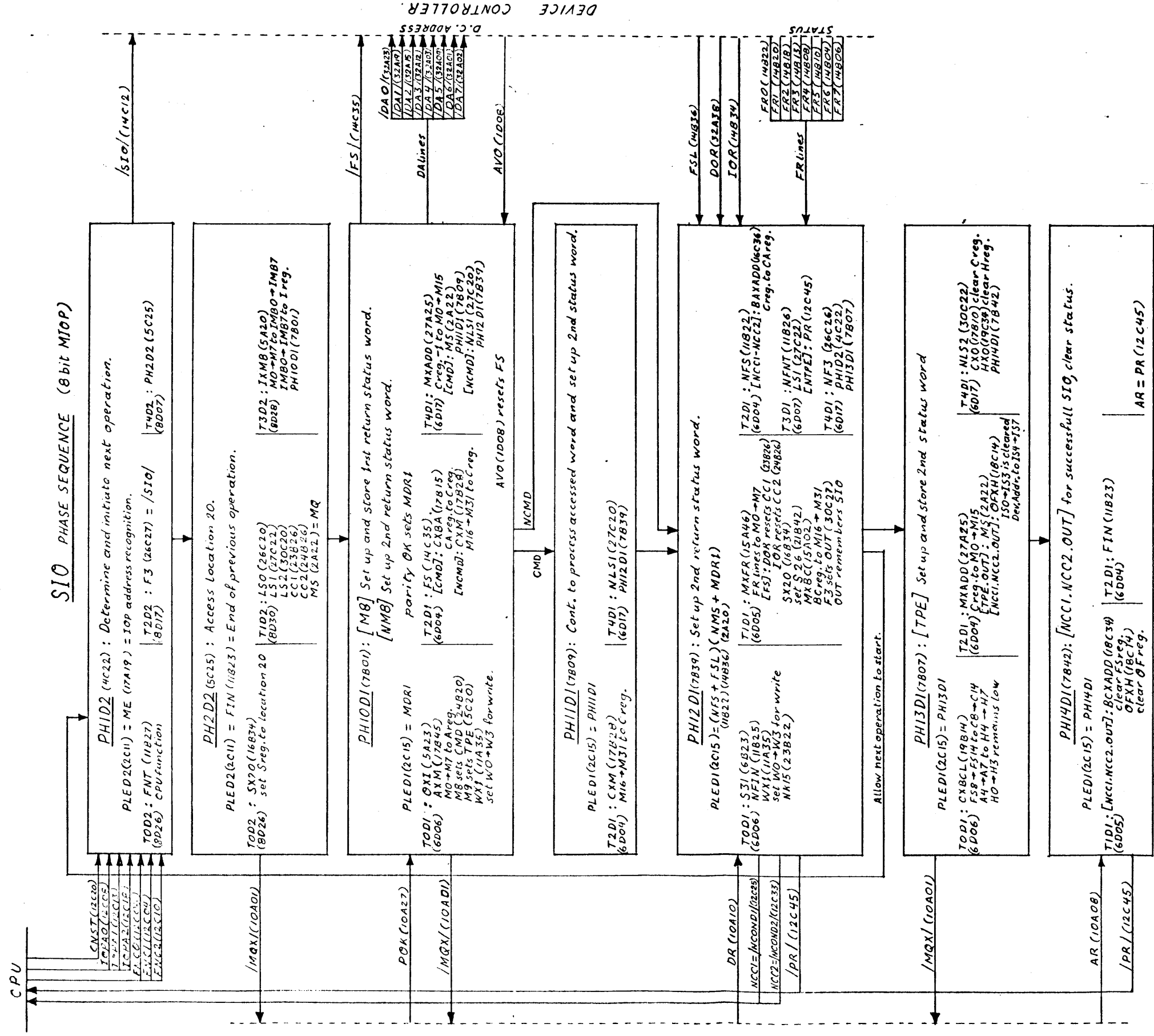


Signal	Description
BKD	Read Backward
CC	Command Chain
CD	Count Done
CE	Channel End
CEI	Channel End Interrupt
CM	Chaining Modifier
CME	TOP Memory Error
CTE	TOP Control Error
DC	Data Chain
DLB	Disregard Last Byte
DME	Memory Data Error
HLT	TOP Halt
HTE	Halt on Transmission Error
I	Interrupt
ICE	Interrupt on Channel End
IL	Incorrect Length
IUE	Interrupt on Unusual End
IZC	Interrupt on Zero Byte Count
MAE	Memory Address Error
S	Skip
SIL	Suppress Incorrect Length
TDE	Transmission Data Error
TEH	Error Halt and No Term. Order
UE	Unusual End
UEI	Unusual End Interrupt
ZCI	Zero Byte Count Interrupt

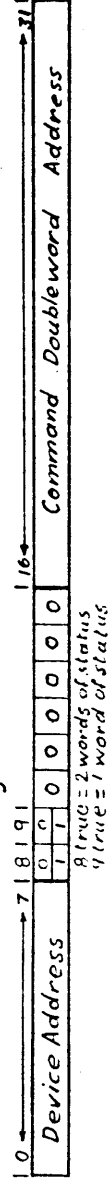


MIOP INTERNAL REGISTERS. (8bit)

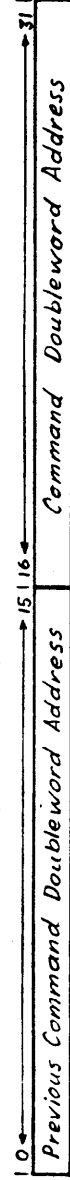
Note: Every PH#DI/2 (phase term) is reset at T3 time of its delay line.
 Every PH#PDI/2 (phase term) is set at T3 time of its delay line and reset at T0 time of its delay line.
 Leaving PH2P02 and PH7P01 or PH4P01 high until the next operation.



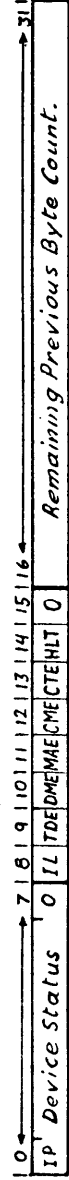
Location 20 before IOP storage



Location 20 after 1st. Status word is stored.

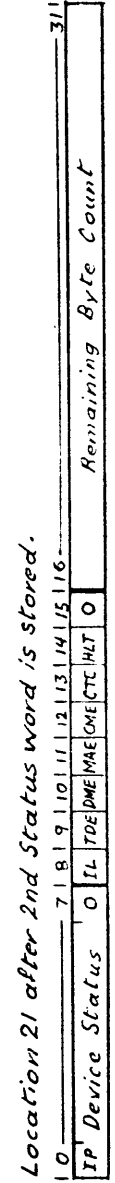
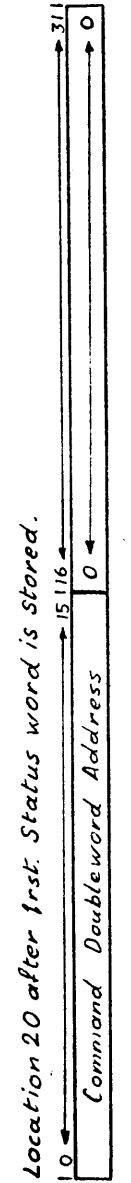
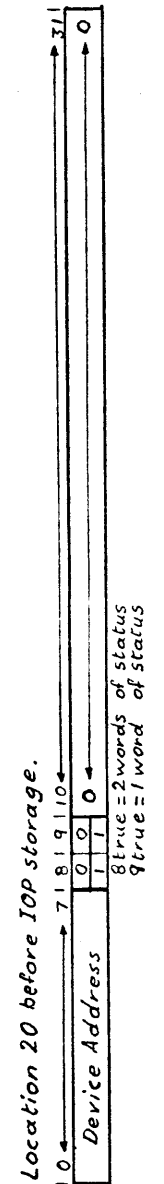
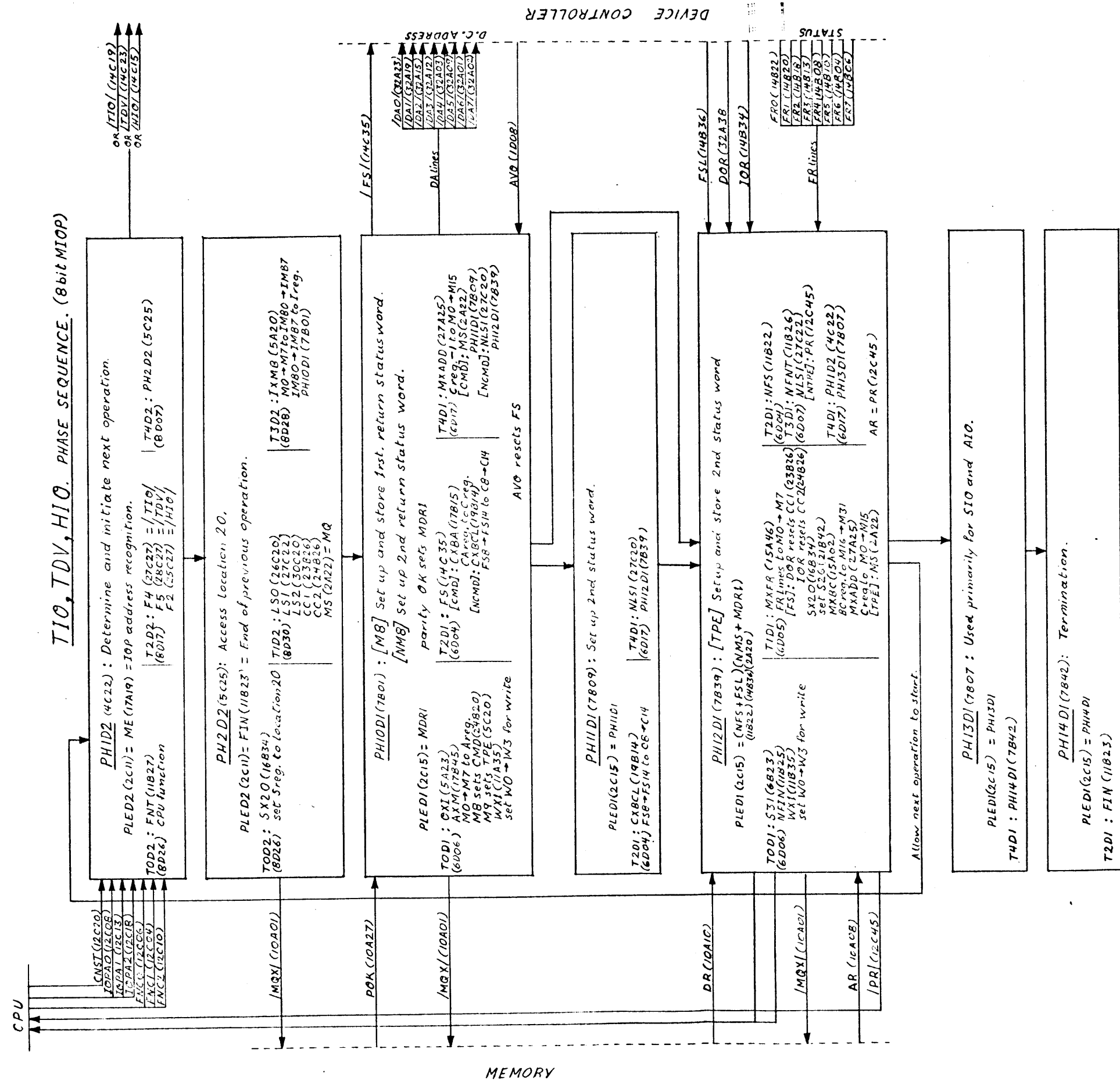


Location 21 after 2nd. Status word is stored.



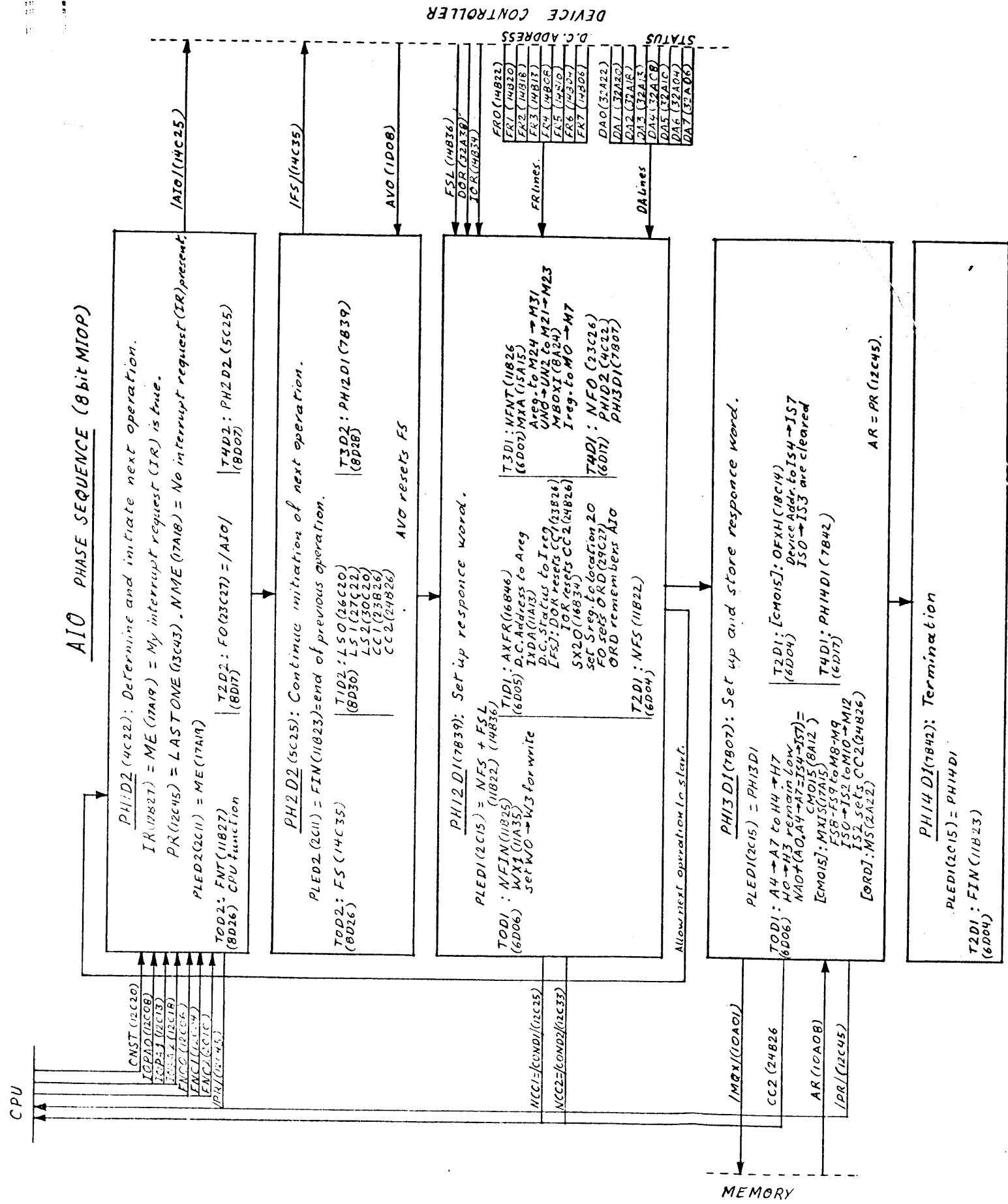
- CME = IOP memory error
- CTE = IOP control error
- DME = Memory data error
- HLT = IOP halt
- IL = Incorrect length
- IP = Interrupt pending
- MAE = Memory address error
- TDE = Transmission data error

Note: Every PH#D1/2 (phase term) is reset at T3 time of its delay line.
 Every PH#DD1/2 (phase term) is set at T1 time of its delay line and reset at T0 time of its delay line.
 Leaving PH2, PD2 and PH7D1 or PH4D1 high until the next operation.



CME = IOP memory error
 CTE = IOP control error
 DME = Memory data error
 HLT = IOP halt
 IL = Incorrect length
 IP = Interrupt pending
 MAE = Memory address error
 TDE = Transmission data error

Note: Every PHWDI/2 (Phase term) is reset at T3 time of its delay line.
 Every PHWDI/2 (Phase term) is set at T1 time of its delay line and is reset at T0 time of its delay line.
 Leaving PH2PD2 and PH7PD1 or PHMPD1 high until the next operation.



Location 20 after response is stored

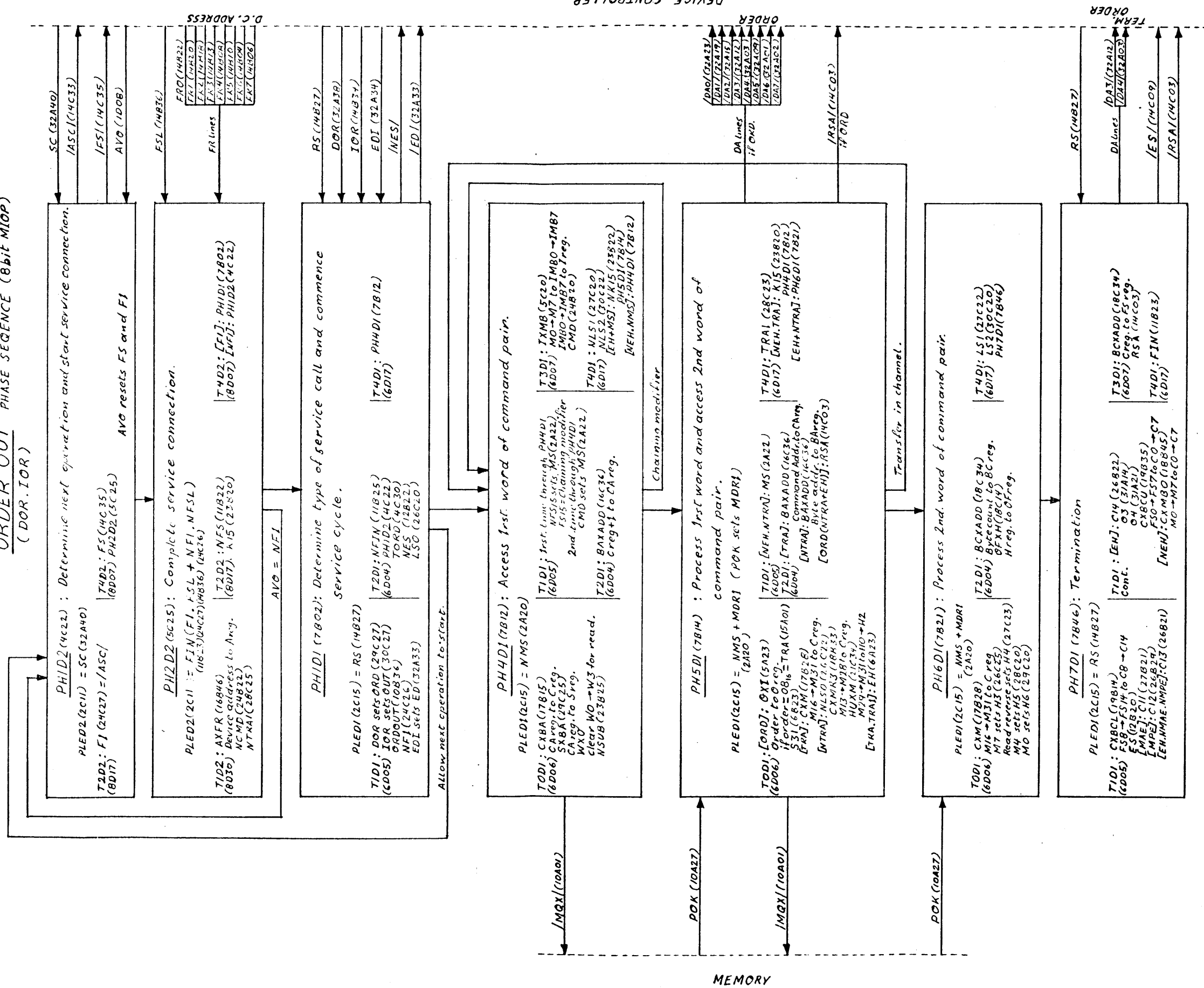
0	7	8	9	10	11	12	13	20	21	23	24	25	27	28	31
D.C. ADDRESS															
D.C. ADDRESS															

- CEI = Channel end interrupt
- D0 = Data overrun
- IL = Incorrect length
- TDE = Transmission data error
- UEI = Unusual end interrupt
- ZCI = Zero byte count interrupt
- D. = M=0/Device Cont. #, M=1/Unit #
- D.C. = Multiunit device cont. #
- M. = 1/Multiunit device, 0/single unit device.

Note: Every PHMDI/2 (phase term) is reset at T3 time of its delay line.
 Every PHMDI/2 (phase term) is set at T1 time of its delay line, and reset at T0 time of its delay line, leaving PH2PD2 and PH7PD1 or PH4PD1 true until the next operation.

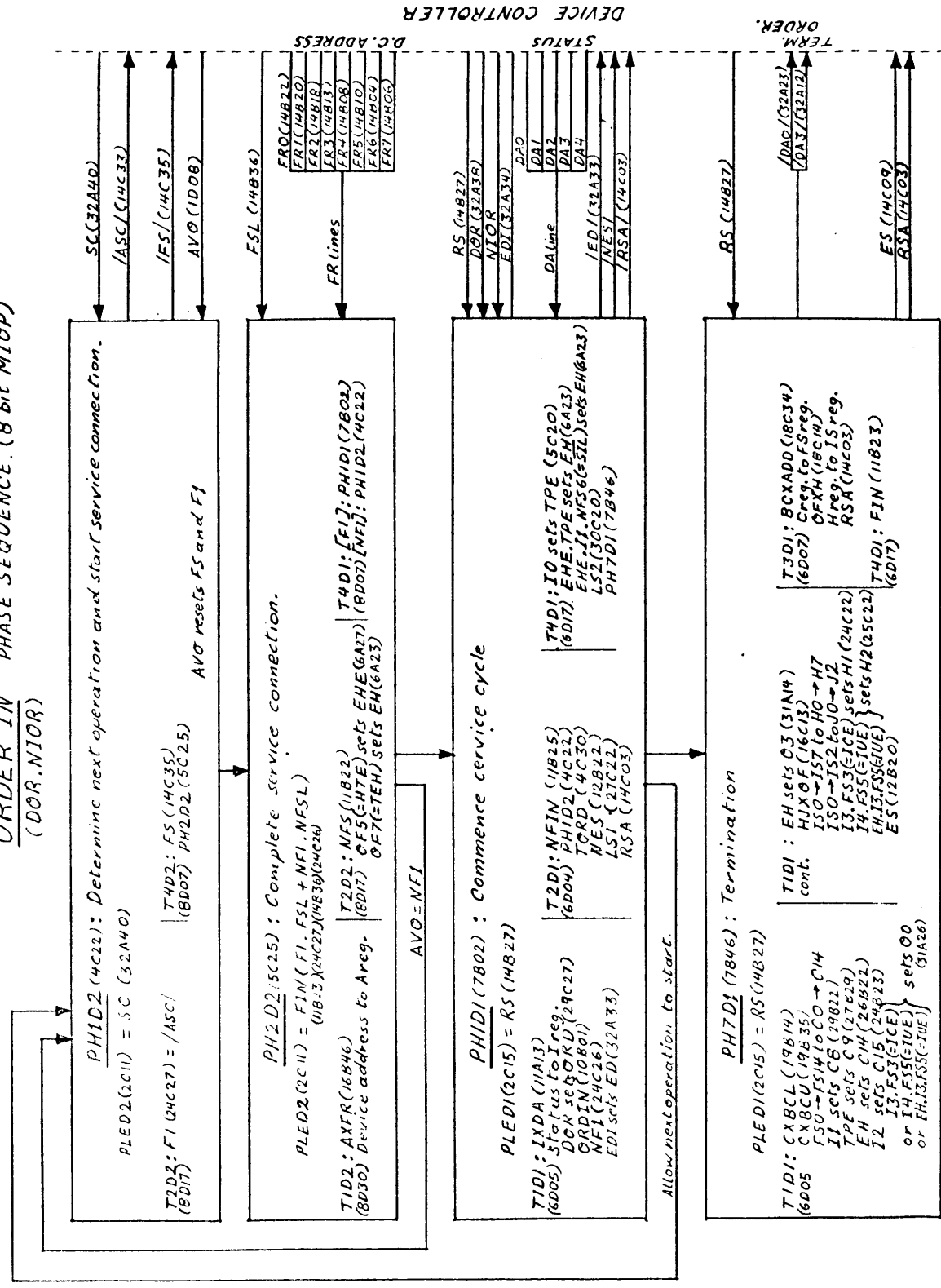
ORDER OUT PHASE SEQUENCE (8bit MIOP)

(DOR, IOR)



Note: Every PH#DI/2 (phase term) is reset at T3 time of its delay line.
 Every PH#PD/2 (phase term) is set at T1 time of its delay line and reset at T0 time of its delay line.
 Leaving PH2PD2 and PH7PD1 true until the next operation.

ORDER IN PHASE SEQUENCE (8 bit MIOP) (DOR, NIOR)



Status in I reg.

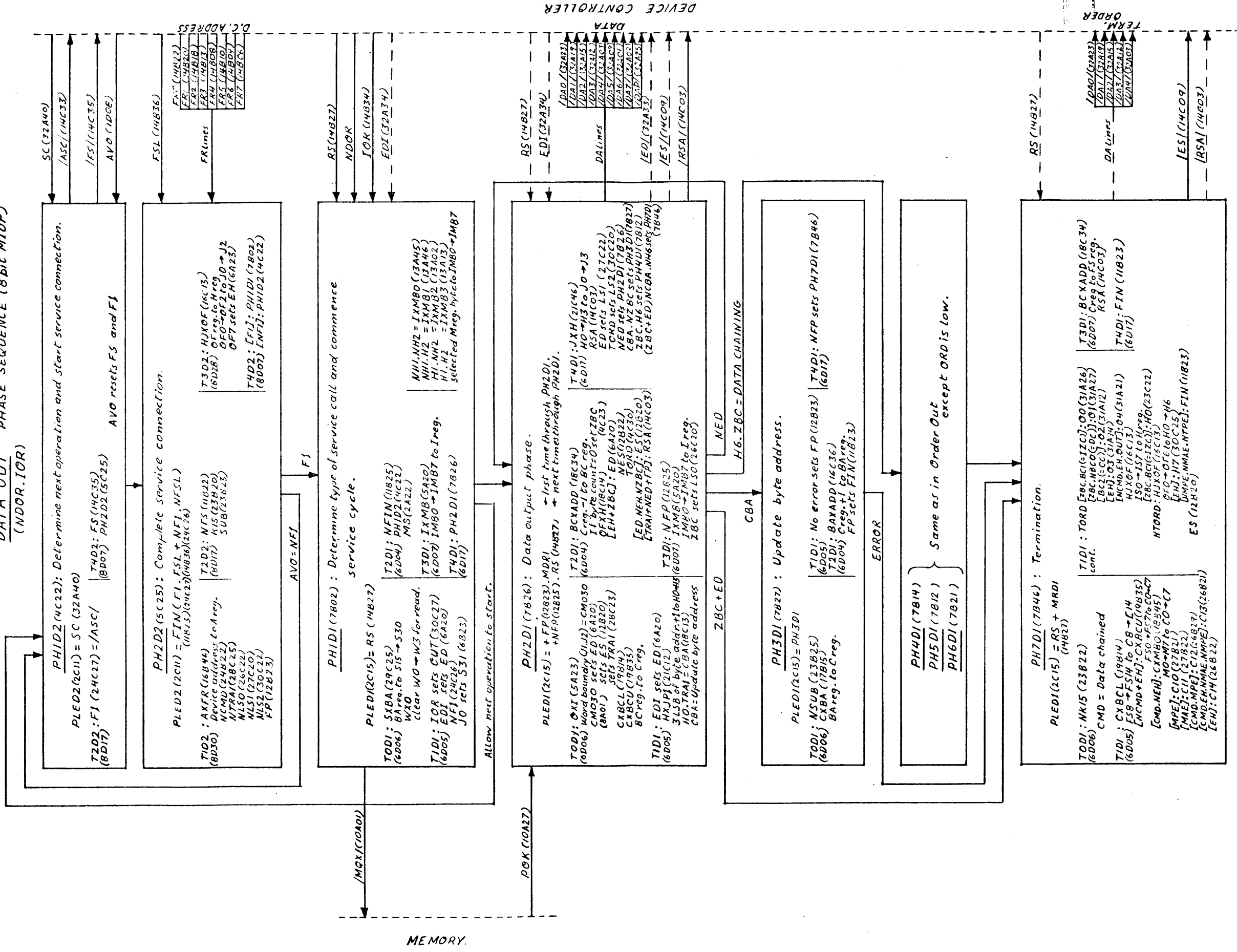
- I0 = TE = Transmission error
- J1 = IL = Incorrect length
- I2 = CM = Chaining modifier
- I3 = CE = Channel end
- I4 = UE = Unusual end

Terminal order in O reg.

- 00 = I = Interrupt
- 03 = HLT = IOP error halt.

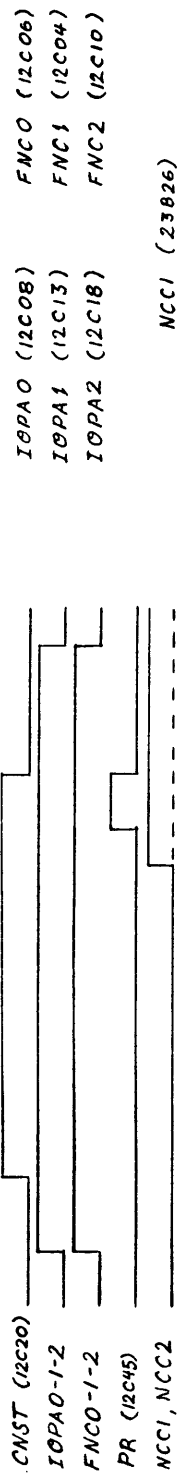
NOTE: Every PH#DI/2 (phase term) is reset at T3 time of its delay line.
 Every PH#PDI/2 (phase term) is set at T1 time of its delay line and reset at T0 time of its delay line.
 Leaving PH2PD2 and PH7PDI or PH3 PDI true until the next operation.

DATA OUT PHASE SEQUENCE (8 bit MIOP)
 (NDOR.IOR)

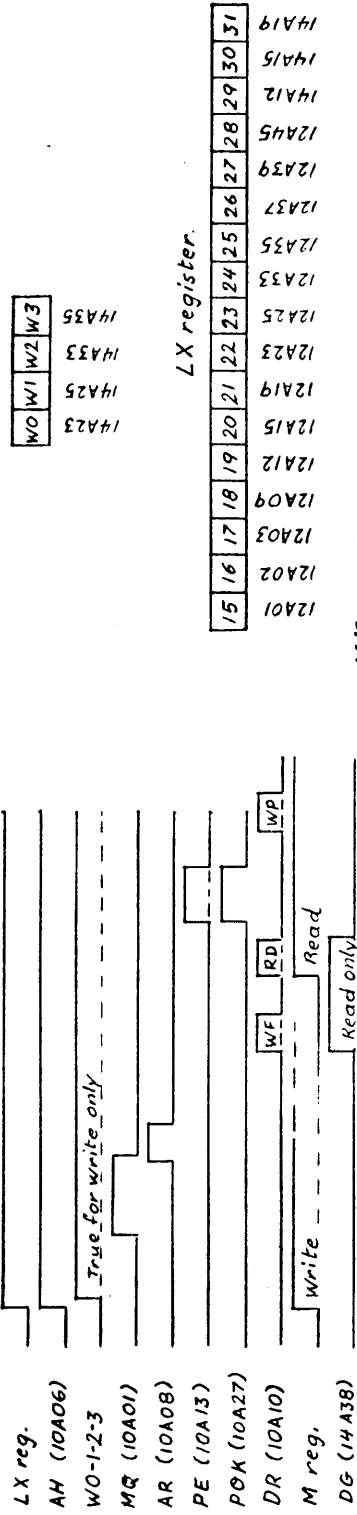


MIOP Interface (8 bit MIOP)

CPU / MIOP

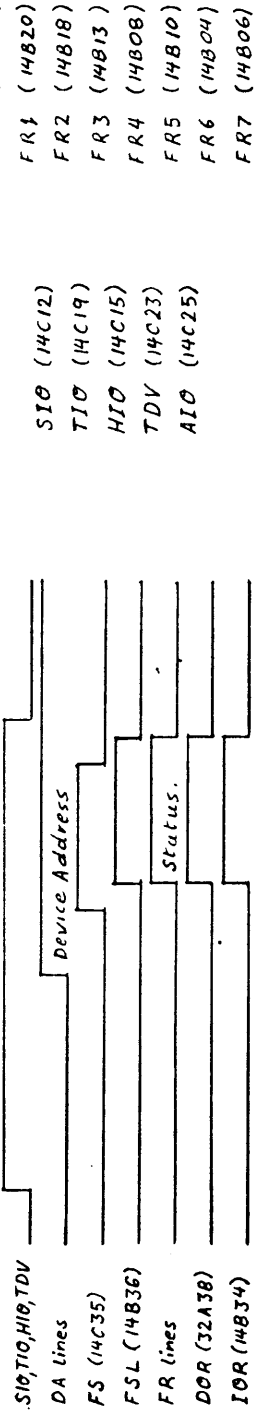


MEMORY / MIOP

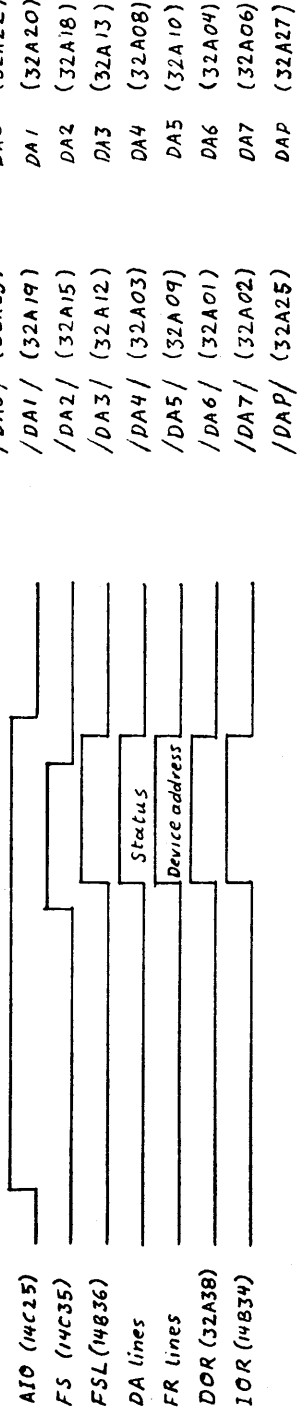


DEVICE CONTROLLER / MIOP

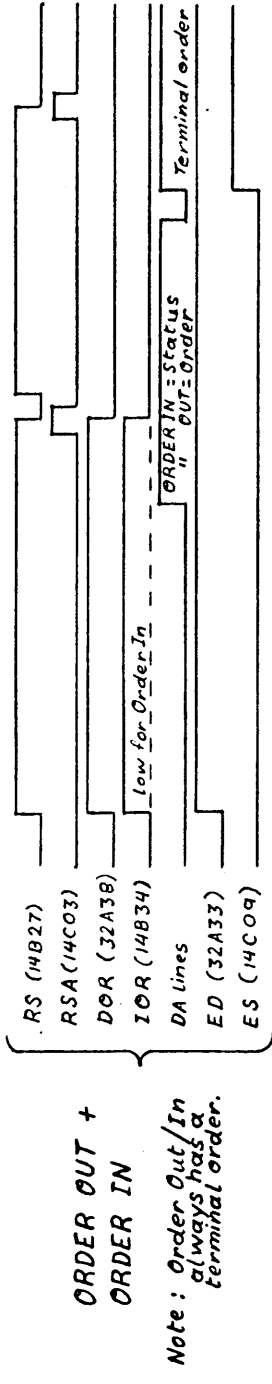
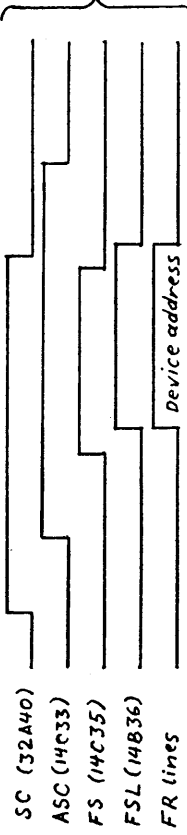
SIO, TIO, HIO, TDV



AIO



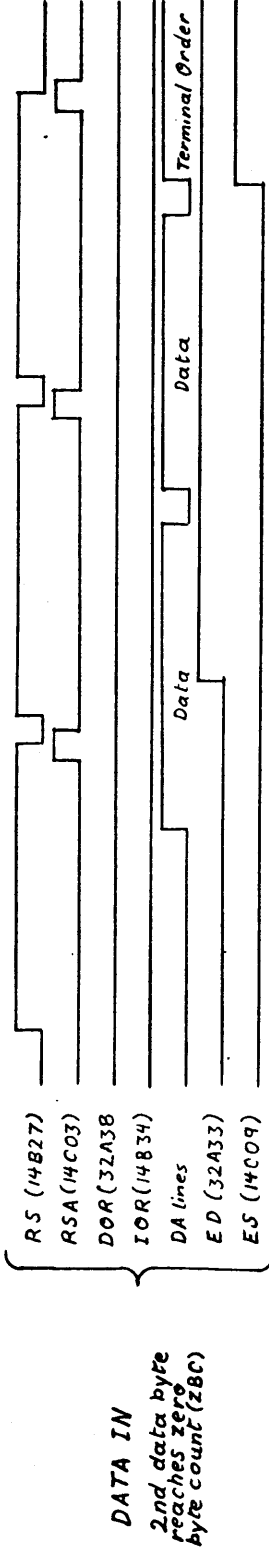
SERVICE CYCLE



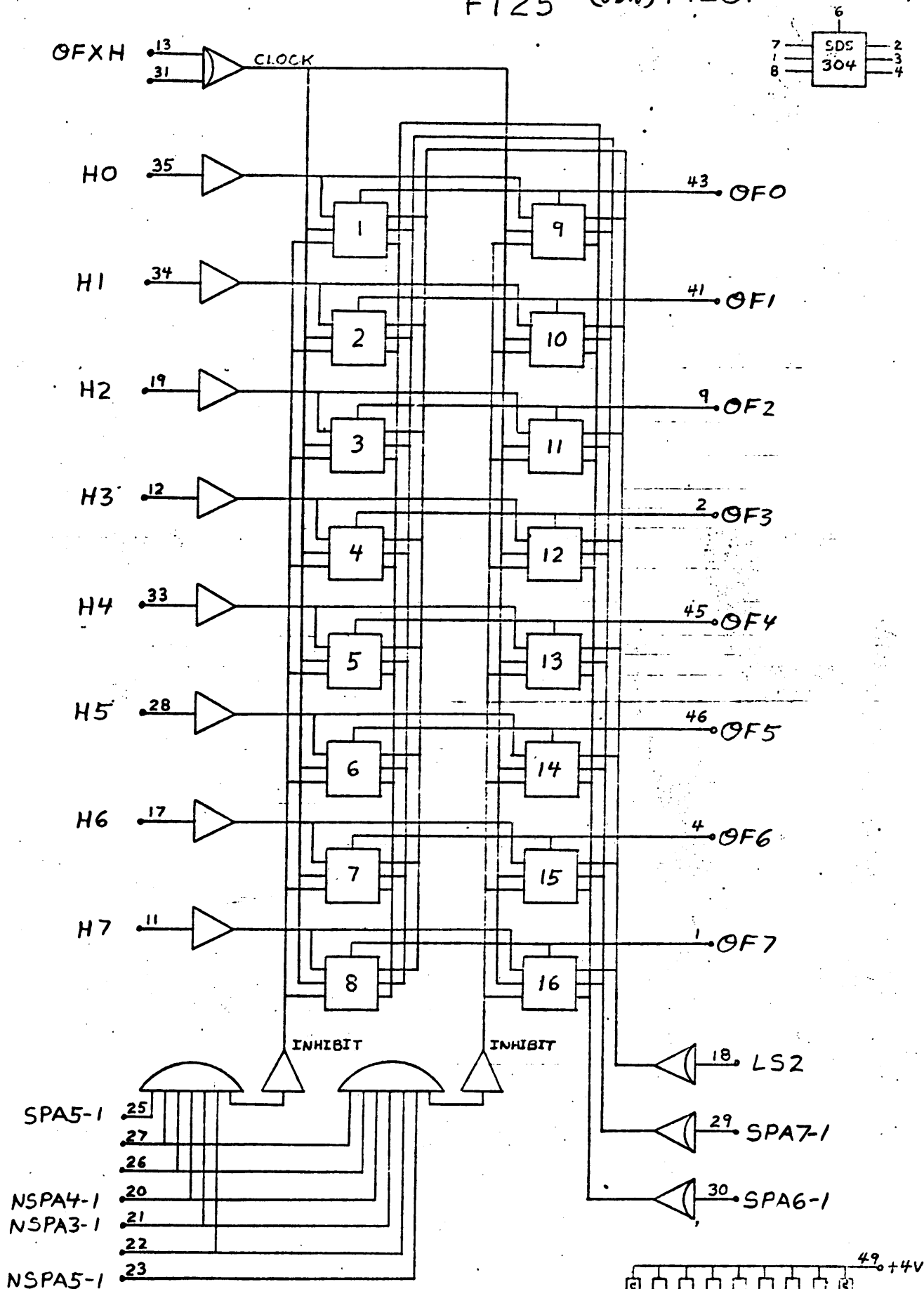
DATA OUT



DATA IN

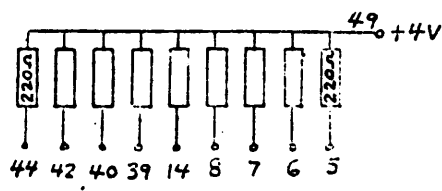


Note: Terminal Orders (ED.NES) are requested on errors, zero byte count, order in and order out.



SPA5-1 25
 27
 26
 NSPA4-1 20
 NSPA3-1 21
 22
 NSPA5-1 23

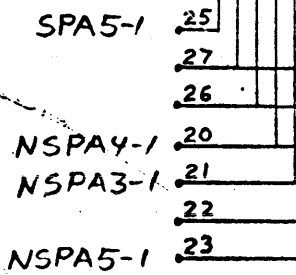
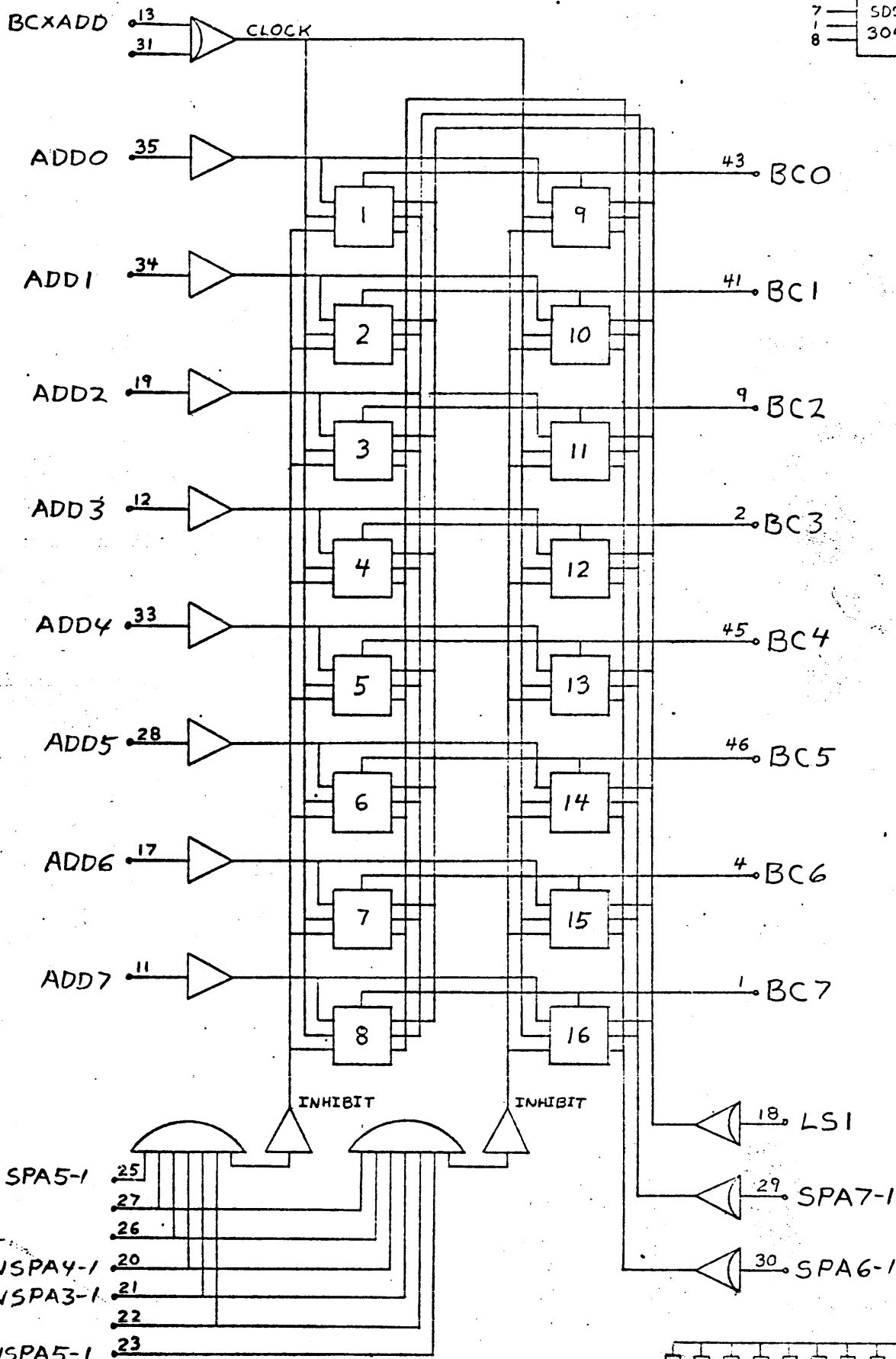
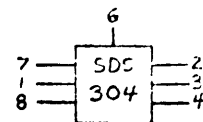
MIOP LS2= INTERRUPT STATUS
 Σ 5/7 NLS2= LSB of Byte Address
 IID f some flags



FT25

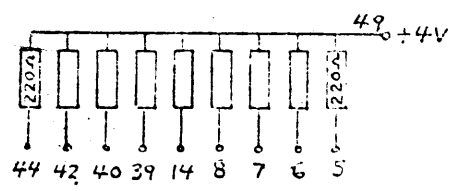
(8bit) MIOP

15D

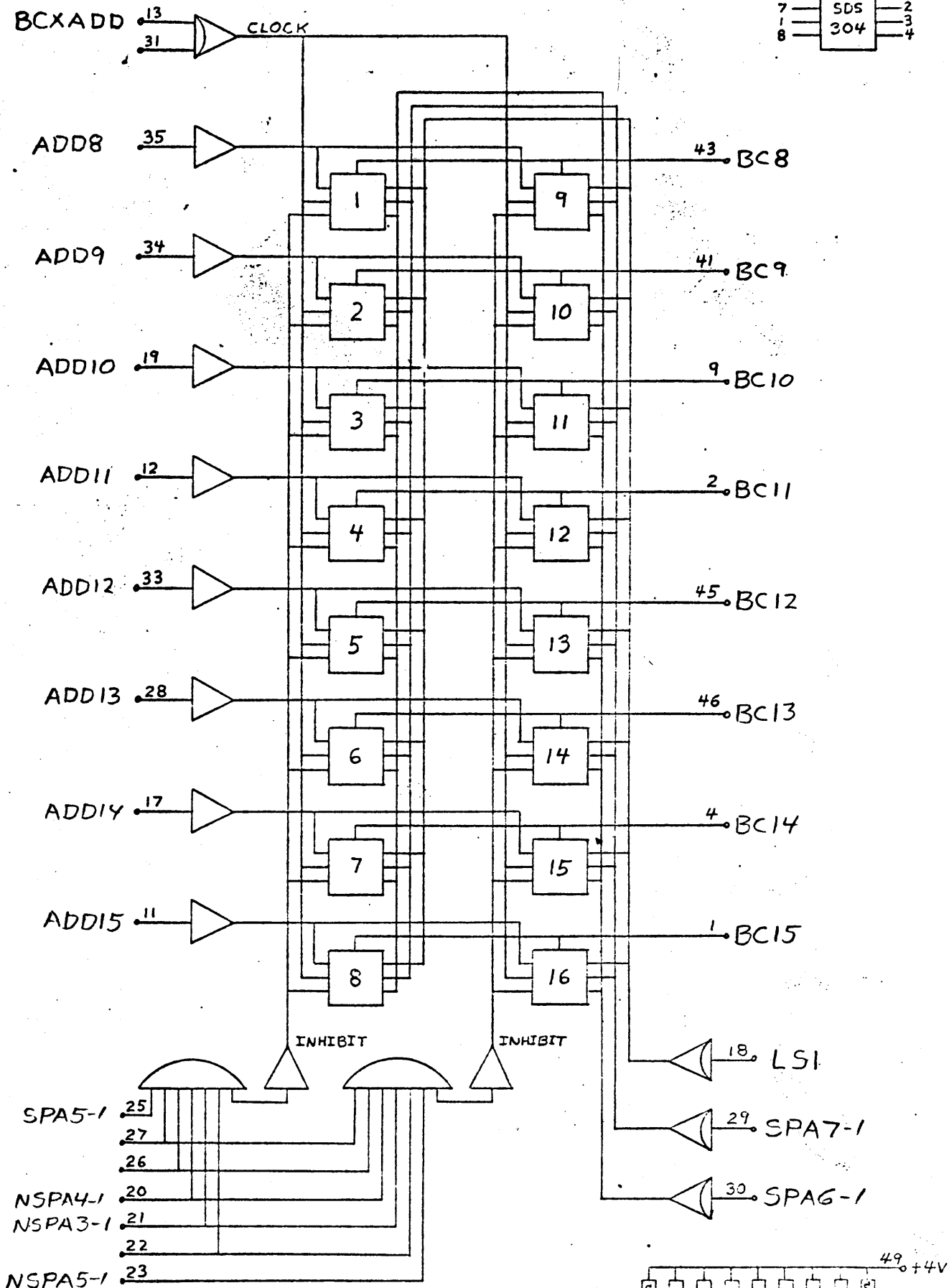
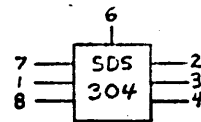


MIOP
Σ5/7
15D

LSI = FLAGS & STATUS
NLSI = BYTE COUNT



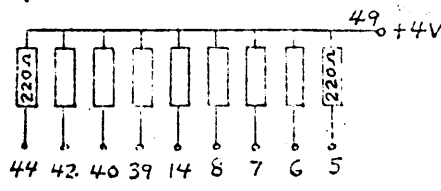
FT25 (8bit) MIOP 19D



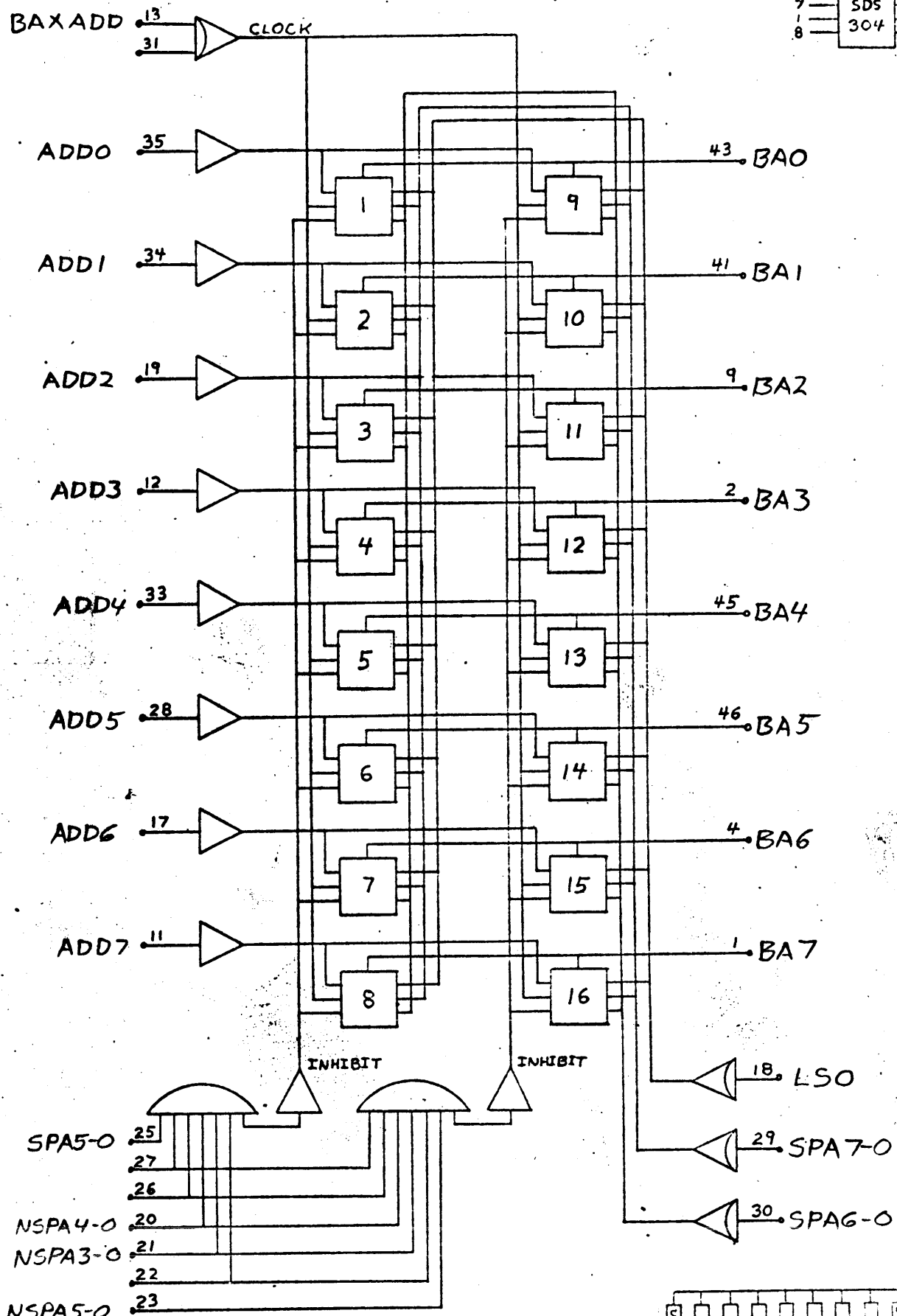
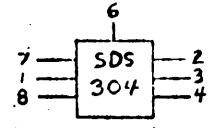
SPA5-1 25
 27
 26
 NSPA4-1 20
 NSPA3-1 21
 22
 NSPA5-1 23

MIOP
 25/7
 19D

LSI = FLAGS & STATUS
 NLSI = BYTE COUNT



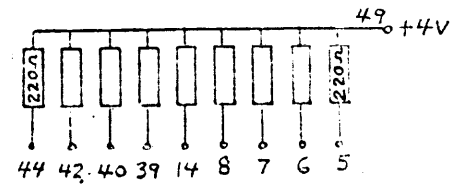
FT25 (8bit)MIOP 23D



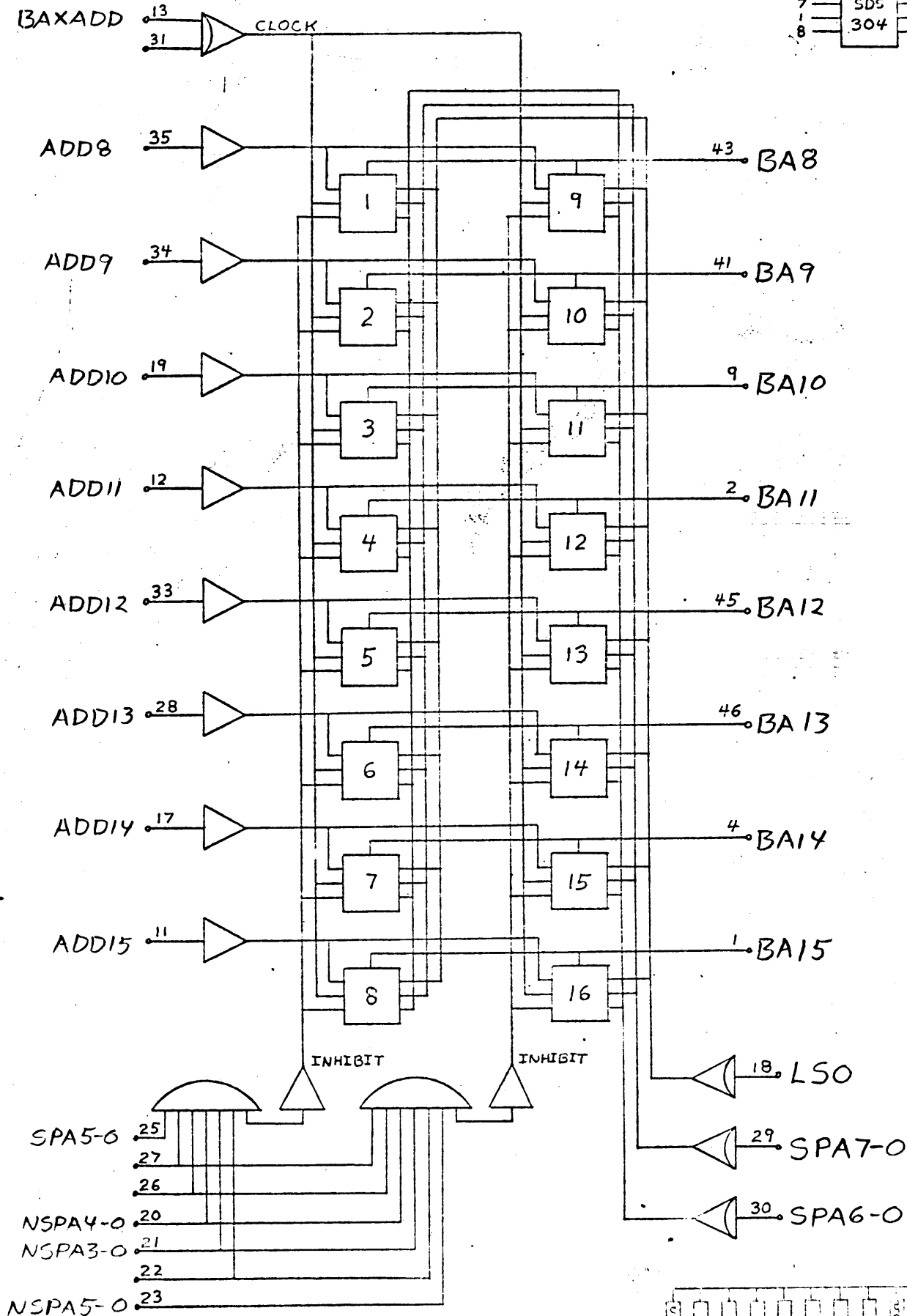
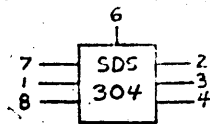
SPA5-0 25
 27
 26
 NSPA4-0 20
 NSPA3-0 21
 22
 NSPA5-0 23

MIOP
 Σ 5/7
 23D

LSO = COMMAND ADDRESS
 NLSO = BYTE ADDRESS

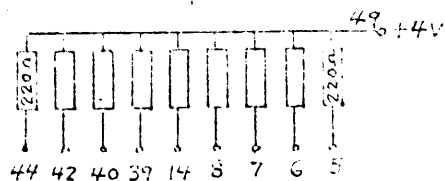


FT25^(8bit)MIOP 27D



MIOP
Σ 5/7
27D

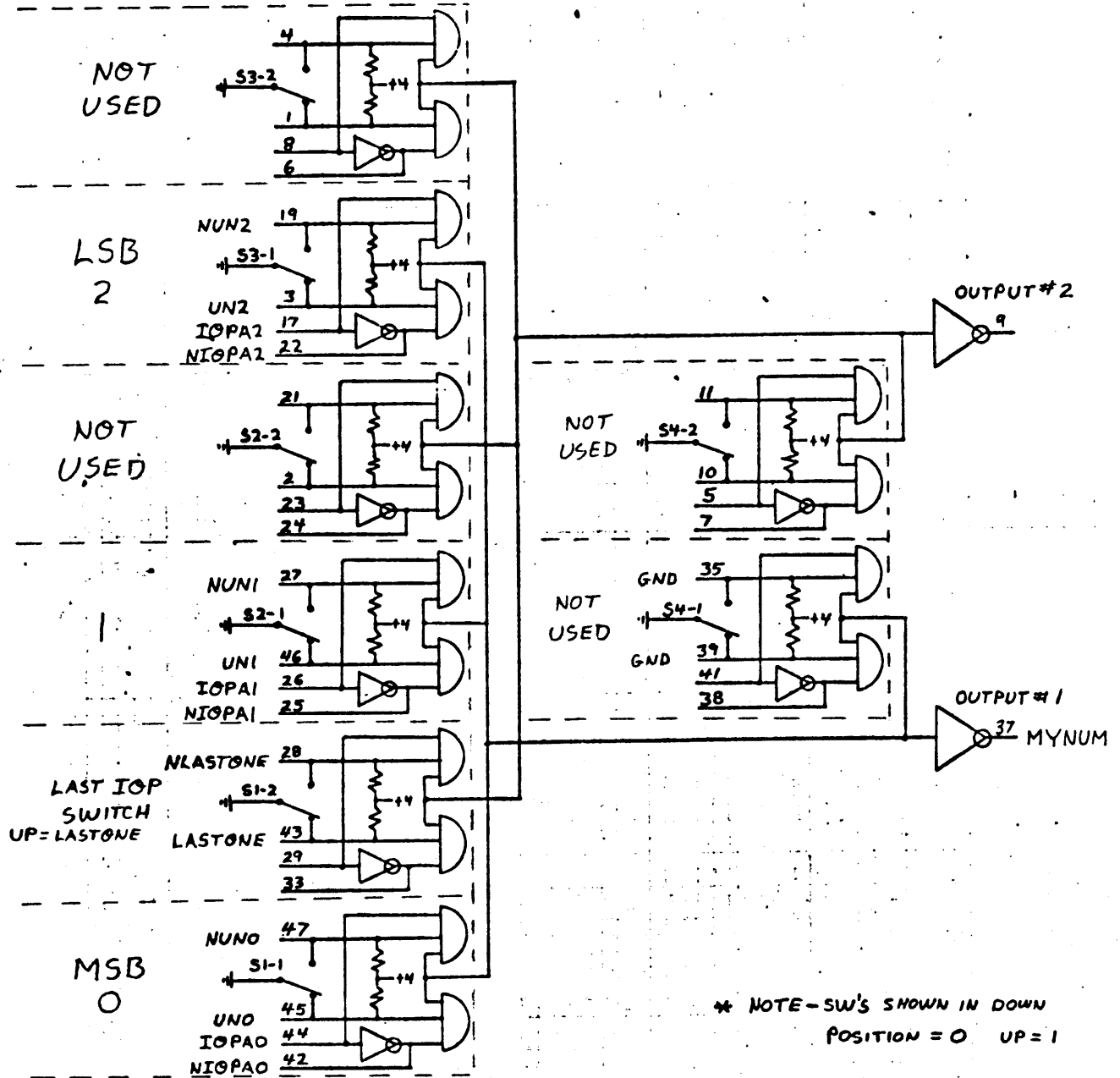
LSO=COMMAND ADDRESS
NLSO=BYTE COUNT



LT26

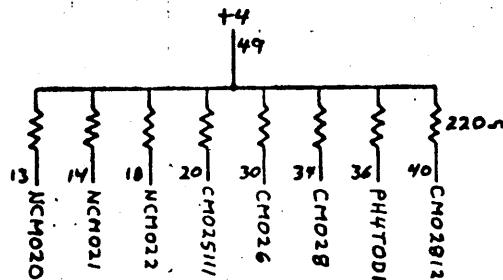
SWITCH MODULE (8bit) MIOP (13C)

COCIRANE



MSB	LSB
0	1 2

0 0 1 = 2nd. IOP



MIOP LT26 (13C)
SWITCH SETTING

BASIC (32 BIT) MIOP SEQUENCE OF EVENTS

SIO (START INPUT/OUTPUT)

1. CPU stores

{	Device Controller Address (M00 → M07)	}	in loc. 20.
	Command Doubleword Address (M16 → M31)		
	Number of status words to be returned (M08, M09)		
2. CPU sends

{	IOP number (IOPA0:R → IOPA2:R)	}	to the MIOP.
	Command to be executed (FNCO:R → FNC2:R)		
	and the Control Strobe (CNST:R)		
3. CPU waits for proceed (PR:R) from MIOP.
4. MIOP accesses loc. 20 (see 1.).
5. MIOP sends

{	Device Controller Address (M00 → M07)	}	to Device Controller.
	Command (FNDSIO:D)		
	Function Strobe (FS:D)		
6. Device Controller responds with FSL:R and holds Device Controller status on FR Lines (FRO:R → FR7:R).
7. MIOP's 1st status word

{	send the old Command Doubleword Address from CA register	}
	to location 20.	
8. MIOP stores new Command Doubleword Address in CA register.
9. MIOP's 2nd status word

{	Status off FR Lines (FRO:R → FR7:R)	}	is stored in location 21.
	Operational status from FS reg. (FS08 → 14)		
	Remaining byte count from BC reg.		
10. MIOP clears FS and OF reg. with successful SIO possible. NCC1.NCC2
11. MIOP sends proceed to CPU.
12. CPU takes status from locations 20 and/or 21 and stores it in its designated registers.

NOTE: If no status is asked for, none is sent.

Service call for Order Out from Device Controller that received the SIO.

ORDER OUT

1. MIOP

{	Connects for service with Device Controller	}
	Receives Request Strobe (RS:D)	
	and determines Order Out Service Call (DOR:R, IOR:R)	

ORDER OUT (CONT'D.)

2. MIOP accesses 1st word of Command Doubleword with Command Doubleword Address in CA reg. (Order and Start Byte Address) or (Transfer In Channel and Command Doubleword Address).
3. MIOP
if not Transfer In Channel { sends order to Device Controller
stores Byte Address (M13 - 28) in BA reg.
and (M29 - 31) the 3 LSB. in OF reg.
(OFF0 → OF02).

if Transfer In Channel { stores new Command Doubleword
Address (M16 - 31) in CA reg.
and goes back to step 2.
4. MIOP { accesses 2nd word of Command Doubleword (Flags and Byte Count)
stores Byte Count in BC reg.
stores Flags in FS reg. (FS00 → FS07)
sets up OF reg. (OF03 - OF06) with Flags and a read reverse order.
5. MIOP { sends Terminal Order to Device Controller
updates operational status and
disconnects service from Device Controller with End Service (ES:D).

Service Call for Data Out from Device Controller assuming the order sent during Order Out was an output order.

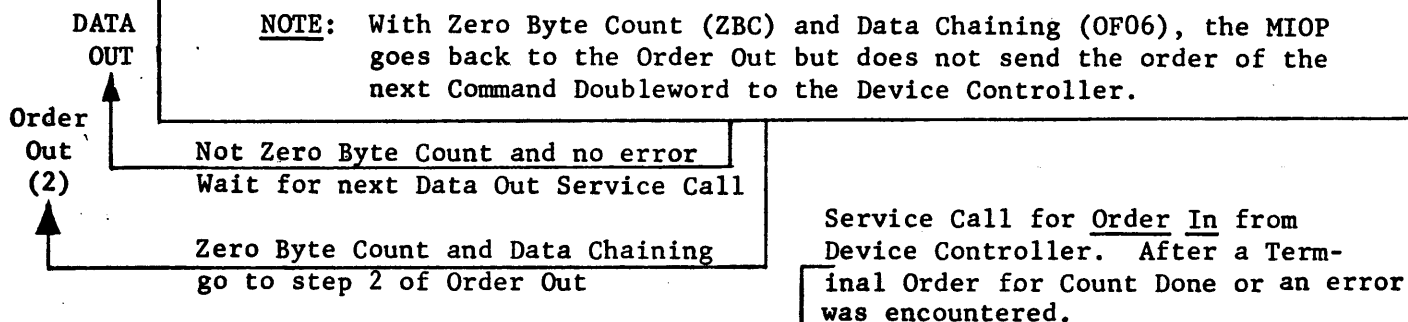
DATA OUT

1. MIOP { connects for service with Device Controller
receives Request Strobe (RS:D) and
determines Data Out Service Call from (NDOR:R.IOR:R)
2. MIOP with Byte Address received during Order Out access output data from Memory.
3. MIOP
1 Byte interface { sends 1 Byte at a time to Device Controller for every Request Strobe (RS:R).
4 Byte interface { sends 1 word at a time to Device Controller.
4. MIOP terminates data transfer (ED:D) if:
{ all data of accessed word has been transferred or
Device Controller sends End Data (ED:R) to MIOP or
Byte Count reaches zero (ZBC)

DATA OUT (CONT'D.)

5. For each Byte transferred:
 - 1 Byte interface { the Byte Count (BC reg.) is decremented by 1.
the Byte Address is incremented by 1.
 - 4 Byte interface { the Byte Count (BC reg.) is decremented by 4.
the Byte Address is incremented by 4.
6. MIOP sends Terminal Order to Device Controller and updates status if:
 - an error (EH) was encountered
 - Zero Byte Count (ZBC) not Data Chaining was reached.
7. MIOP disconnects service from Device Controller (ES:D).

NOTE: With Zero Byte Count (ZBC) and Data Chaining (OF06), the MIOP goes back to the Order Out but does not send the order of the next Command Doubleword to the Device Controller.



ORDER IN

1. MIOP { connects for service with Device Controller
receives Request Strobe (RS:R) and
determines Order In Service Call (DOR:R.NIOR:R).
2. MIOP accepts order from Device Controller.
3. MIOP updates its status (FS and IS reg.).
4. MIOP sends Terminal Order (TORD) to Device Controller.
5. MIOP disconnects service from Device Controller (ES:D).

NOTE: If Command Chaining (02:D) was sent to the Device Controller during the Terminal Order, the Device Controller should come back with a Service Call for Order Out. If not, another SIO must be issued by the CPU for any further operation.

Order Out

DATA IN

1. Data In is equal to Data Out except that data is received by MIOP.

TIO (TEST INPUT/OUTPUT)

1. TIO is the same as SIO except for steps 7 and 11 and no Order Out Service Call is sent in response.

TDV (TEST DEVICE)

1. TDV is the same as TIO except that the status off FR Lines is unique to Device.

HIO (HALT DEVICE)

1. HIO is the same as TIO except the Device must stop all operations.

AIO (ACKNOWLEDGE INPUT/OUTPUT INTERRUPT)

1. CPU sends

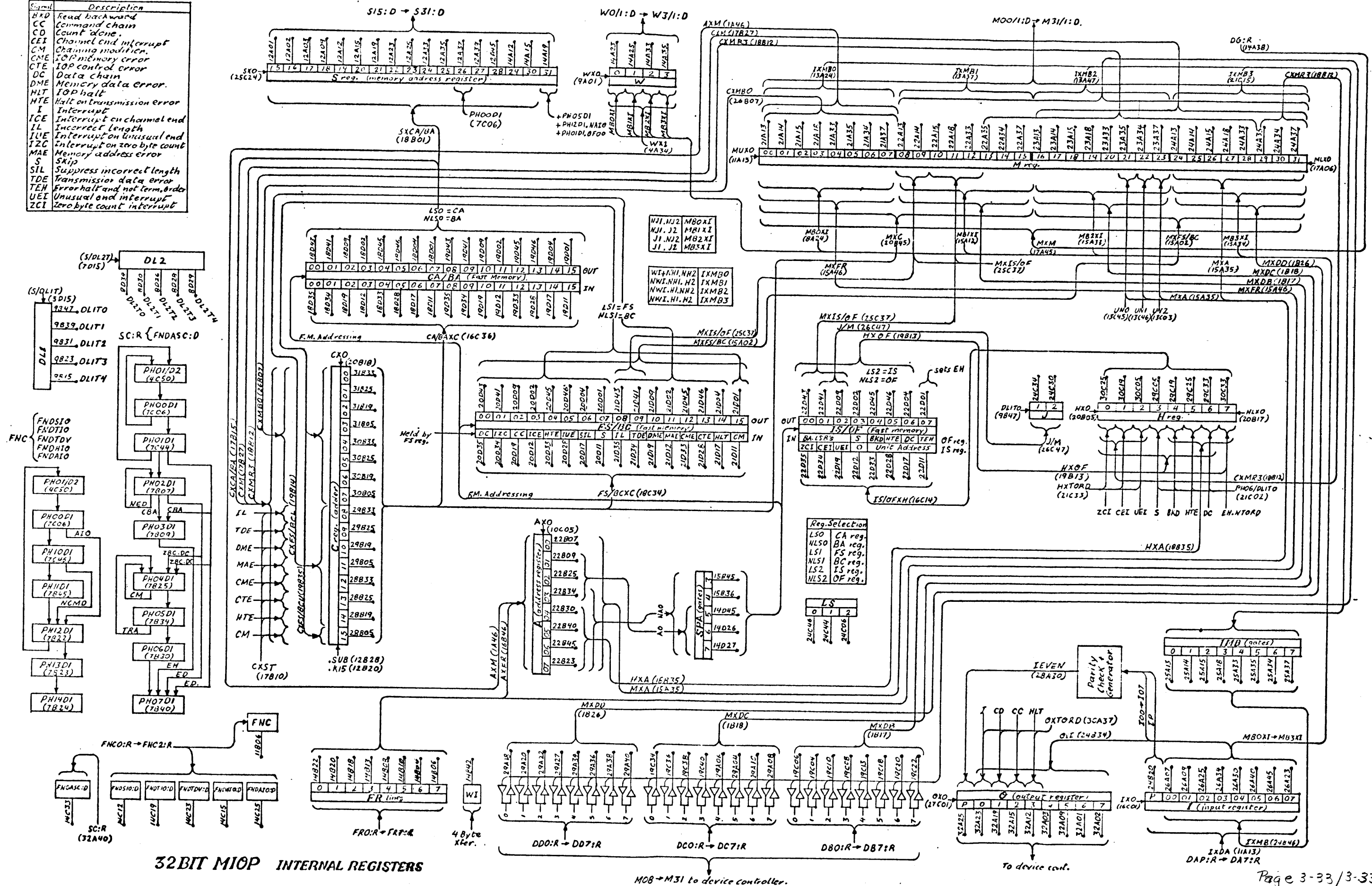
{	command to be executed (FNC0:D - FNC2:D) to MIOP.
	Control Strobe (CNST:R)
2. CPU waits for Proceed (PR:D).
3. MIOP sends

{	AIO Command (FNDAIO:D) to Device Controller.
	Function Strobe (FS:D)
4. Device Controller responds with:

{	FSL:R
	its address on FR Lines
	status unique to Device on data lines
5. MIOP takes

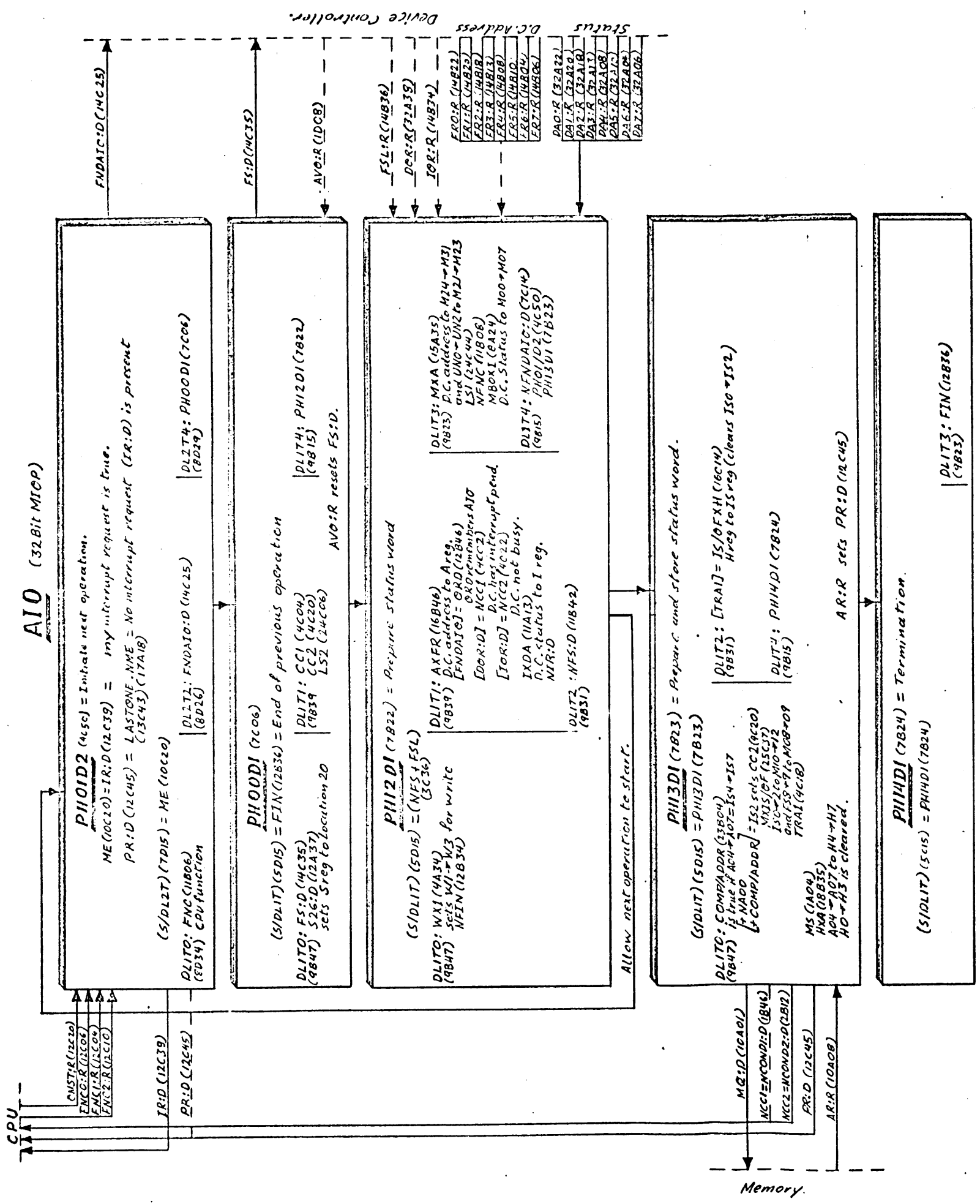
{	Device Address off FR Lines (FRD:R → FR7:R)	} and	
	its own address off its switches (UN0 → UN2)		store
	status unique to Device off Data Lines		it
	interrupt status from IS register (IS00 → IS02)		into
operational status from FS reg. (FS08 - FS09)		loc. 20	
6. MIOP sends Proceed to CPU.
7. CPU takes the status from location 20 and stores it in its designated register.

Signal	Description
BAO	Read backward
CC	Command chain
CD	Count done
CEI	Channel end interrupt
CM	Channel modification
CME	ICP memory error
CTE	IOP control error
DC	Data chain
DME	Memory data error
HLT	IOP halt
HTE	Halt on transmission error
I	Interrupt
ICE	Interrupt on channel end
IL	Interrupt length
IUE	Interrupt on unusual end
IJC	Interrupt on zero byte count
MAE	Memory address error
S	Skip
SIL	Suppress incorrect length
TDE	Transmission data error
TEH	Error half and not term. byte
UEI	Unusual end interrupt
ZCI	Zero byte count interrupt

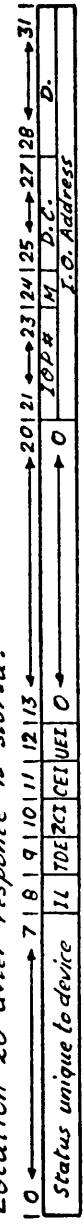


32 BIT MIOP INTERNAL REGISTERS

M08 → M31 to device controller.



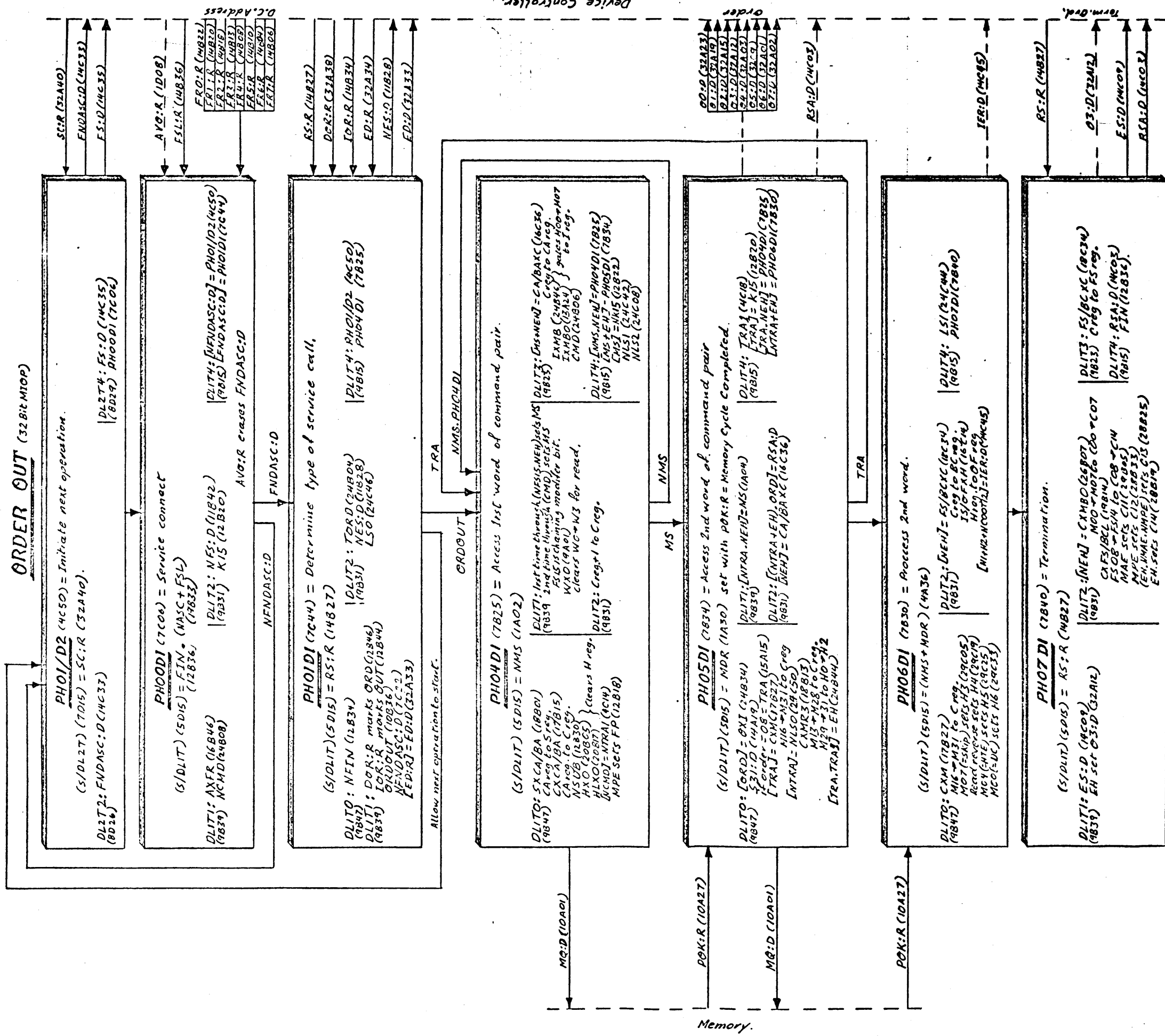
Location 20 after response is stored.



- CEI = Channel end interrupt
- IL = Incorrect length
- TDE = Transmission data error
- UEI = Unusual end interrupt.
- ZCI = Zero byte count interrupt
- D. = if M_i = 0 then D_i = device controller number. if M_i = 1 then D_i = unit number.
- D.C. = multiunit device controller number.
- M. = if 0 means single unit device. if 1 means multiunit device.

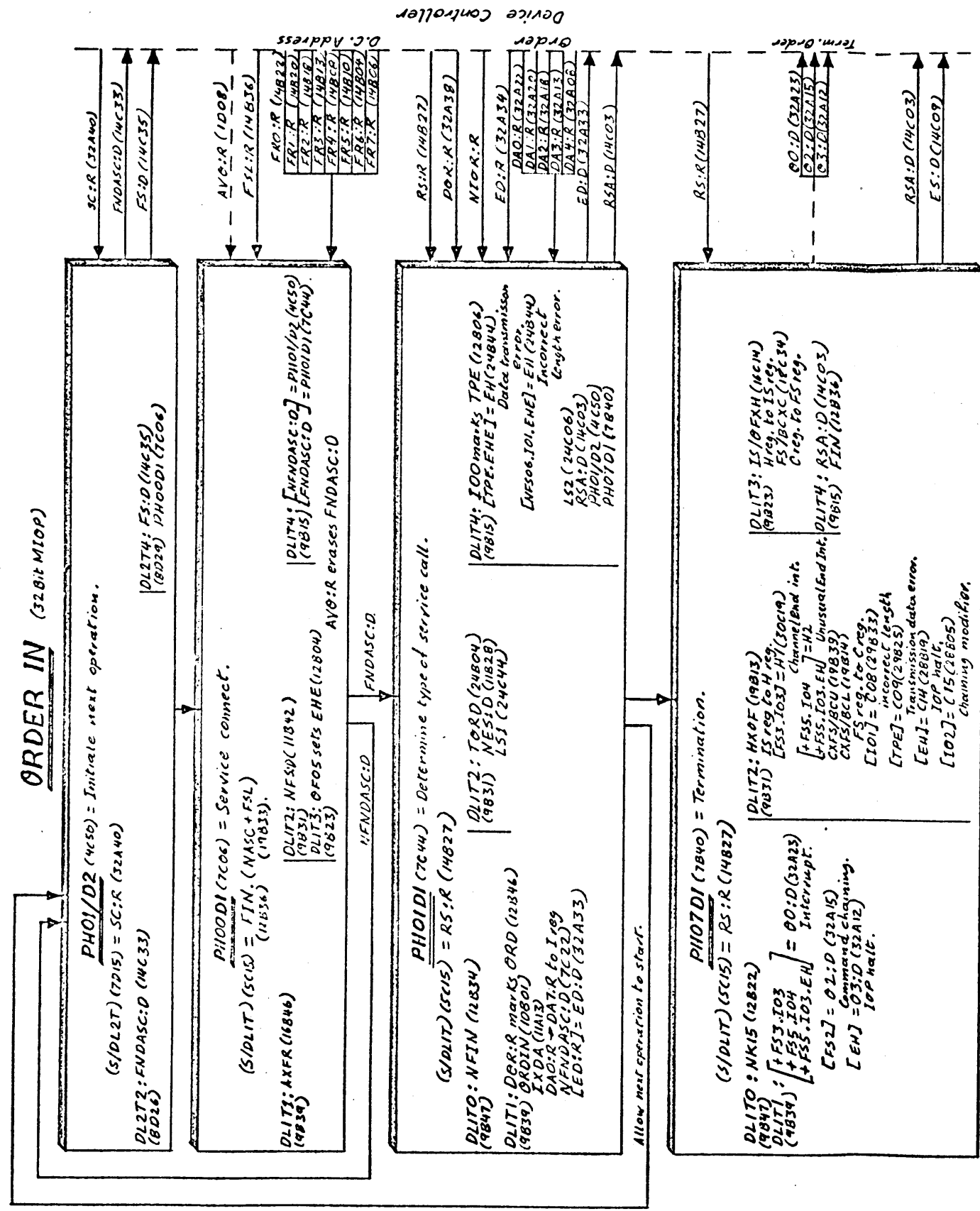
Note: Every PH1I4D1/02 term is reset at T3 time of its delay line. Every PH1I02/02 term is set at T1 time of its delay line and reset at T0 time of its delay line.

ORDER OUT (32 bit MOP)



Note: Every PH# DI/D2 is reset at T3 time of its delay line.
 Every PH# PD1/D2 is set at T1 time of its delay line and reset at T0 time of its delay line.

ORDER IN (32-bit M10P)

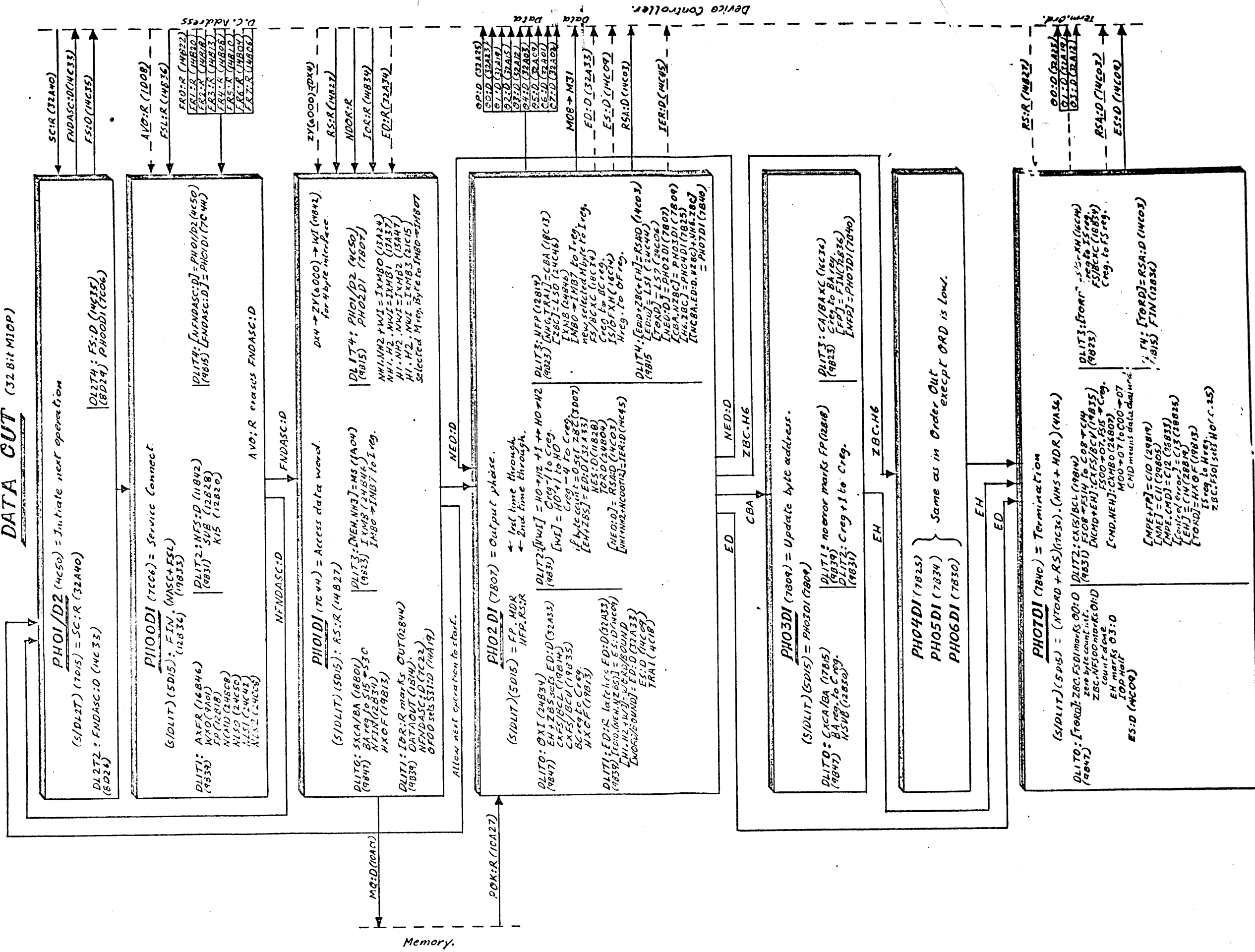


*Note: Every PHO1D1/D2 is reset at T3 time of its delay line.
Every PHO1D1/D2 is set at T1 time of its delay line and reset at T0 time of its delay line.*

ORDER

- DAO:R = Transmission error
- DA1:R = Incorrect length
- DA2:R = Chaining modifier
- DA3:R = Channel end.
- DA4:R = Unusual end.

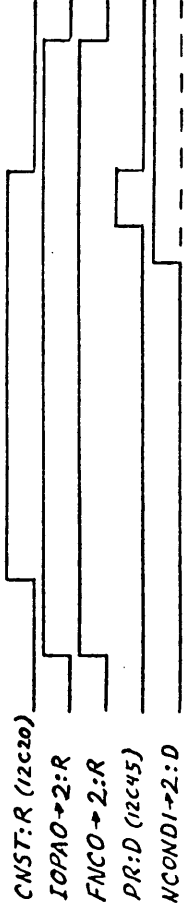
DATA OUT (32 Bit M10P)



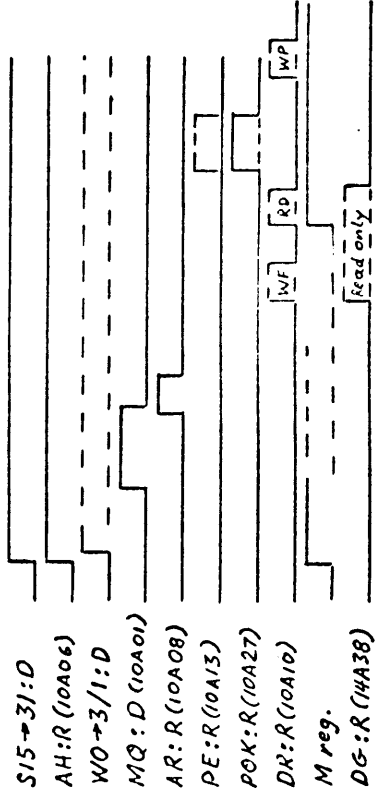
Note: Every PH01/D2 term is reset at T3 time of its delay line. Every PH02/D2 term is reset at T1 time of its delay line and reset at T0 time of its delay line.

MIOP Interfaces (32bit)

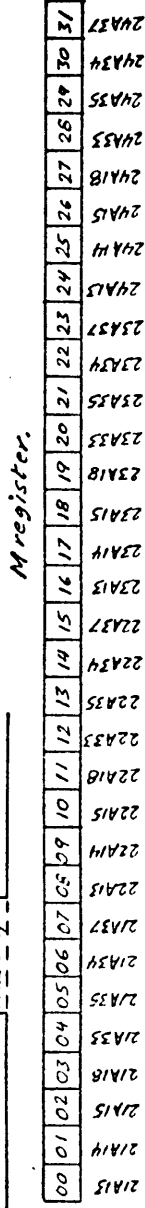
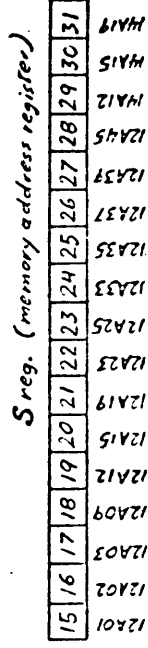
CPU / MIOP



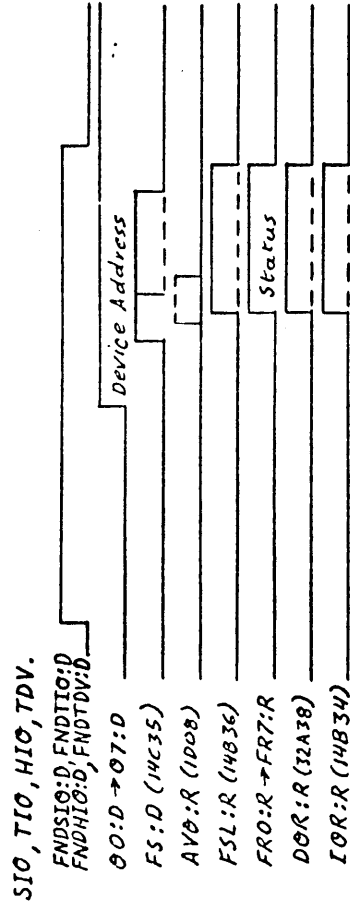
MEMORY / MIOP



TOPAO:R (12C08) FNCO:R (12C0E)
 TOPAI:R (12C13) FNCI:R (12C04)
 TOPAZ:R (12C18) FNC2:R (12C10)
 NCONDI:D (12C25) WO1:D (14A23)
 NCONDI2:D (12C33) W11:D (14A25)
 W21:D (14A33)
 W31:D (14A35)



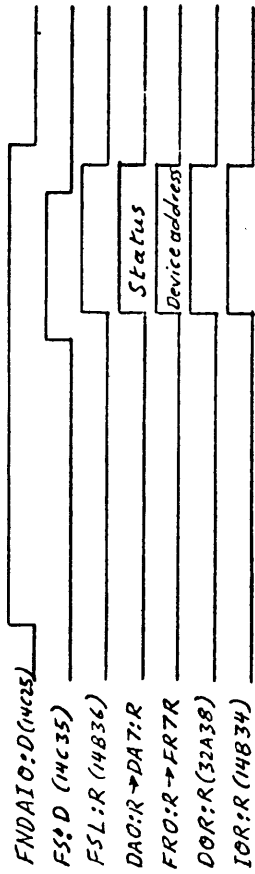
DEVICE CONTROLLER / MIOP



SIO, TIO, HIO, TDV.

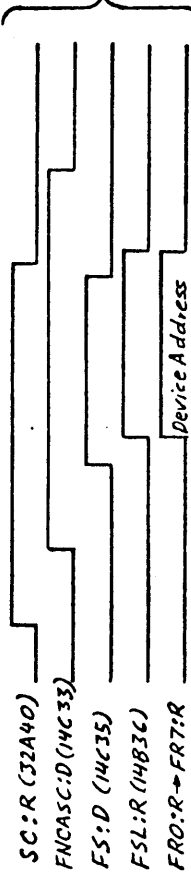
FNDHIO:D, FNDTIO:D
 FNDTIO:R
 FS:D (14C35)
 AVB:R (10A08)
 FSL:R (14B36)
 FRO:R -> FRT:R
 DOR:R (32A38)
 IOR:R (14B34)

AIO



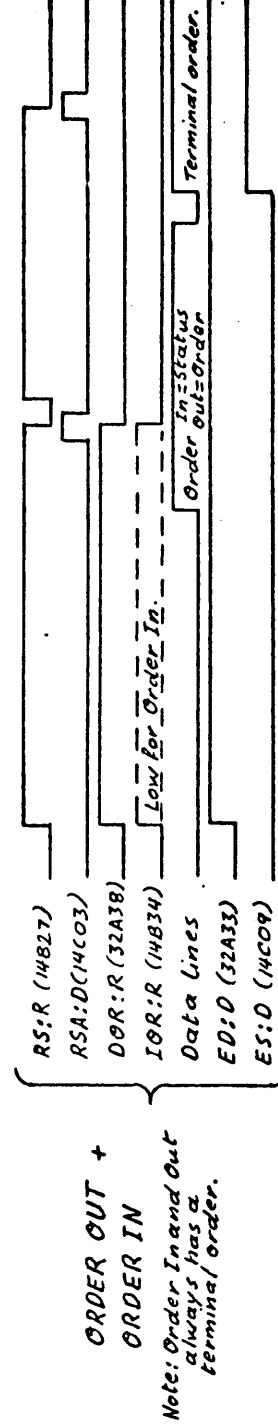
FNDAT0:D (14C25)
 FS:D (14C35)
 FSL:R (14B36)
 DAO:R -> DAT:R
 FRO:R -> FRT:R
 DOR:R (32A38)
 IOR:R (14B34)

SERVICE CYCLE



SC:R (32A40)
 FNASC:D (14C33)
 FS:D (14C35)
 FSL:R (14B36)
 FRO:R -> FRT:R

SERVICE CONNECTION

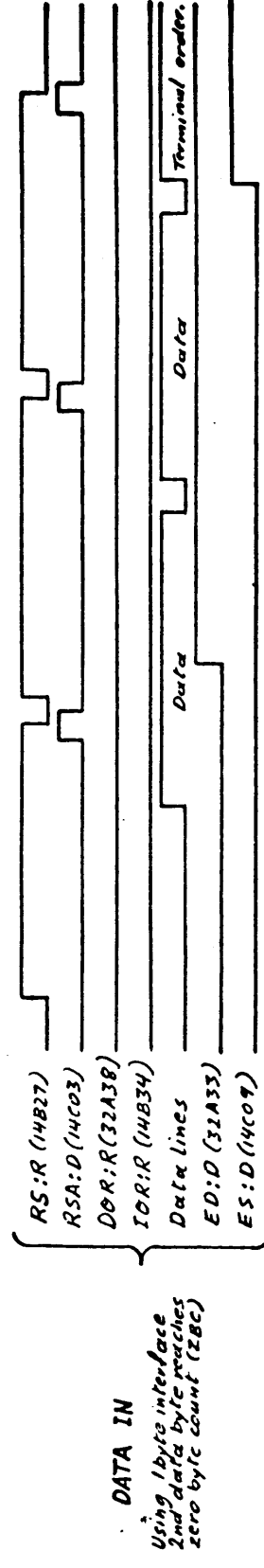


ORDER OUT +
 ORDER IN

Note: Order In and Out always has a terminal order.

DATA OUT

Using 4byte interface



DATA IN

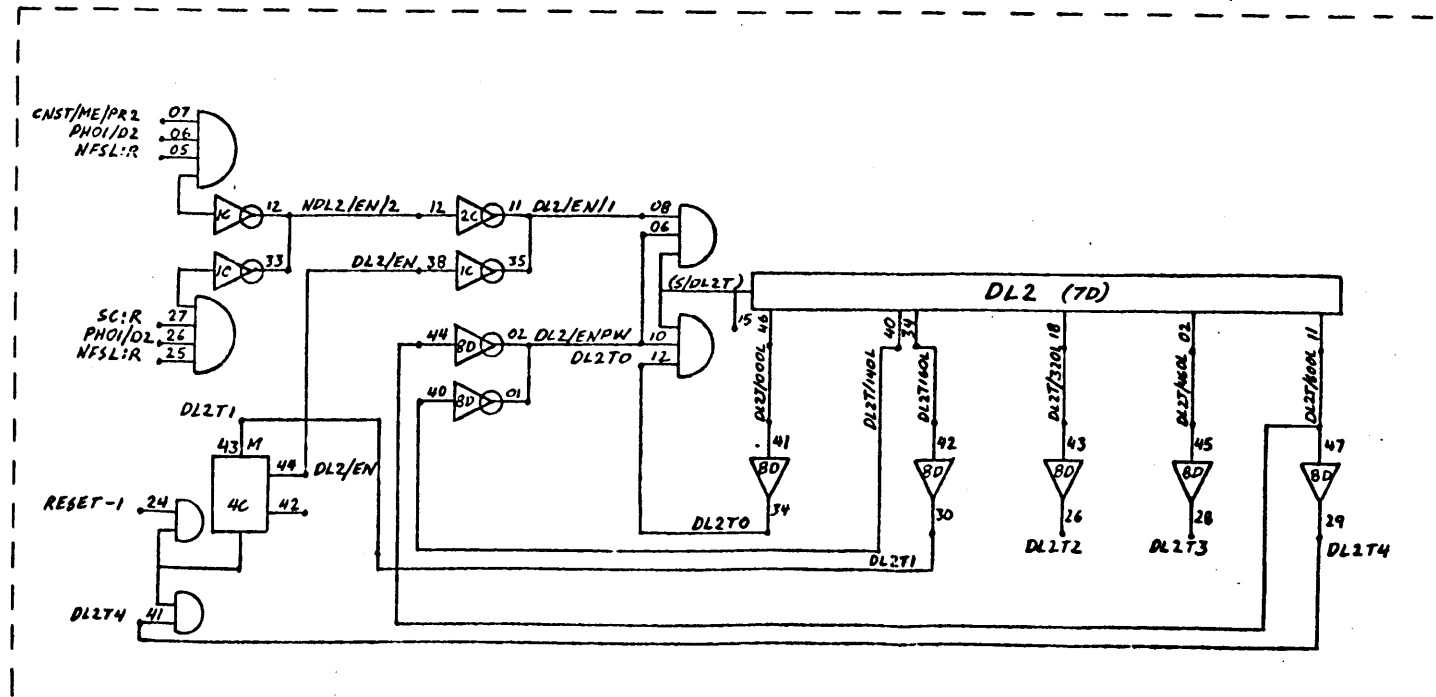
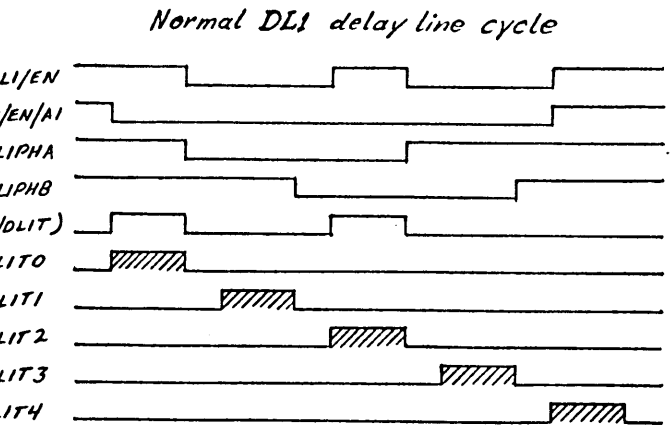
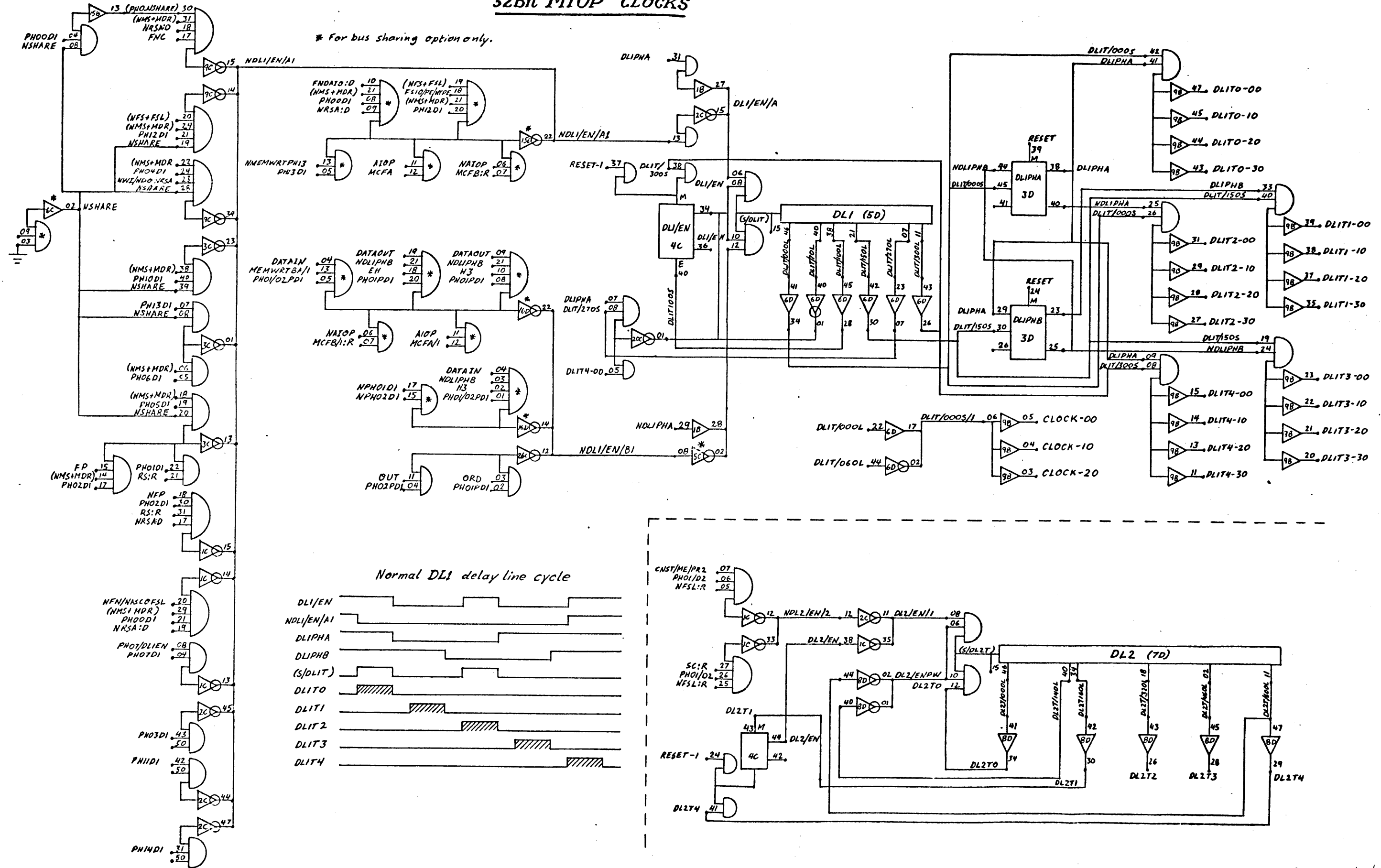
Using 1byte interface
 2nd data byte reaches zero byte count (ZBC)

OUT		DATA		IN	
00:D	32A25	DAP:R	32A27	DA0:R	32A22
01:D	32A19	DA1:R	32A20	DA2:R	32A18
02:D	32A15	DA3:R	32A17	DA4:R	32A08
03:D	32A09	DA5:R	32A06	DA6:R	32A04
04:D	32A03	DA7:R	32A02	DA8:R	32A06
05:D	32A01	DB0:R	19C02	DB1:R	19C04
06:D	19C02	DB2:R	19C04	DB3:R	19C06
M08	19C01	DB4:R	19C03	DB5:R	19C05
M09	19C04	DB6:R	19C02	DB7:R	19C02
M10	19C03	DC0:R	19C33	DC1:R	19C34
M11	19C03	DC2:R	19C35	DC3:R	19C36
M12	19C12	DC4:R	19C34	DC5:R	19C36
M13	19C15	DC6:R	29A01	DC7:R	29A06
M14	19C19	DD0:R	29A03	DD1:R	29A18
M15	19C23	DD2:R	29A09	DD3:R	29A20
M16	19C33	DD4:R	29A15	DD5:R	29A22
M17	19C35	DD6:R	29A19	DD7:R	29A22
M18	19C37	DD8:R	29A23	DD9:R	29A22
M19	19C39	DDA:R	29A25	DDB:R	29A37
M20	29A02	DDC:R	29A33	DDD:R	29A36
M21	29A01	DD4:R	29A35	DD5:R	29A36
M22	29A01	DD6:R	29A37	DD7:R	29A36
M23	29A03	DD8:R	29A39		
M24	29A15				
M25	29A19				
M26	29A23				
M27	29A25				
M28	29A33				
M29	29A35				
M30	29A37				
M31	29A39				

FNDHIO:D (14C15)
 FNDTIO:D (14C19)
 FNDTIO:R (14C12)
 FNDHIO:D (14C15)
 FNDAT0:D (14C25)

FRO:R (14B22)
 FRI:R (14B20)
 FR2:R (14B18)
 FR3:R (14B13)
 FR4:R (14B08)
 FR5:R (14B10)
 FR6:R (14B04)
 FRT:R (14B06)

32Bit MIOP CLOCKS

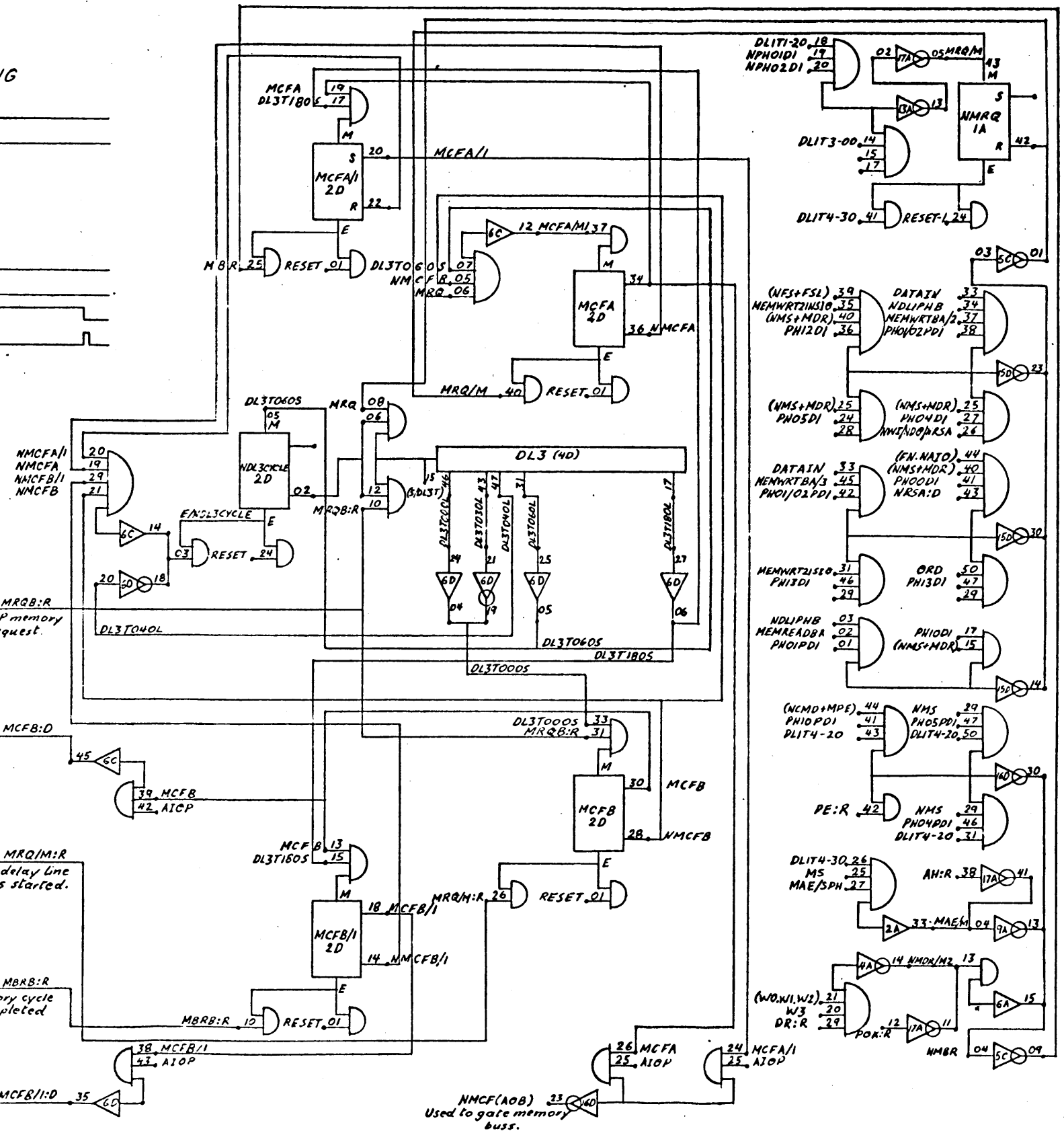
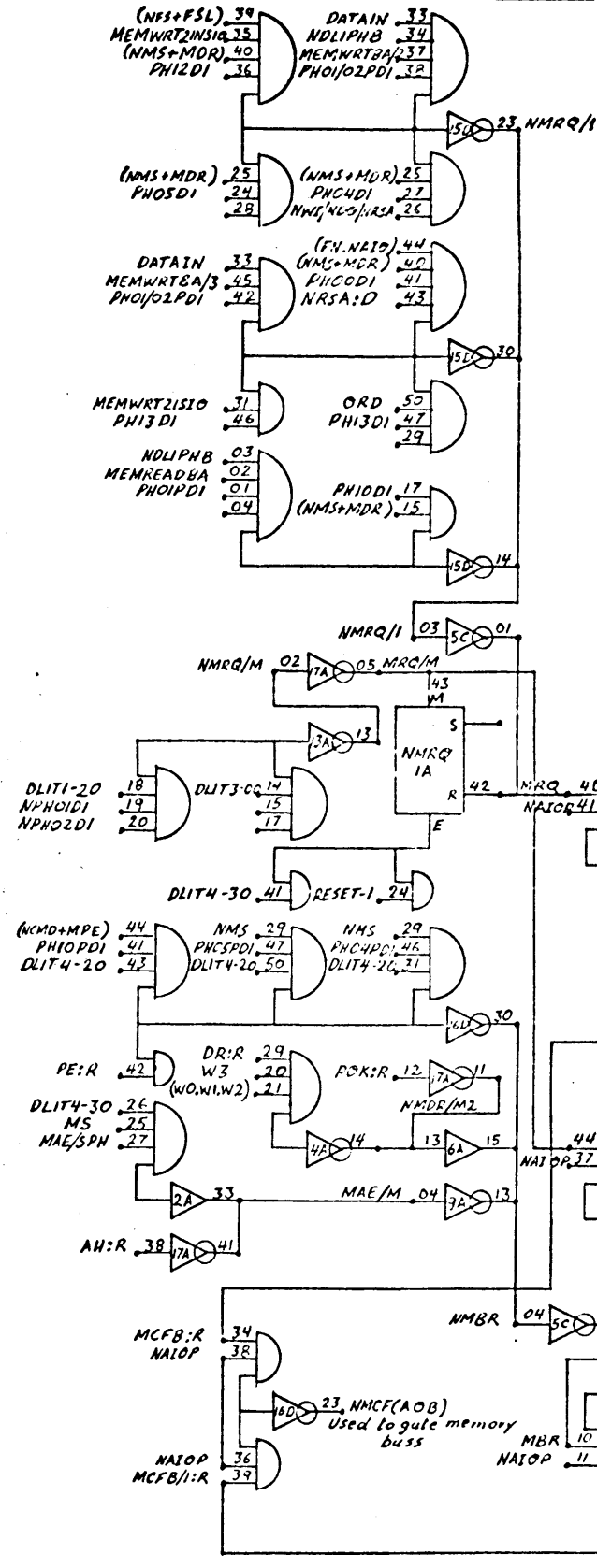
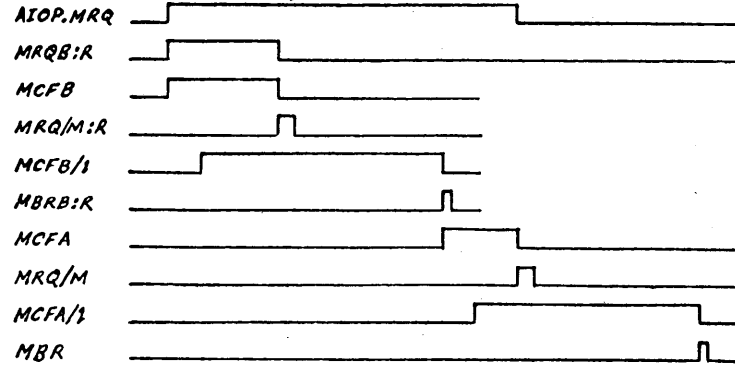


32BIT MIOP BUSS SHARING OPTION

NAIOP

AIOP

MEMORY CONTROL TIMING



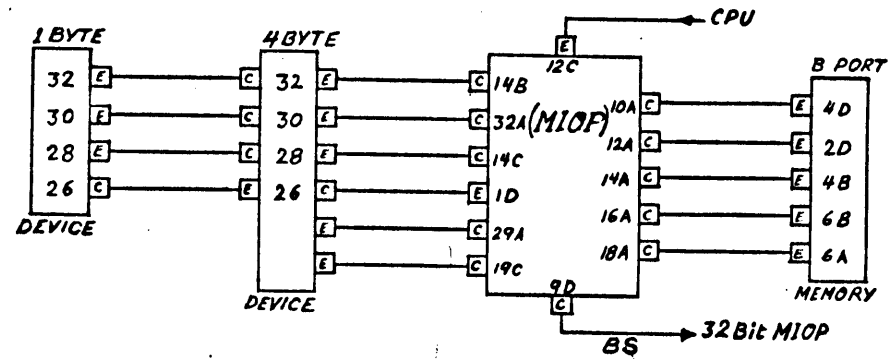
32 Bit MIOP (MODULE CHART)

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
A	AT11	FT65	LT13	AT11	LT12	FT27	FT65	FT63	FT63	FT63	FT63	FT63	XT10	FT27	AT11	IT16	AT11	BT11	AT70	LT13	AT61	IT11	AT11	IT11	LT13	XT10	BT16	BT16	IT11		BT11	FT66		
				4B																														
B	XT10	FT18	FT18	FT18	FT18	FT27	BT18	XT10	FT66	BT10	FT65	FT67	IT16	IT11	BT11	IT16	IT11	BT11	AT10		FT66	FT66	BT11	AT24	FT67	FT65	LT21	BT11	XT10	LT20	BT11	BT15		
C	FT26	FT26	FT18	FT18	XT10	IT11	LT13	LT13	FT66	IT11		BT11	LT13	AT11	IT11	IT11	IT11	XT10	AT12	LT26	AT13	IT11	BT17	IT11	XT10	FT66	BT25	IT15	FT66	LT13	IT16	IT11		
D	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	XT10	LT20	LT20	IT16					LT13	XT10	AT11	HT15	DT11	HT15	DT14	DT14	FT10	FT66	AT11
	2	2	2	2	2	1	1	1	1	1							BS	BS						BS			BS	BS			ABS	ABS		

Page 4-41

MIOP#	S1-1	S2-1	S3-1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

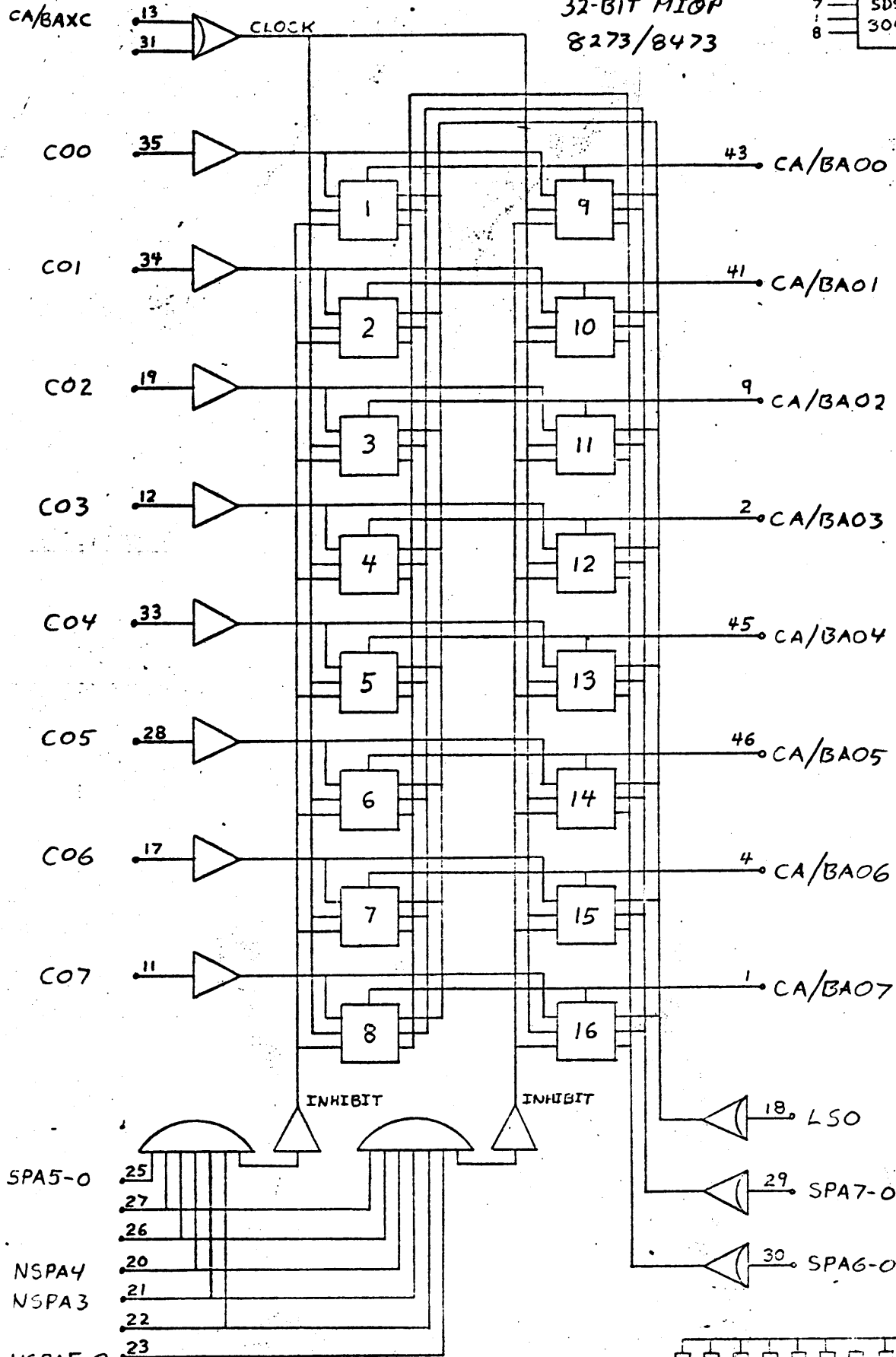
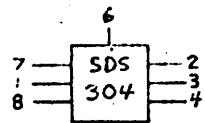
FOR: LASTONE → S1-2 UP
 FOURBYTE → S2-2 UP
 AIOP → S3-2 UP



- 1 : 8 Additional Channels. Channel 8 → 15
- 2 : 8 Additional Channels. Channel 16 → 23
- 4B : 4 Byte Option.
- BS : Memory Buss Sharing Option.
- ABS : Buss Sharing Option In AIOP Only.

FT25 (18D)

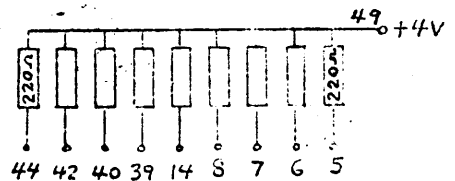
32-BIT MIOP
8273/8473



Σ5/7 32-BIT
MIOP

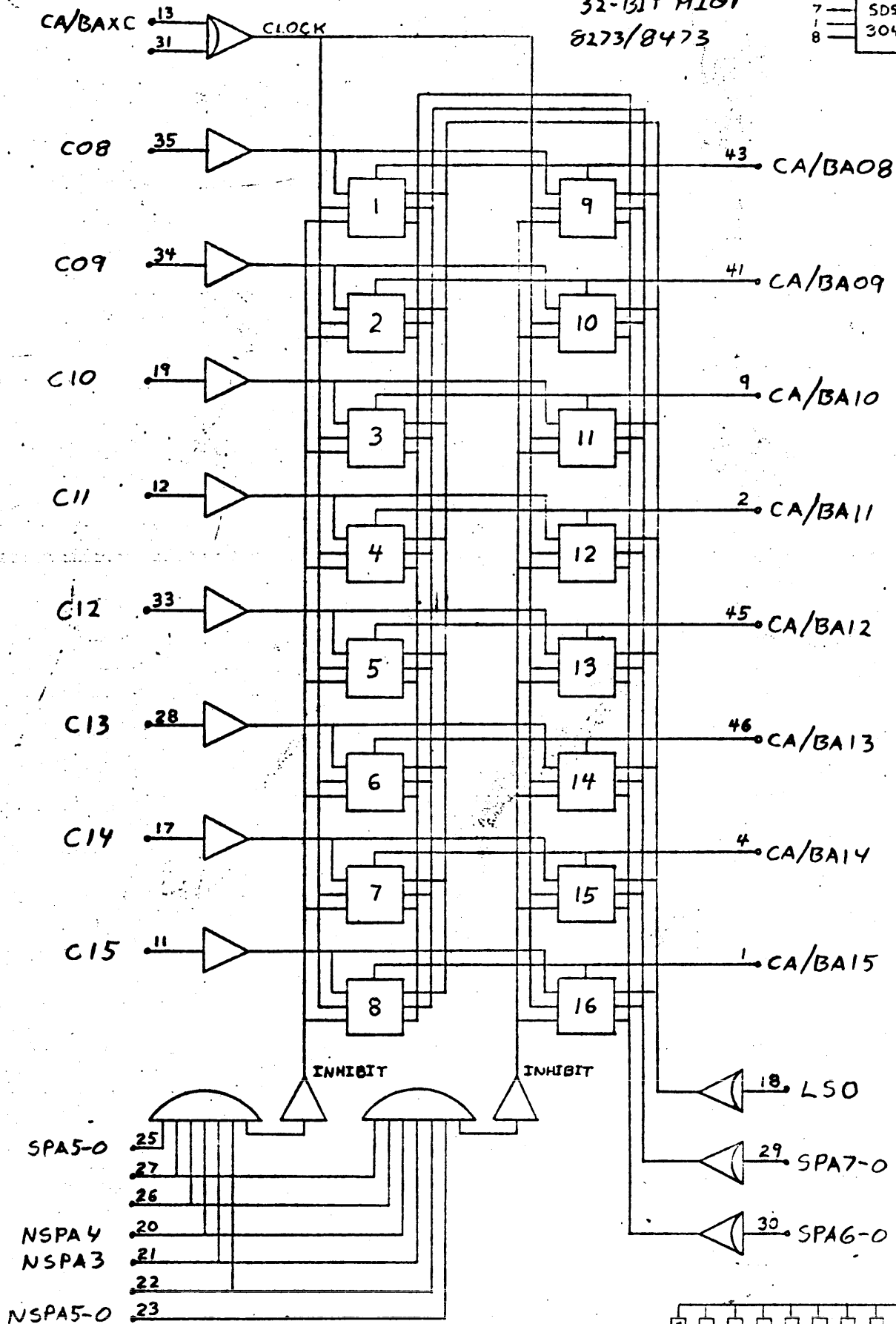
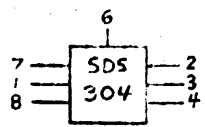
(CA) - LSO = COMMAND ADDRESS
(BA) - NLSO = BYTE ADDRESS

(18D)

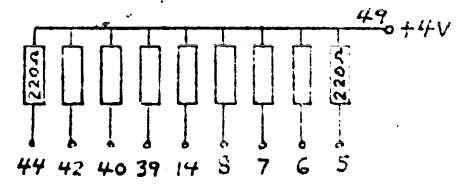


FT25 (19D)

32-BIT MIOP
8273/8473



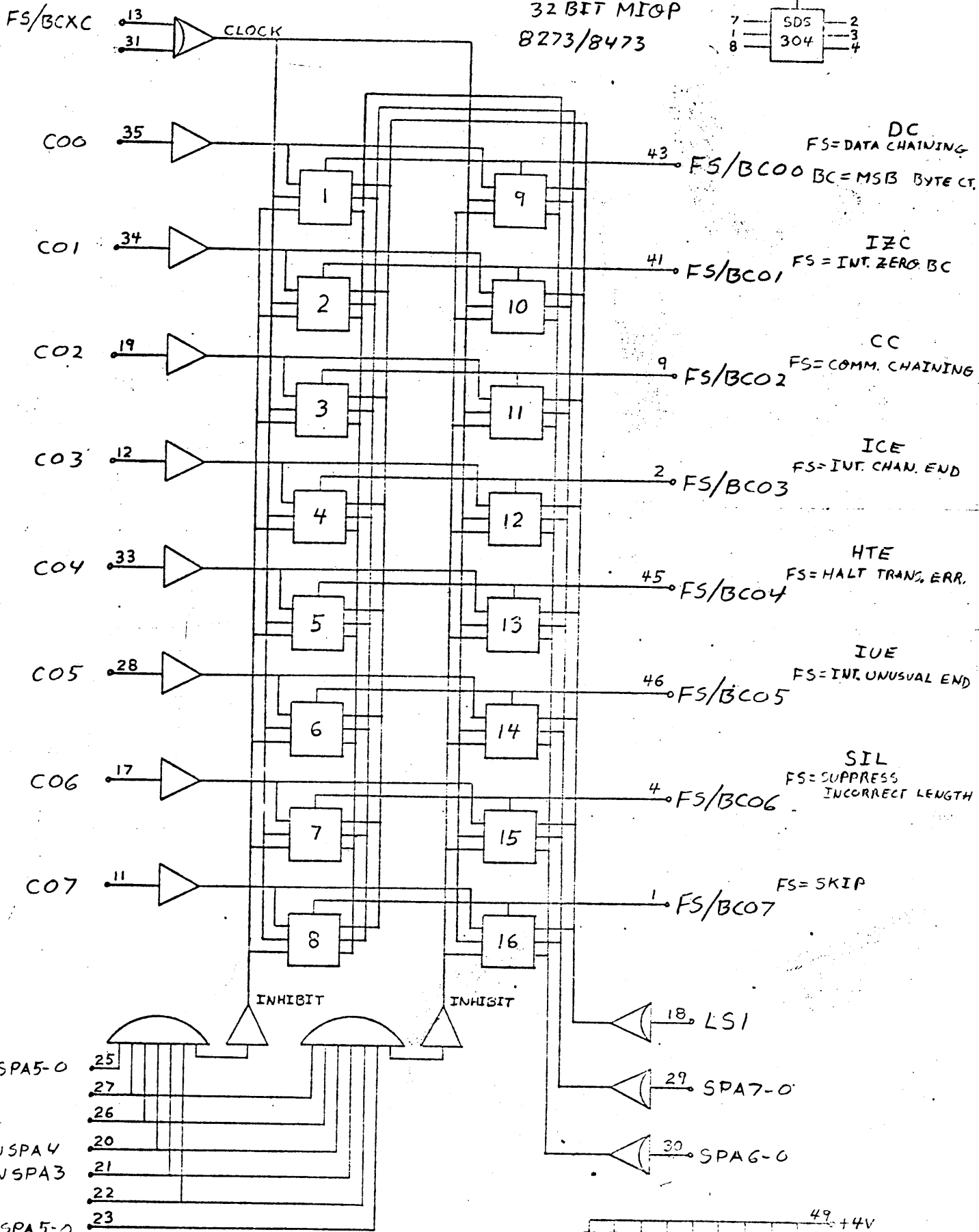
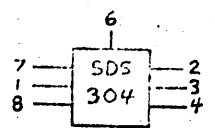
Σ5/7 32-BIT MIOP
(CA) - LSO = COMMAND ADDRESS
(BA) - NLSO = BYTE ADDRESS



(19D)

FT25 (20D)

32 BIT MIOP
8273/8473



DC
FS=DATA CHAINING
BC=MSB BYTE CT.

IZC
FS=INT. ZERO BC

CC
FS=COMM. CHAINING

ICE
FS=INT. CHAN. END

HTE
FS=HALT TRANS. ERR.

IUE
FS=INT. UNUSUAL END

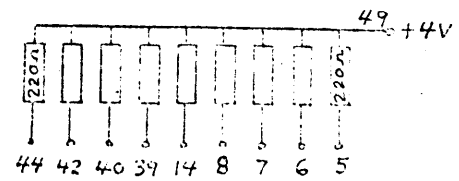
SIL
FS=SUPPRESS INCORRECT LENGTH

FS=SKIP

SPA5-0 25
27
26
NSPA4 20
NSPA3 21
NSPA5-0 22
23

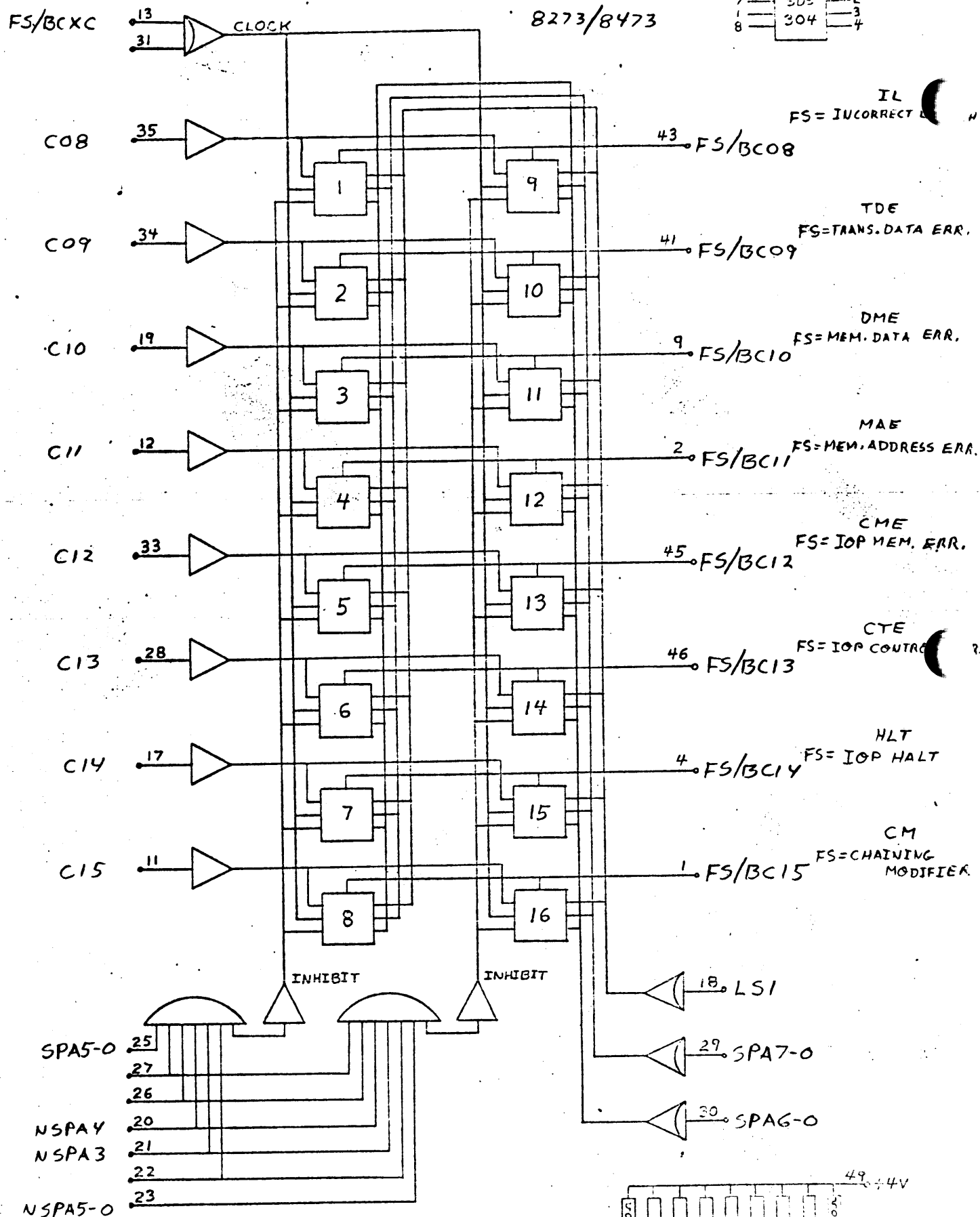
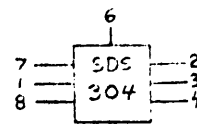
Σ5/7 32-BIT
MIOP

(FS)-LSI=FLAGS & STATUS
(BC)-NLSI=BYTE COUNT



(20D)

FT25 (21D)
32-BIT MIOP
8273/8473



IL
FS= INCORRECT L

TDE
FS= TRANS. DATA ERR.

DME
FS= MEM. DATA ERR.

MAE
FS= MEM. ADDRESS ERR.

CME
FS= IOP MEM. ERR.

CTE
FS= IOP CONTRA

HLT
FS= IOP HALT

CM
FS= CHAINING MODIFIER

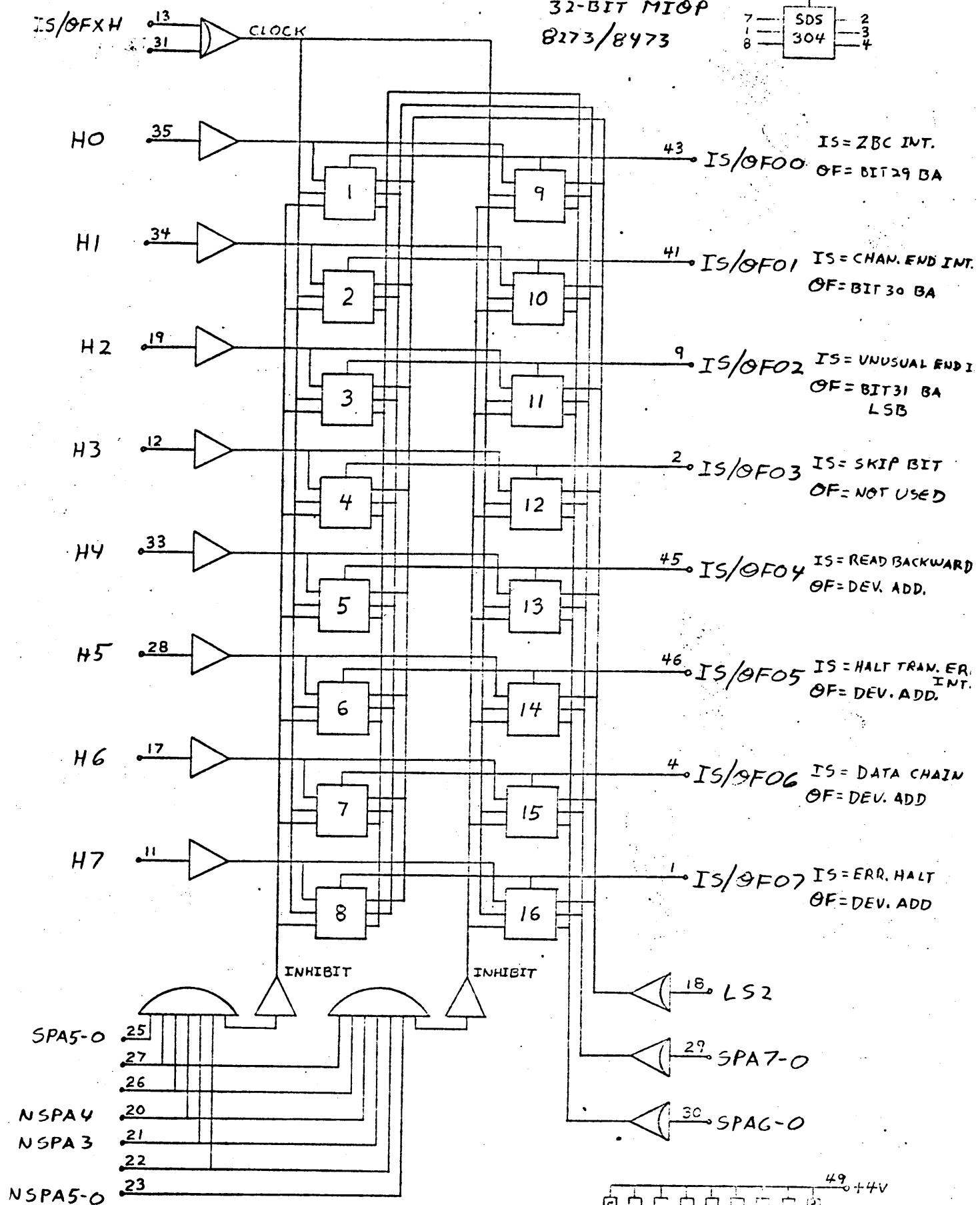
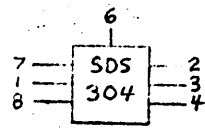
Σ5/7 32-BIT MIOP

(FS)- LSI= FLAGS & STATUS
(BC)- NLSI= BYTE COUNT

(21D)

FT25 (22D)

32-BIT MIOP
8273/8473



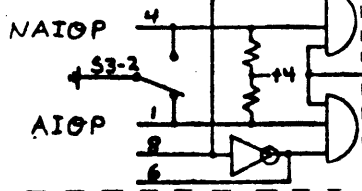
32-BIT
MIOP

(IS) - LS2 = INTERRUPT STATUS
(OF) - NLS2 = LSB OF BYTE ADDRESS
& SOME FLAGS

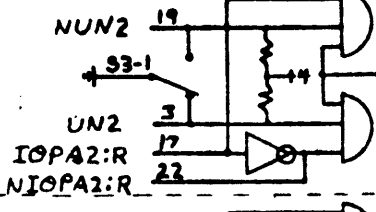
(22D)

8273/8473

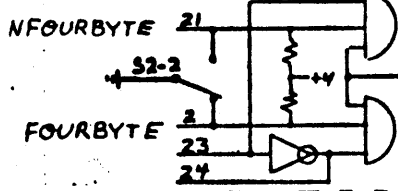
UP=HIGH PRIORITY
ON BUS-SHARE



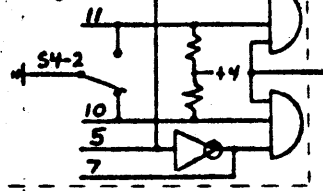
LSB
2



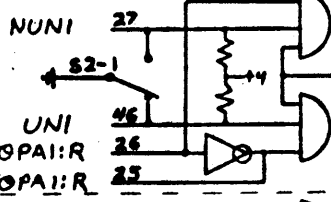
UP=4 BYTE
OPTION



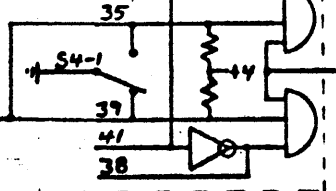
NOT
USED



OUTPUT #2



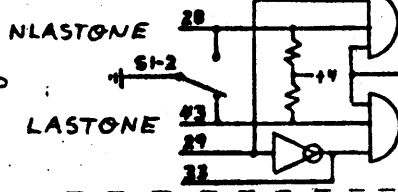
NOT
USED



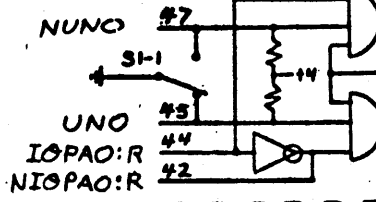
OUTPUT #1



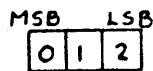
UP=LAST IOP



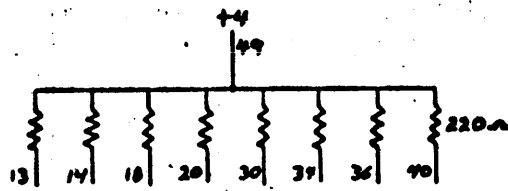
MSB
0



* NOTE-SW'S SHOWN IN DOWN
POSITION = 0 UP = 1



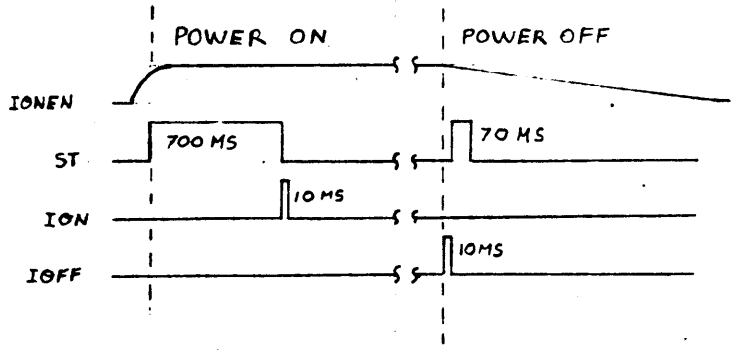
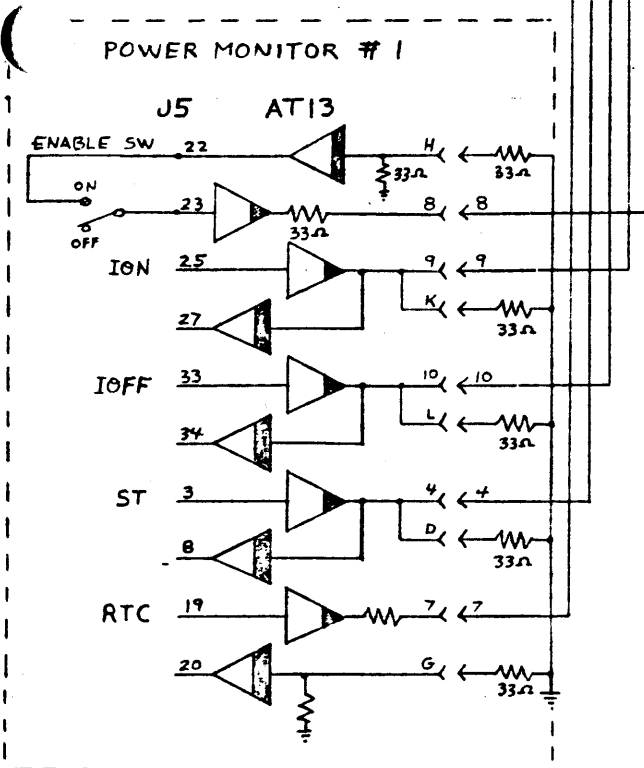
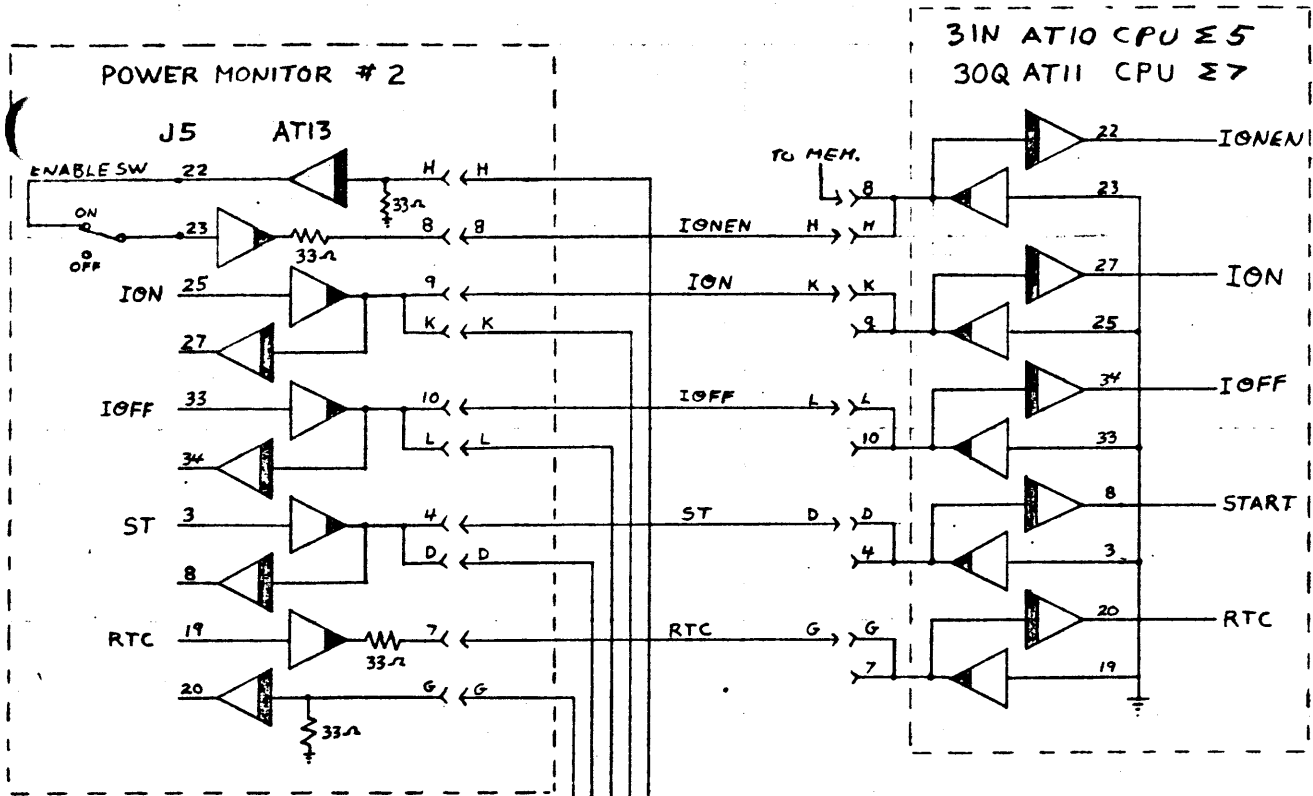
0 0 1 = 2nd. IOP



(13C)

32-BIT MIOP

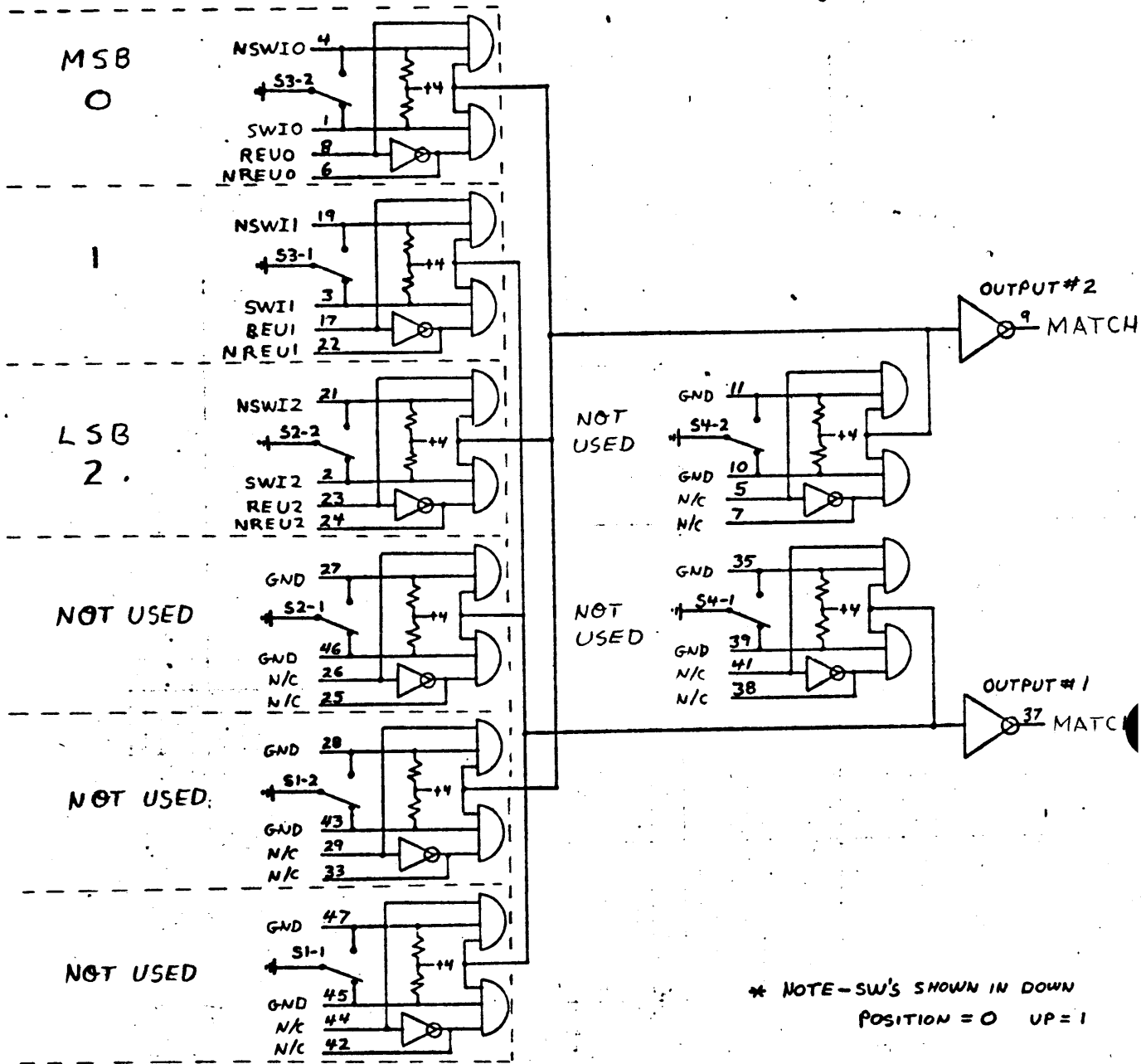
POWER MONITOR INTERFACE Σ7/5



LT26
Σ5/7

SWITCH MODULE
REGISTER EXTENSION UNIT
(32A)

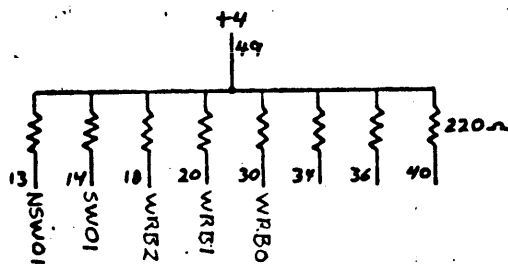
COCIRANE



* NOTE - SW'S SHOWN IN DOWN POSITION = 0 UP = 1

MSB LSB
0 1 2

0 0 1 = 1st EXT. REG



Σ5/7 REGISTER EXTENSION UNIT
(32A)

Σ 5/7 CFE

WITH 1 MA SECTION (= 2 MA UNITS)

69
CHRANE

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	ZT 23	AT 23	XT 10	AT 23	ZT 23	AT 23	ZT 23	AT 23	ZT 23	AT 23	ZT 23	AT 23	AT 23	ZT 23	AT 23	DT 14	HT 15	DT 14	HT 15	DT 14	LT 29	LT 29	LT 29	FT 22	GT 11	FT 22	XT 10	LT 26				
B	AT 11 MOO ↓ M13		AT 11 M14 ↓ M27	BT 16	AT 11 M28 ↓ M31	BT 16	AT 11 HREQ	XT 10	AT 12 L15 ↓ L28	FT 22	FT 22	Y	IT 14	IT 14	FT 12	FT 12	FT 12	Y	FT 12	IT 16	LT 13	Y	LT 21	BT 16	FT 26	FT 26	FT 22	Y	FT 22	BT 16		
C	ZT 46 31A ↓ 1	ZT 46 2	FT 22	FT 22	PET	PET	XT 10	FT 41	LT 17	LT 17	FT 41	Y	LT 18	FT 41	LT 17	LT 17	FT 41	Y	FT 39	FT 39	FT 39	Y	FT 26	IT 16	FT 26	BT 16	BT 16	Y	FT 18	FT 18	FT 18	XT 10
D	ZT 23	IT 16	AT 11	FT 22	AT 11	LT 13	FT 41	LT 17	LT 17	FT 41	XT 10	LT 18	FT 41	LT 17	LT 17	FT 41	BT 10	IT 16	BT 16	LT 18	XT 10	GT 11	FT 22	FT 18	LT 18	IT 25	FT 26	LT 18	IT 25	FT 26	XT 10	BT 11
E	Y	Y	BT 11	AT 11	IT 14	AT 10	BT 16	AT 11	FT 22	XT 10	FT 22	FT 22	IT 16	BT 11	BT 16	IT 16	LT 13	BT 10	XT 10	LT 13	IT 25	IT 25	BT 11	IT 16	IT 25	Y	IT 16	LT 13	XT 10	FT 22	FT 18	
A	Y	Y	ZT 23		FT 41	LT 17	FT 17	FT 41	LT 17	XT 10		LT 17	FT 41	LT 18	FT 17	LT 17	FT 41	FT 17	LT 17	XT 10	LT 17	FT 41	FT 17	LT 17	FT 41	LT 18	XT 10	LT 17	FT 41	FT 17	LT 17	FT 41
B					FT 41	FT 41	BT 16					IT 16	BT 16	BT 16	BT 16	XT 10	IT 16	FT 41	BT 16	FT 41	FT 41	LT 18	XT 10	BT 16	FT 41						XT 10	
C	ZT 46 32A ↓ 1		XT 10		FT 41	LT 17	FT 17	FT 41	LT 17	XT 10		LT 17	FT 41	LT 18	FT 17	LT 17	FT 41	FT 17	LT 17	XT 10	LT 17	FT 41	FT 17	LT 17	FT 41	LT 18	XT 10	LT 17	FT 41	FT 17	LT 17	FT 41

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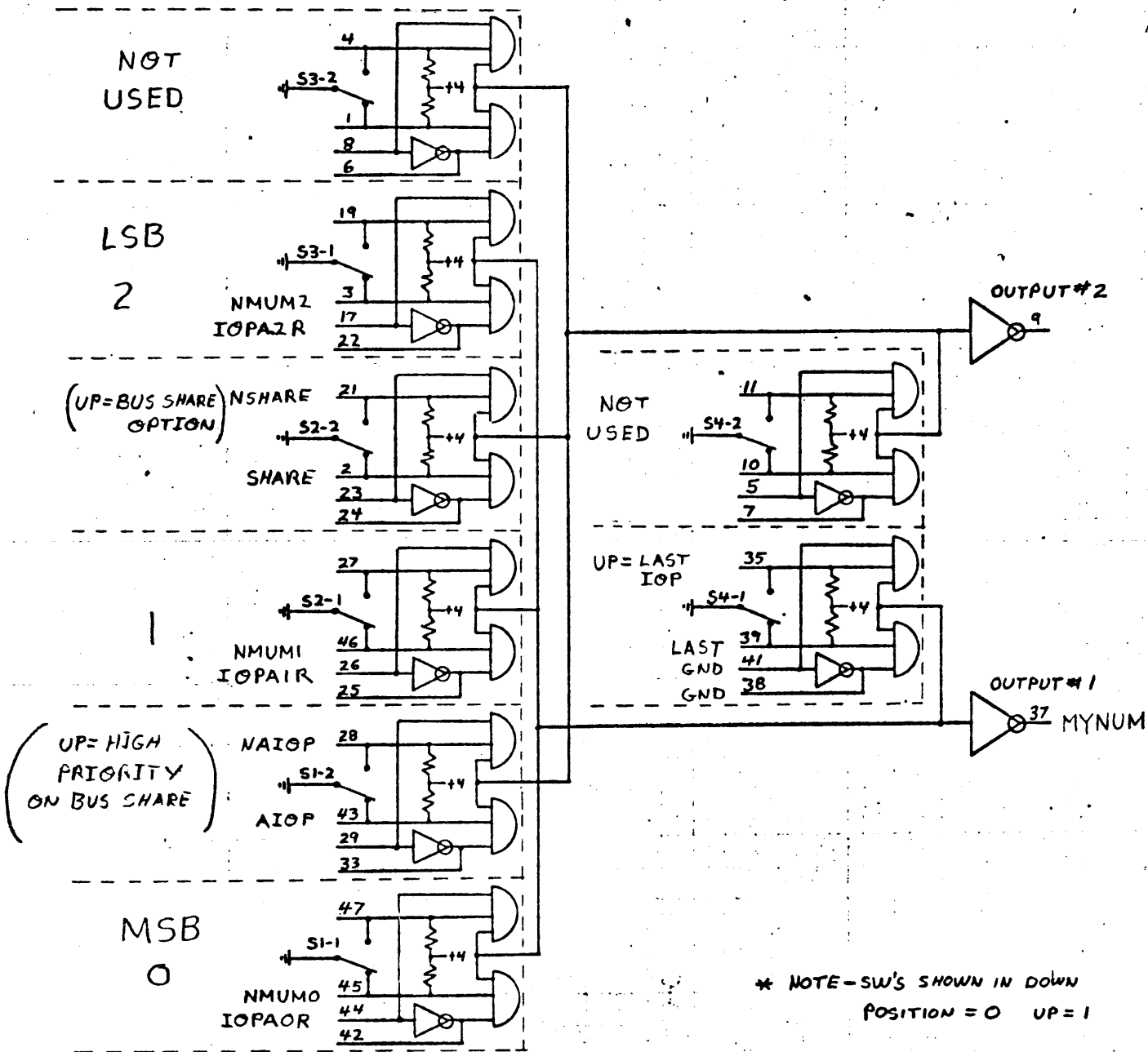
1 = TO 1ST MULT/ADD FRAME MA2 THRU MA 4
2 = TO 2ND MULT/ADD FRAME MA5 THRU MA 7

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	DT 14	HT 15	BT 22	FT 24	IT 26	LT 13	XT 10	BT 10	XT 10	AT 24	FT 37	IT 13	BT 16	FT 38	FT 38	FT 38	AT 16	BT 10	LT 20	IT 16	AT 11	IT 25	LT 21		XT 10	LT 13	LT 13	FT 37	BT 18	BT 15	IT 18	A	
B	AT 16	IT 25	IT 24	BT 22	IT 25	LT 21	FT 26	BT 16	IT 16	FT 39	FT 39	FT 27	FT 39	FT 26	FT 39	XT 10	LT 13	IT 16	IT 15	IT 11	IT 11	IT 11	BT 18	FT 37	XT 10	XT 10	IT 15	FT 37	IT 16	FT 37	LT 13	IT 25	B
C	FT 18	FT 18	LT 13	FT 27	XT 10		IT 15	IT 25	BT 25	XT 10		BT 10	BT 25	IT 16	IT 25		BT 10	BT 10	LT 21	BT 15		BT 18	IT 18	LT 13	XT 10		LT 29	DT 14	HT 15	BT 16		BT 22	C
D	BT 11	FT 18	FT 18	FT 18	FT 18		FT 38	FT 38	FT 38	FT 38		FT 38	AT 11	FT 38	AT 11		FT 38	AT 11	FT 38	AT 11		AT 12	FT 37	FT 37	LT 21		XT 10	DT 11	HT 15	BT 15		BT 22	D
E	GT 11	FT 18	FT 18	BT 11	FT 18	FT 18	FT 18	FT 18	XT 10	FT 38	AT 11	FT 37	AT 11	FT 37	AT 11	BT 16	XT 10	AT 10	BT 18	BT 25	AT 12	LT 21	AT 11	LT 21	XT 10		FT 24	FT 37	LT 20	BT 10	LT 21	E	
F			BT 22	BT 16	XT 10	BT 11	BT 15	FT 18	FT 18	GT 11	BT 22	BT 10	FT 22	BT 24	IT 16	LT 65	IT 15	IT 25	BT 18	IT 16	IT 25	BT 16	AT 13	LT 64	LT 26	XT 10	IT 16	IT 25					F
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

1= BUSS SHARING OPTION
2= AT16 USED IN 1st. SIOP ONLY

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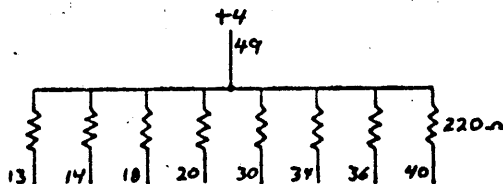
CoProne
4/30/69



MSB LSB

0	1	2
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 0 0 1 = 2ND IOP



(8F) SIOP

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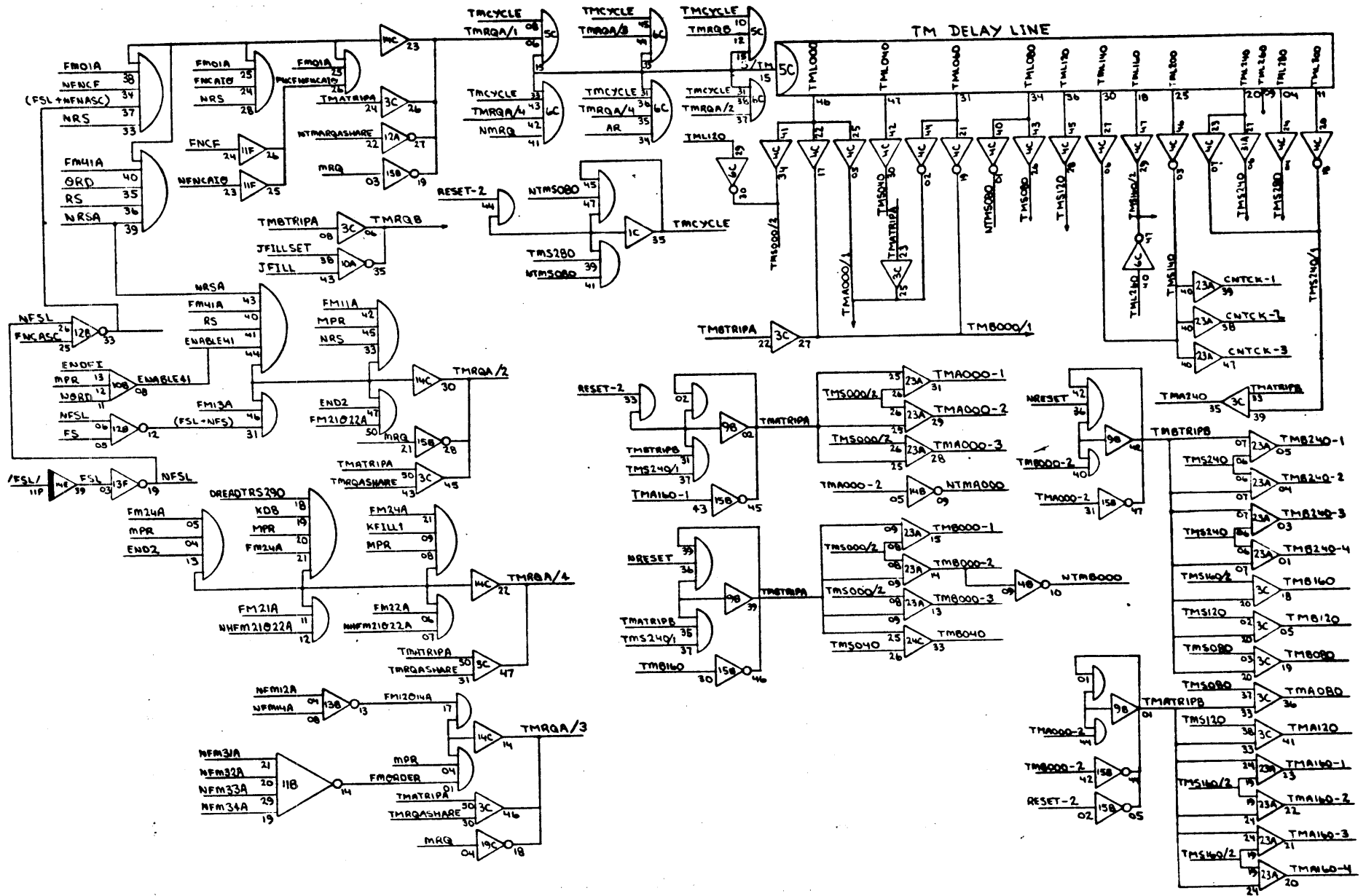
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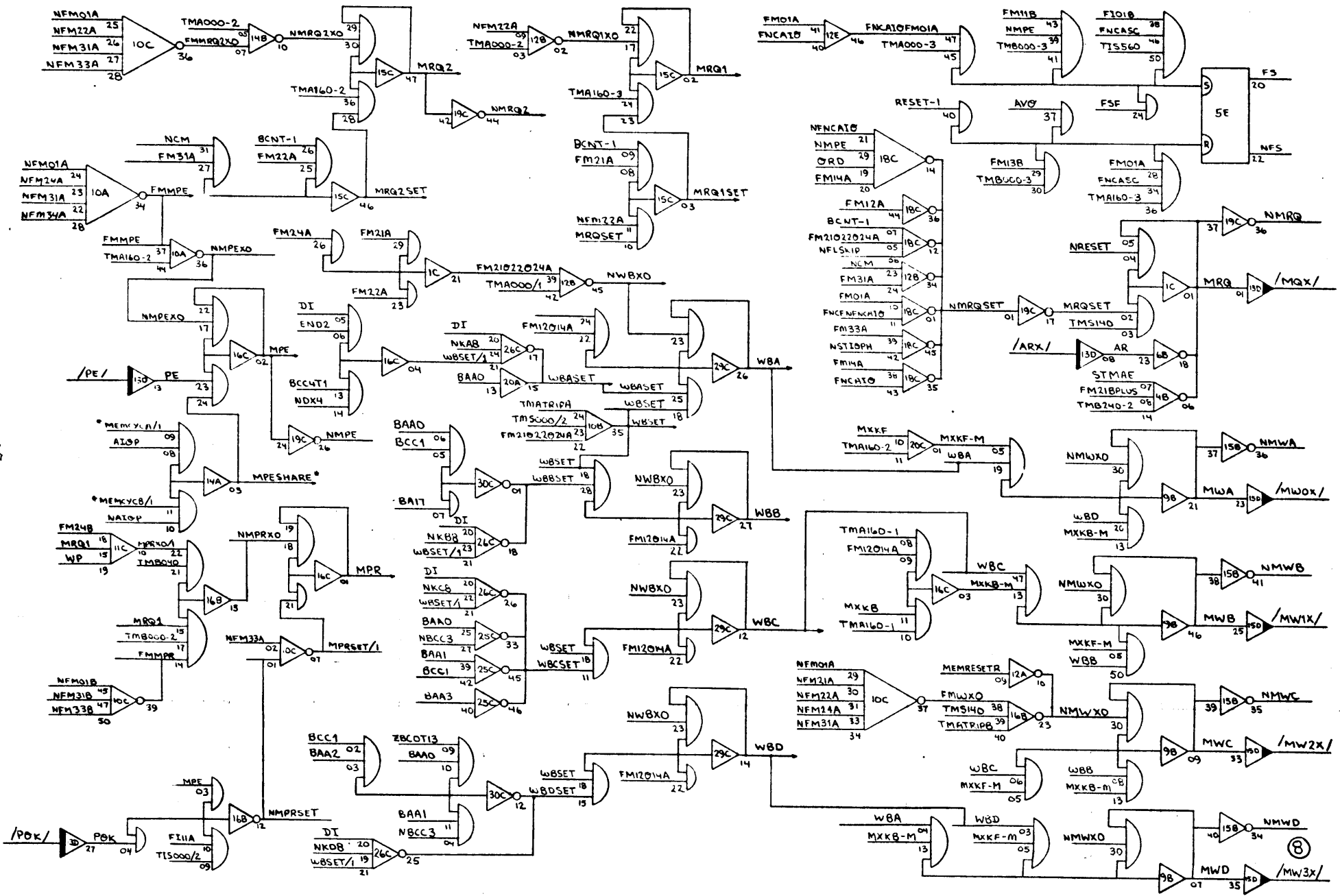
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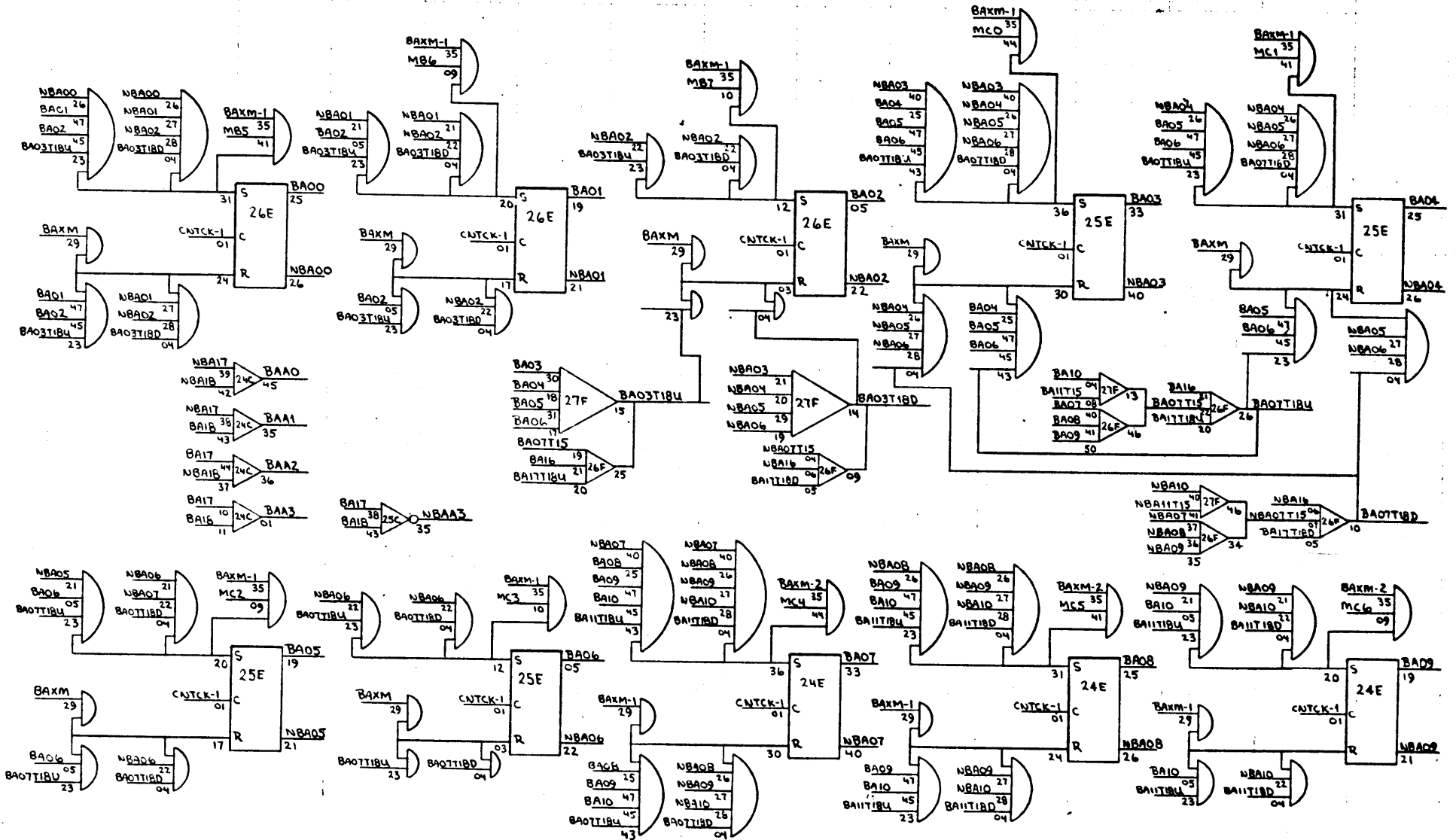
* BUSS SHARE

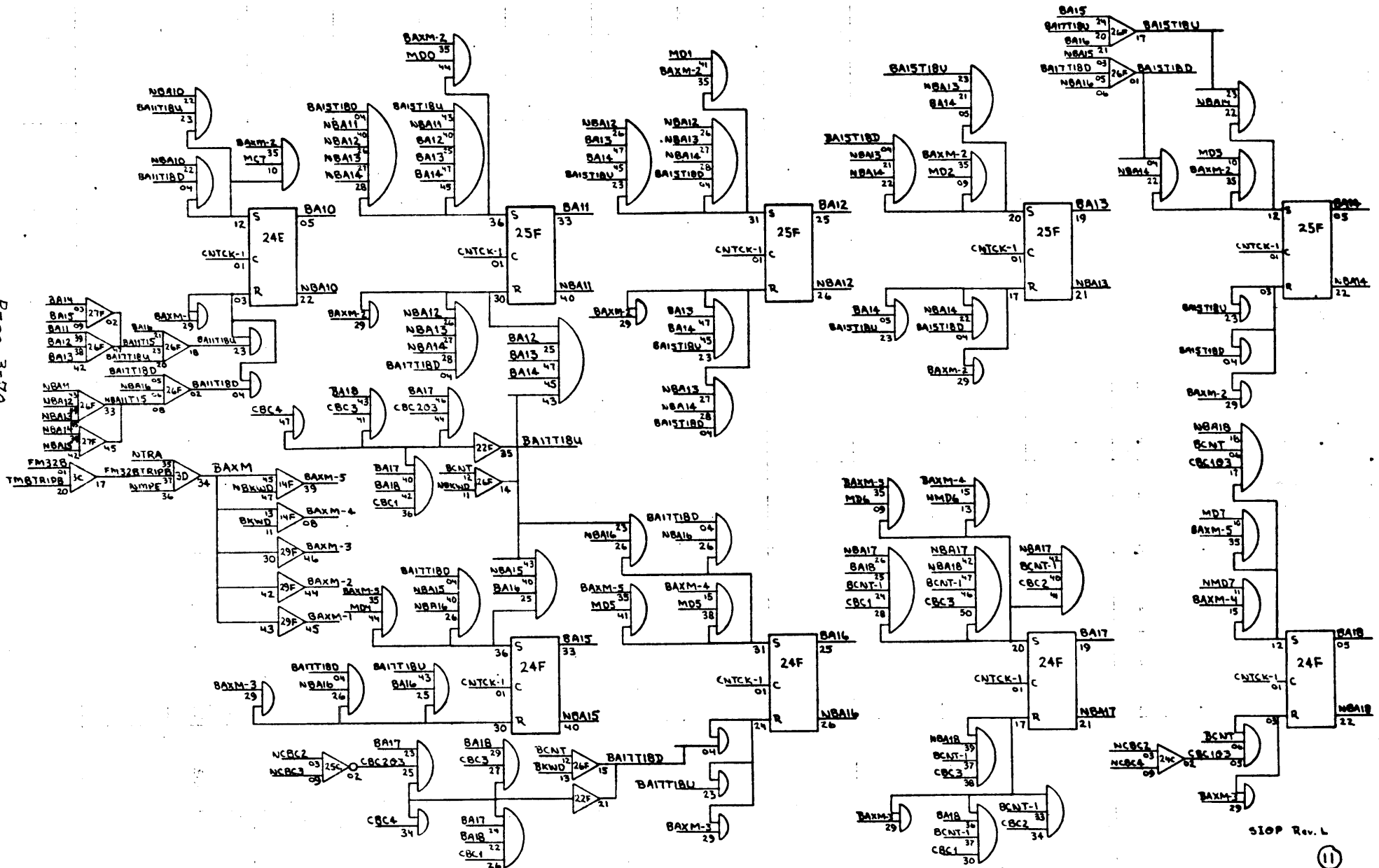
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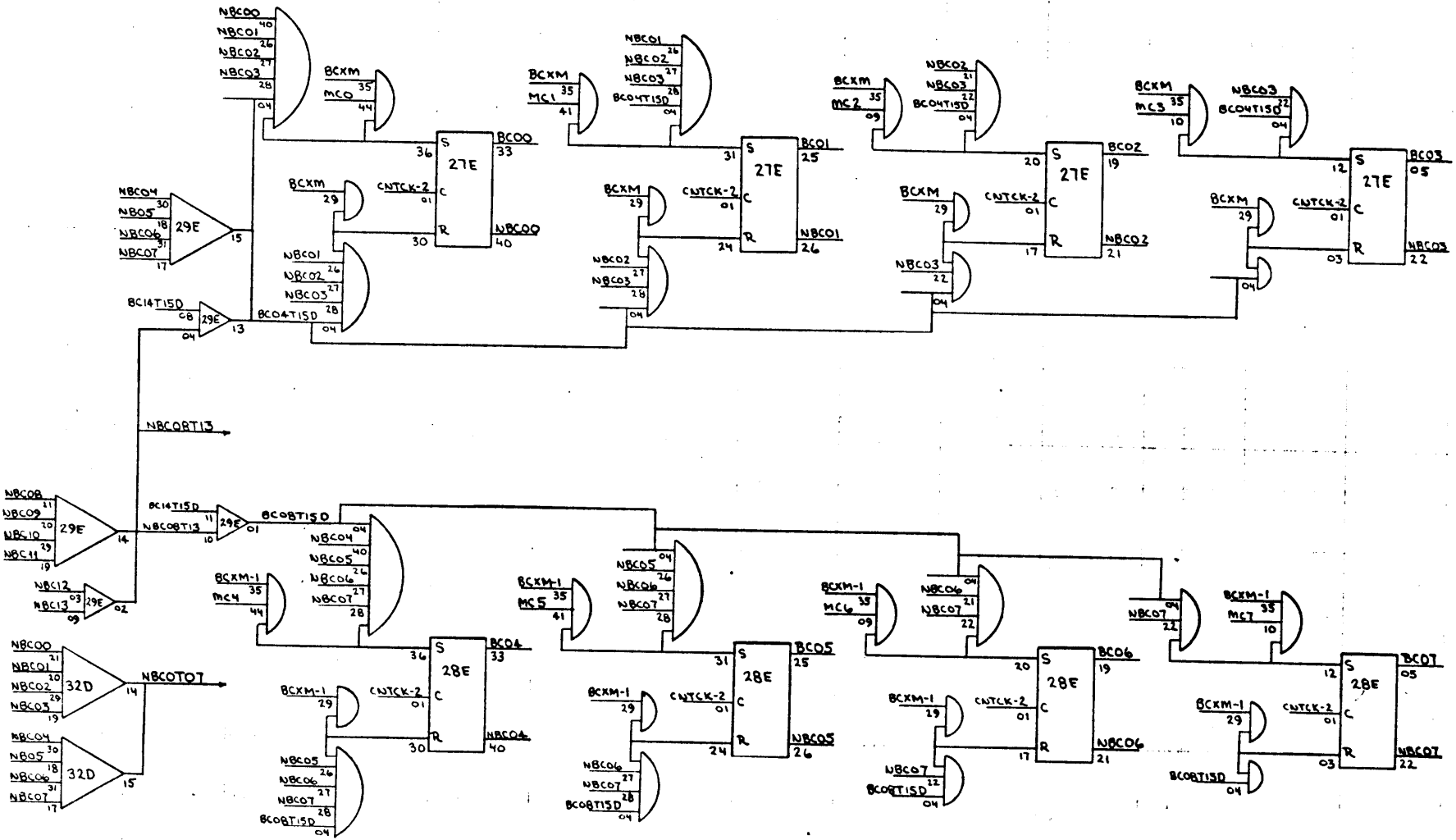
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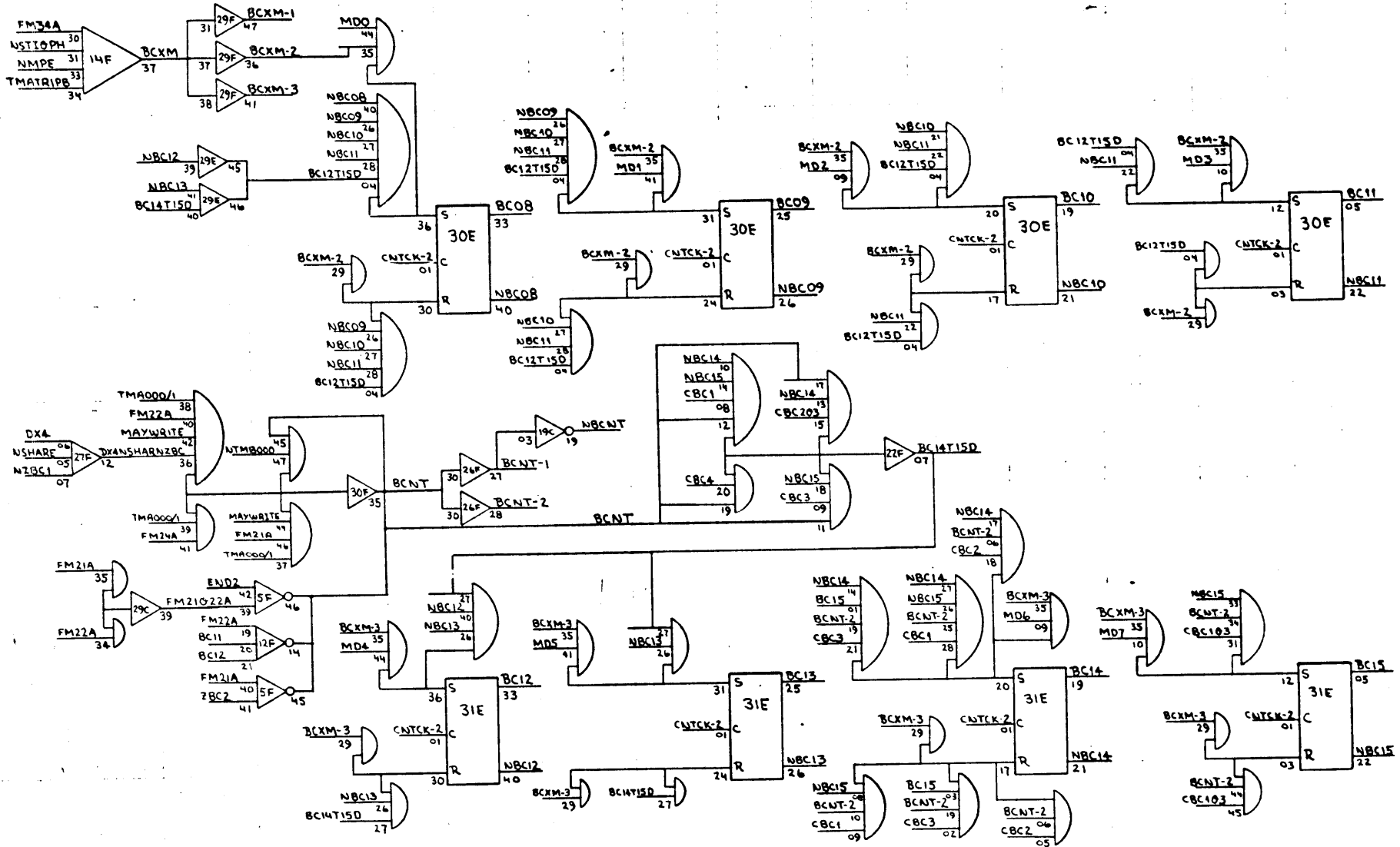








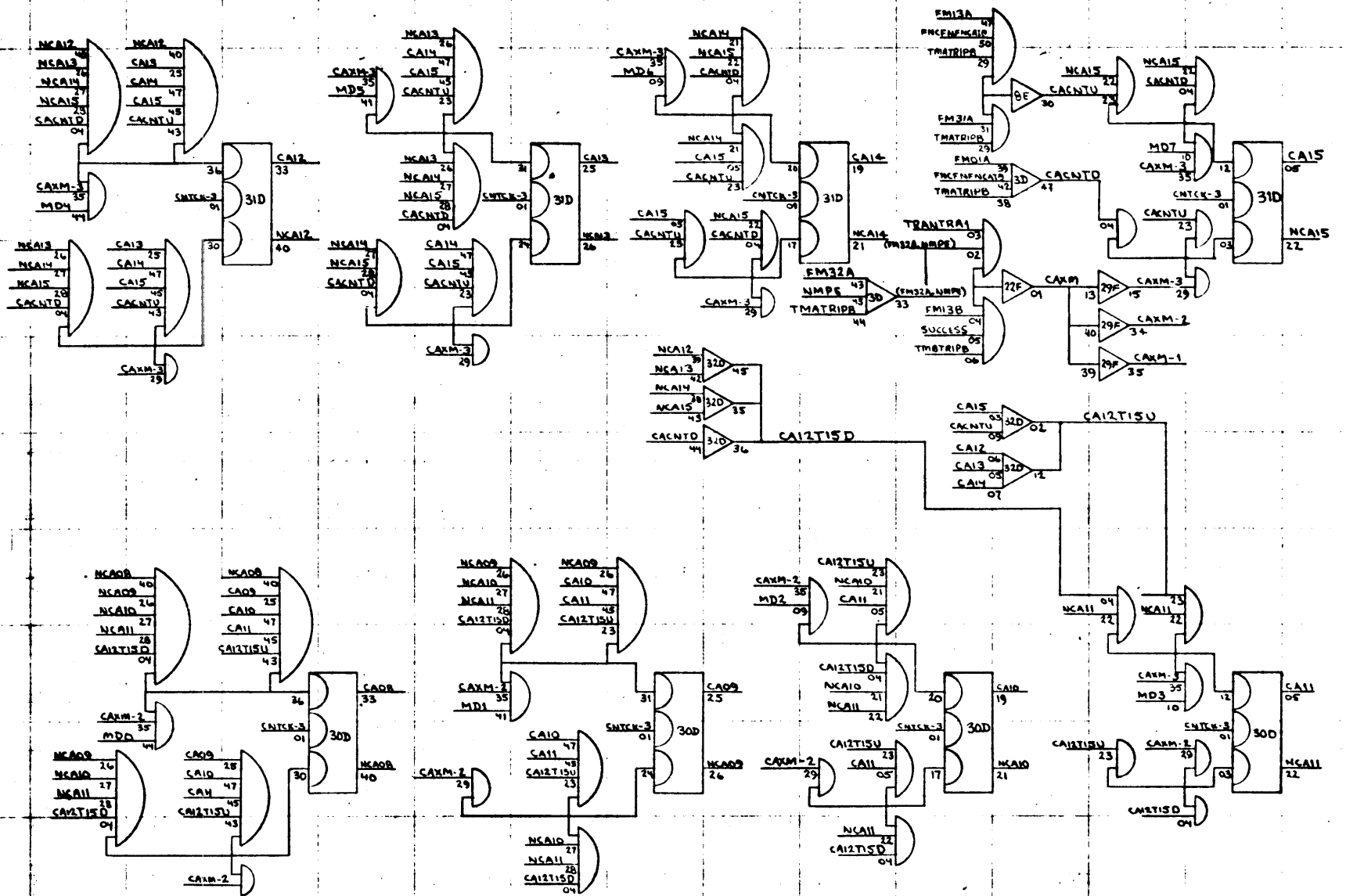
SIOP Rev. L
Circ. Schematic



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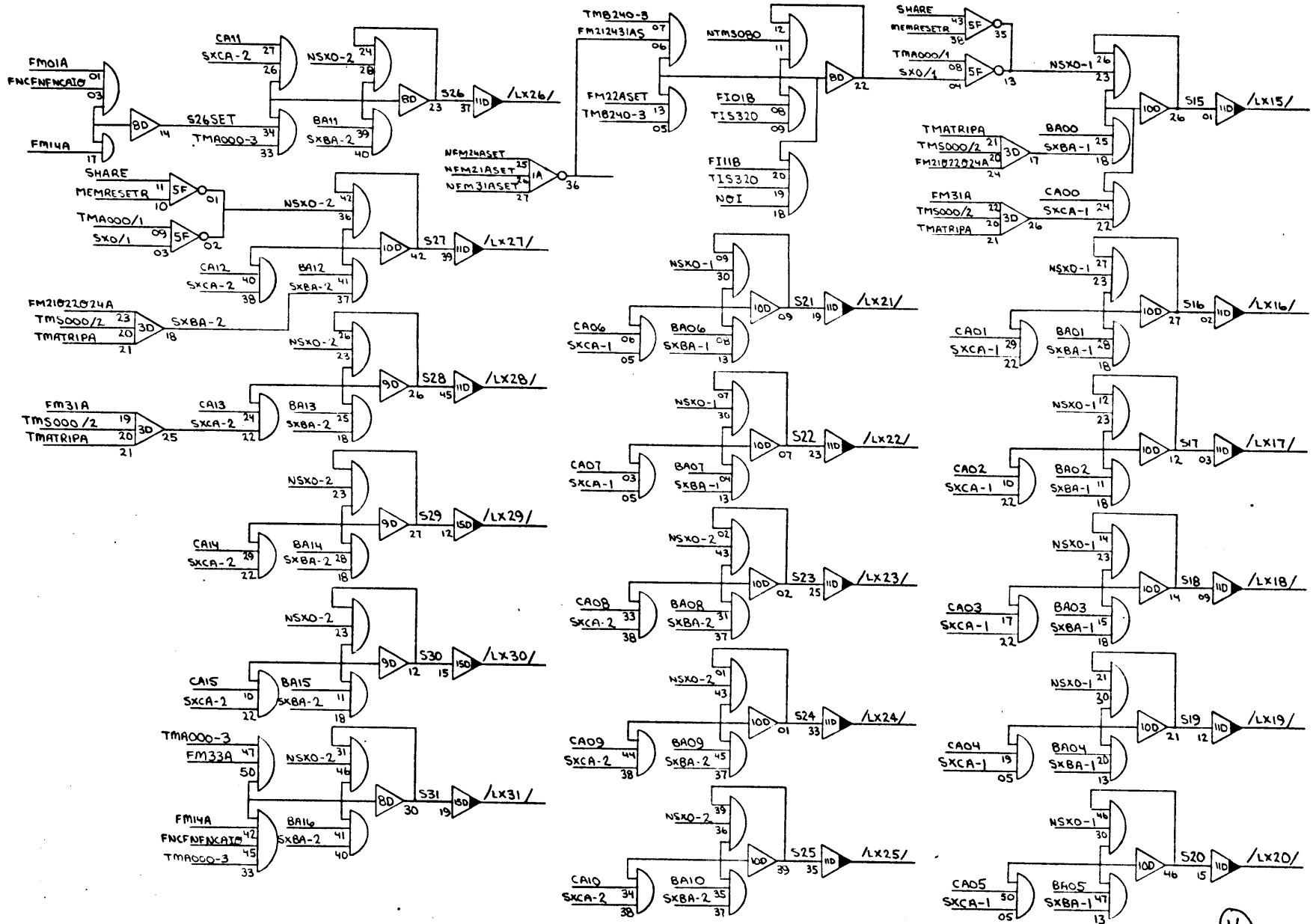
SIOP Rev L
Eric Salmons

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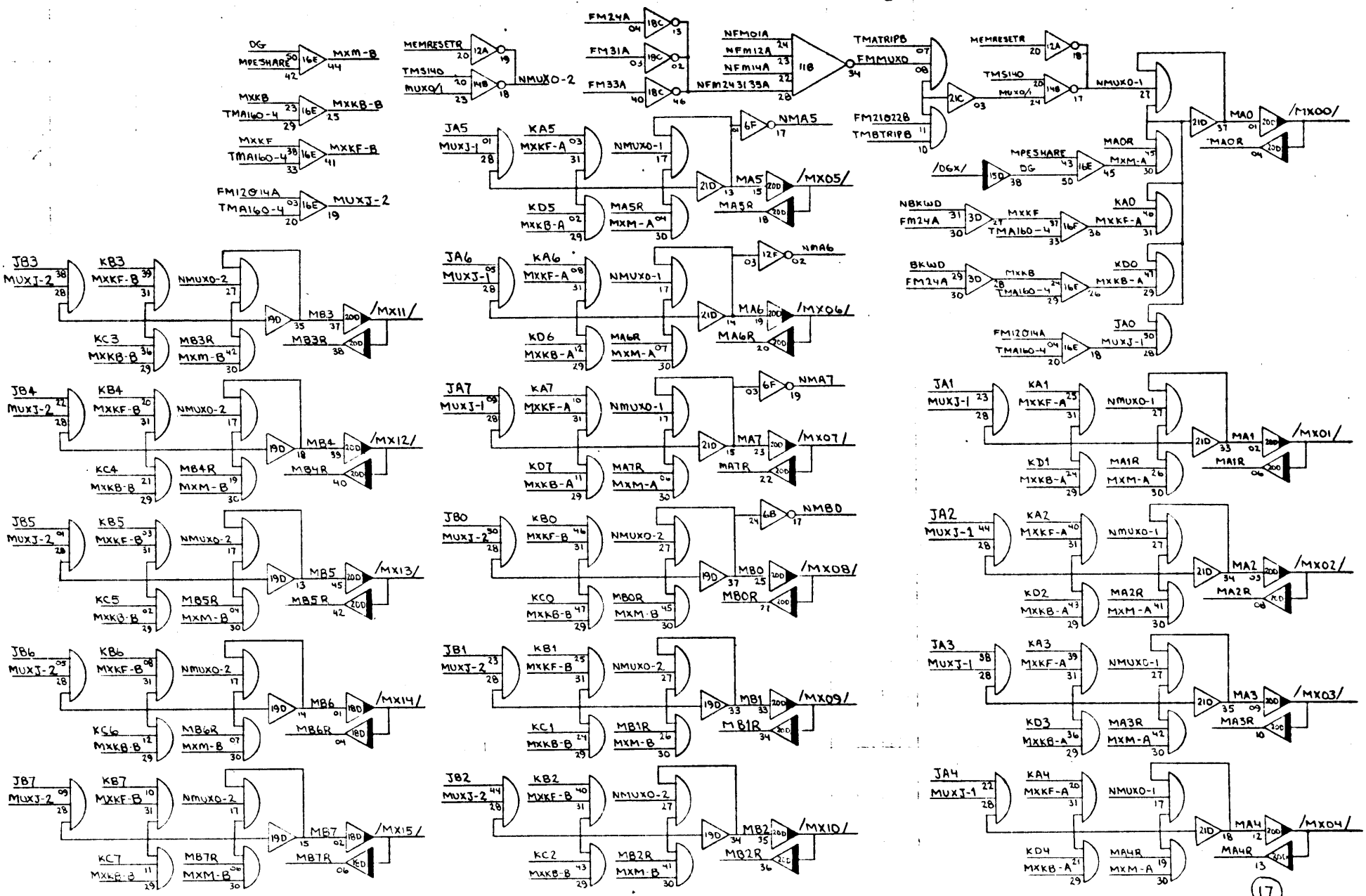
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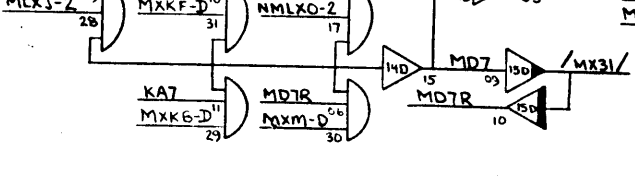
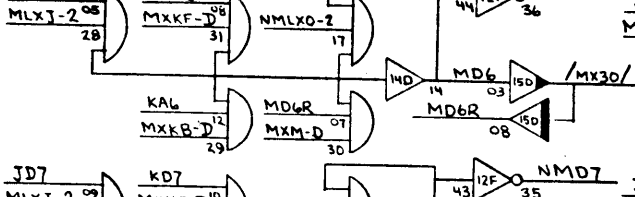
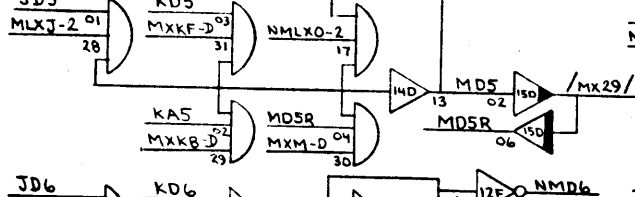
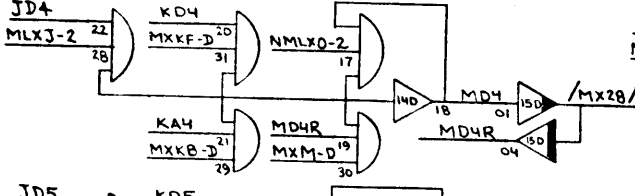
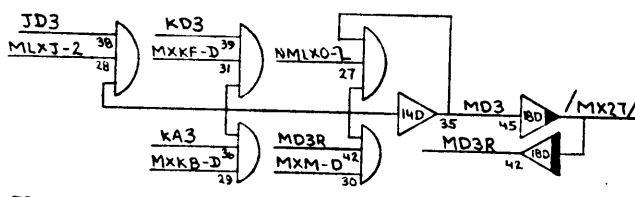
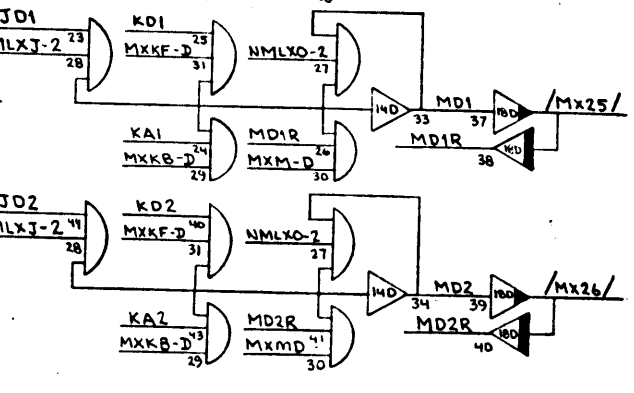
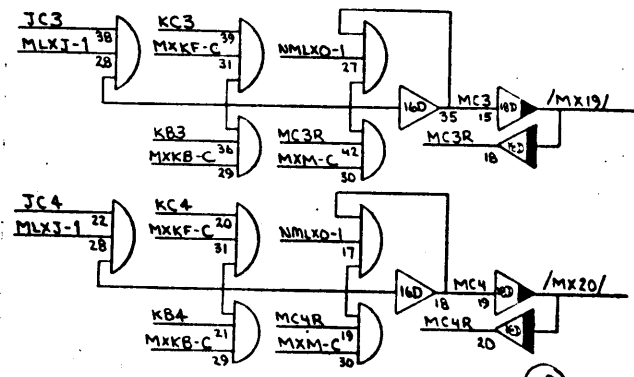
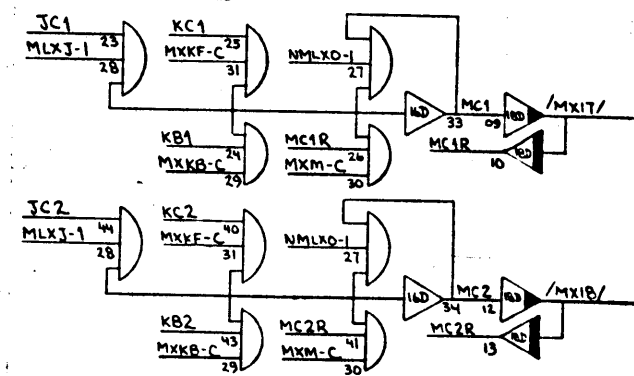
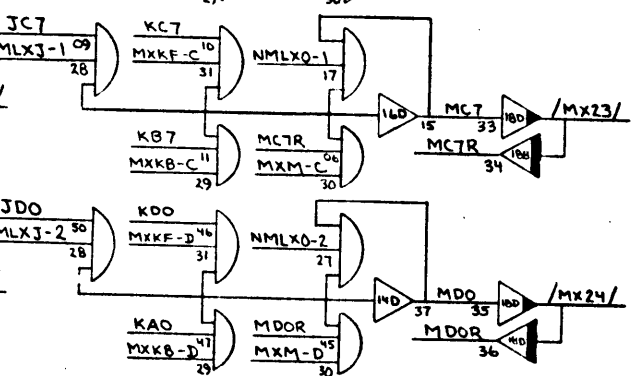
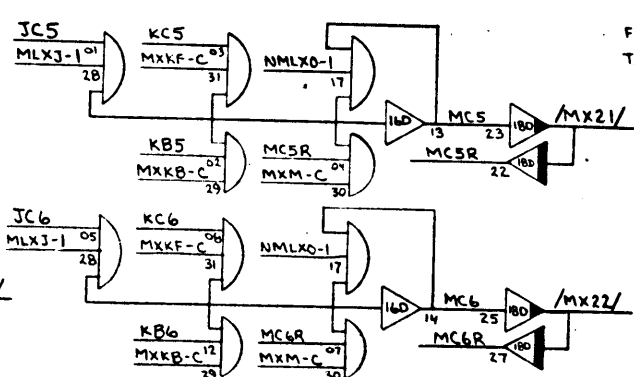
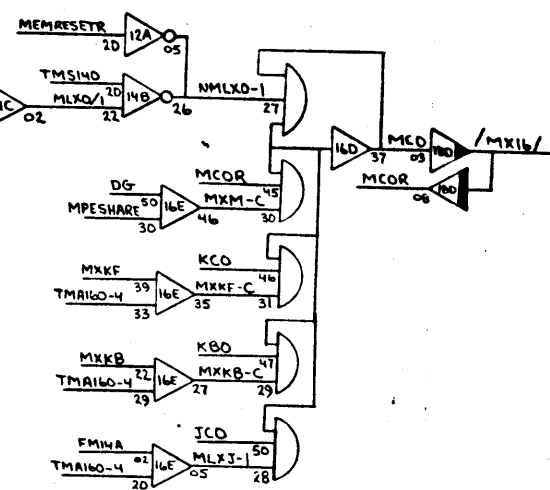
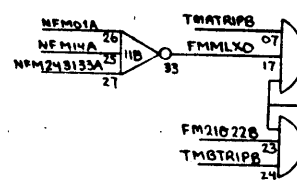
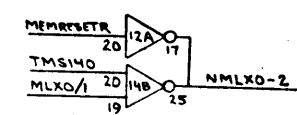
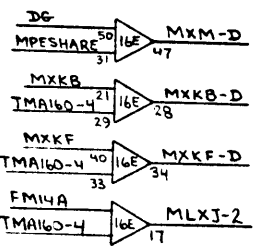
STOP REV L ERIC SALONIS



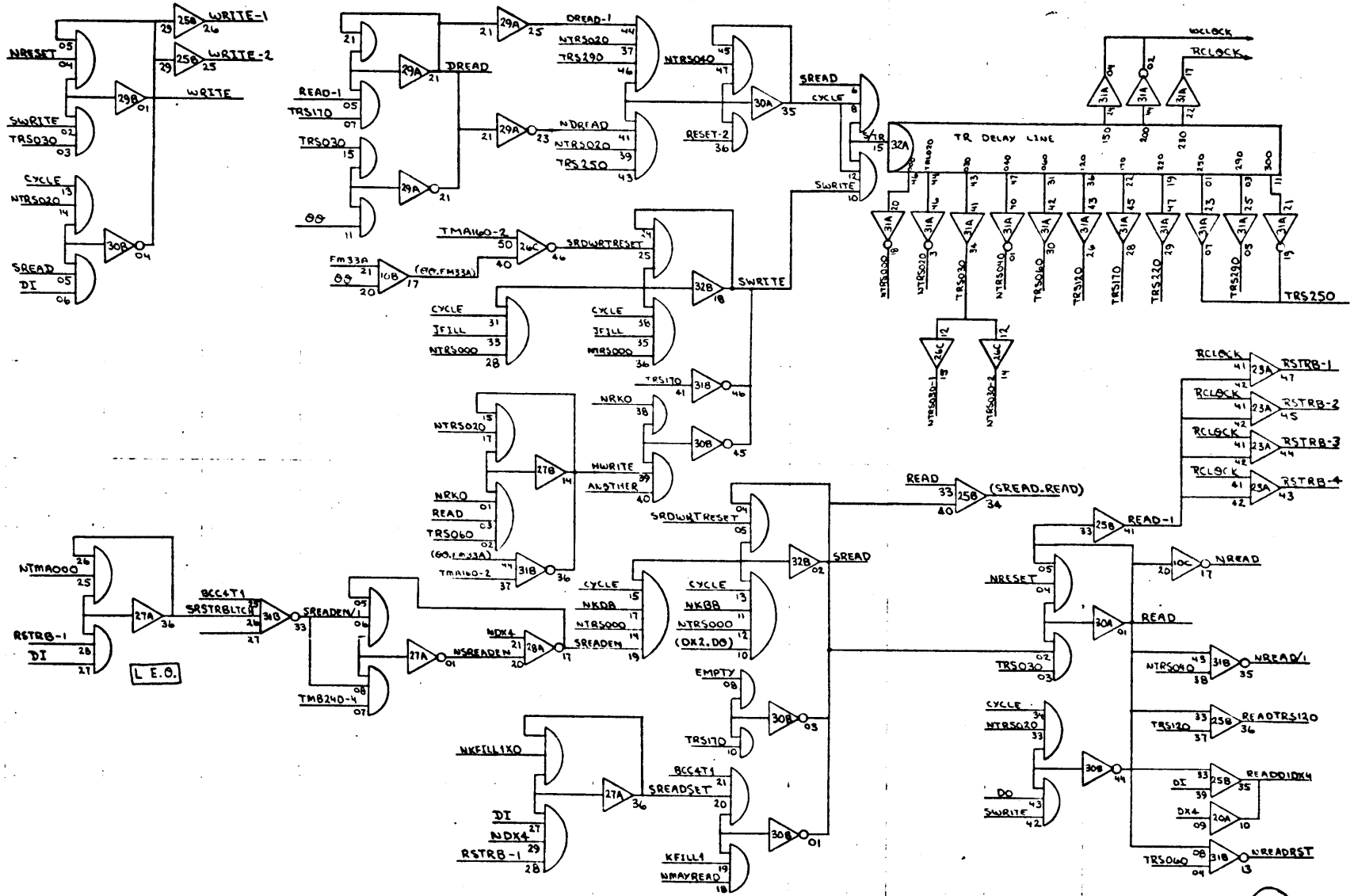
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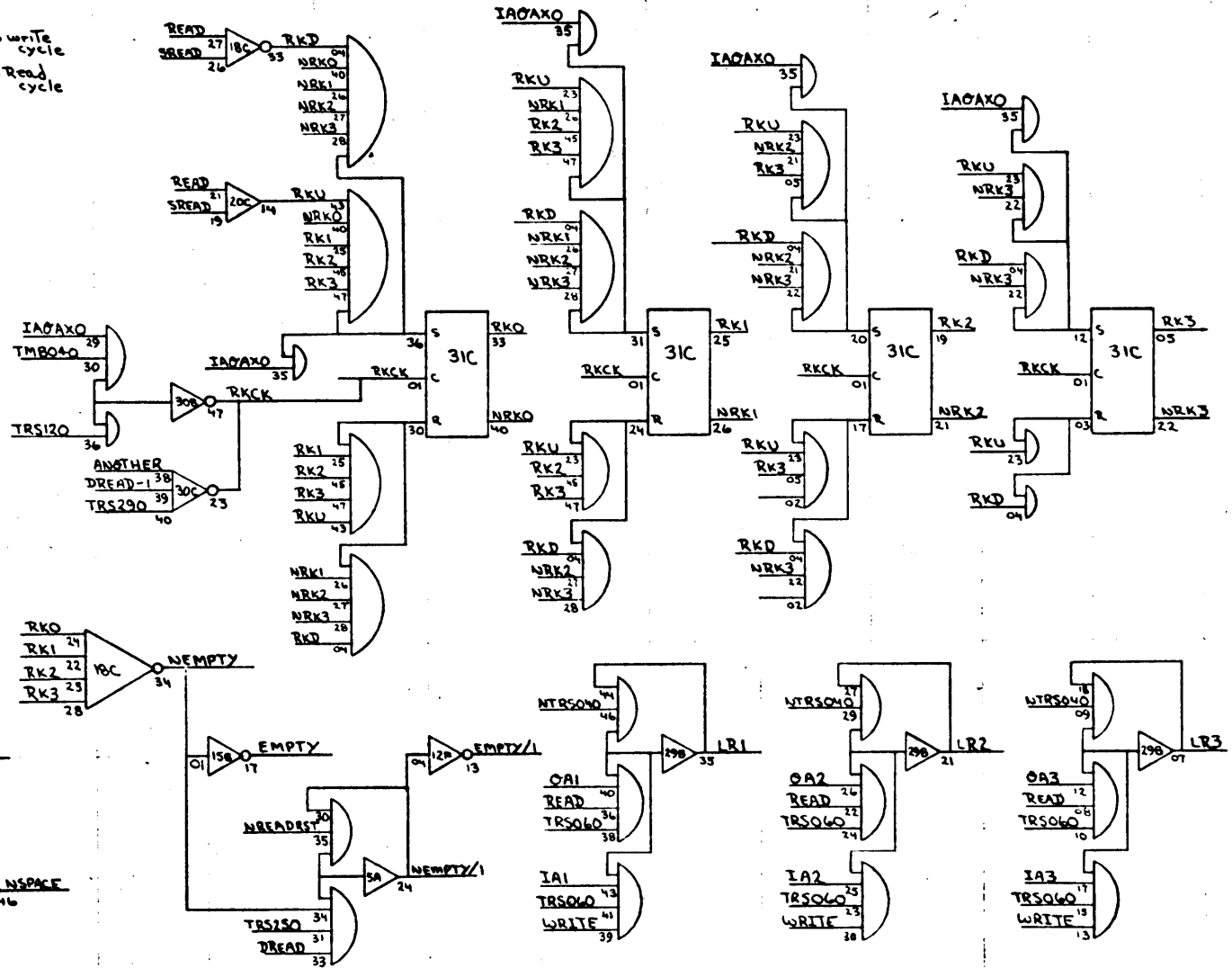
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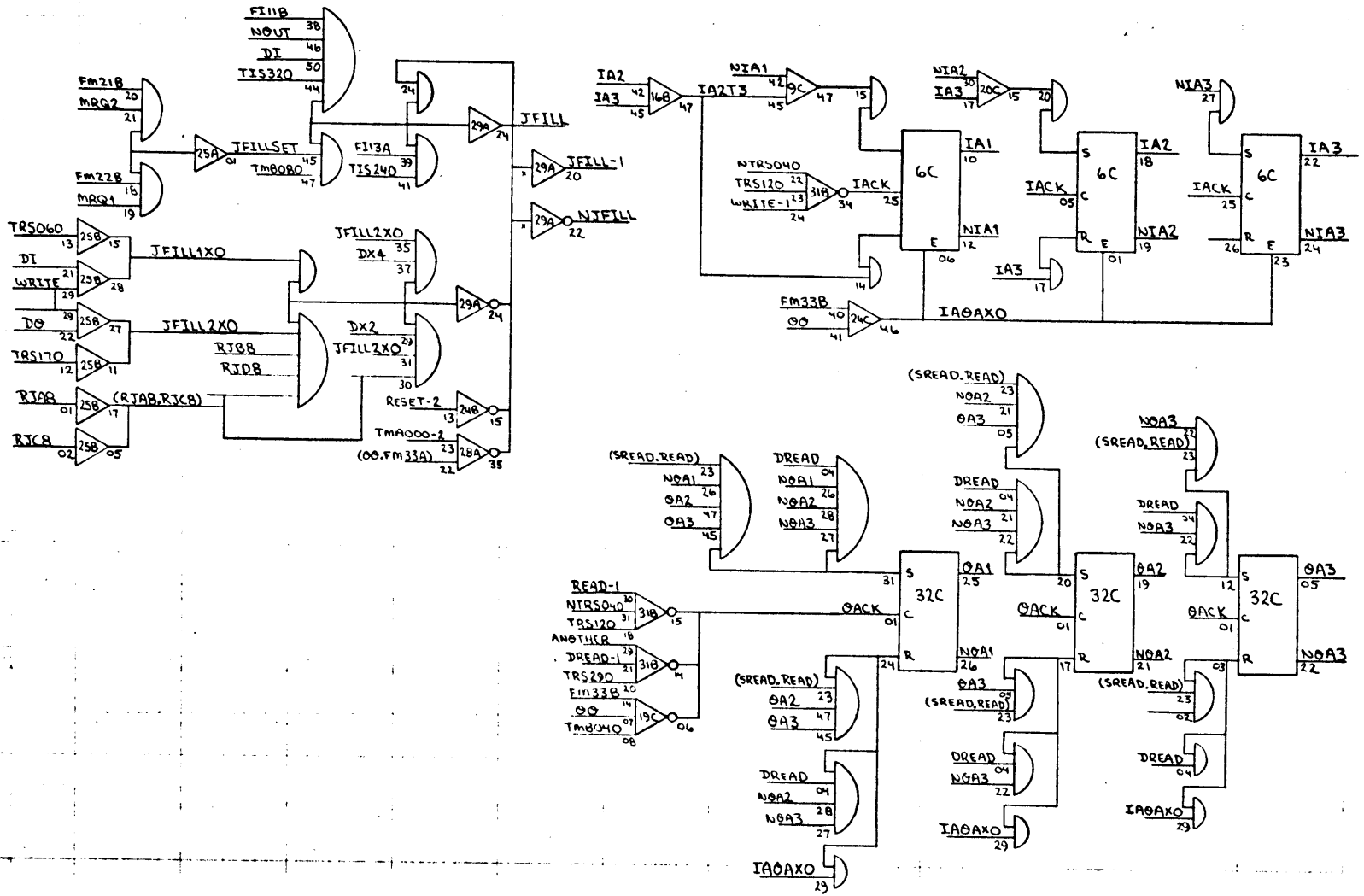
RK-Register Decode

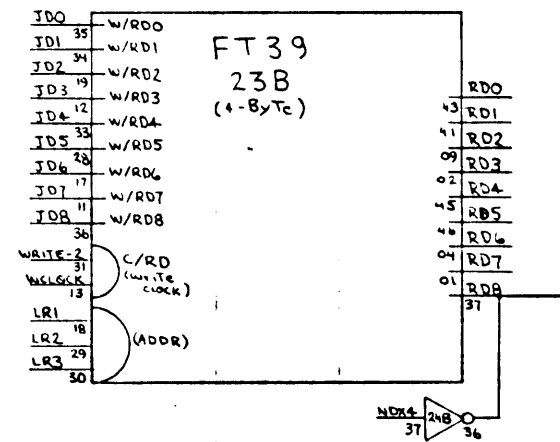
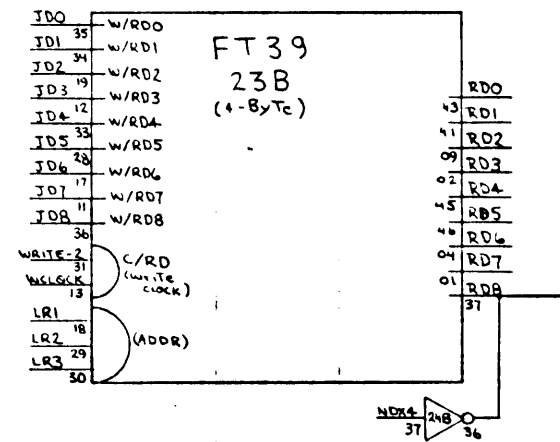
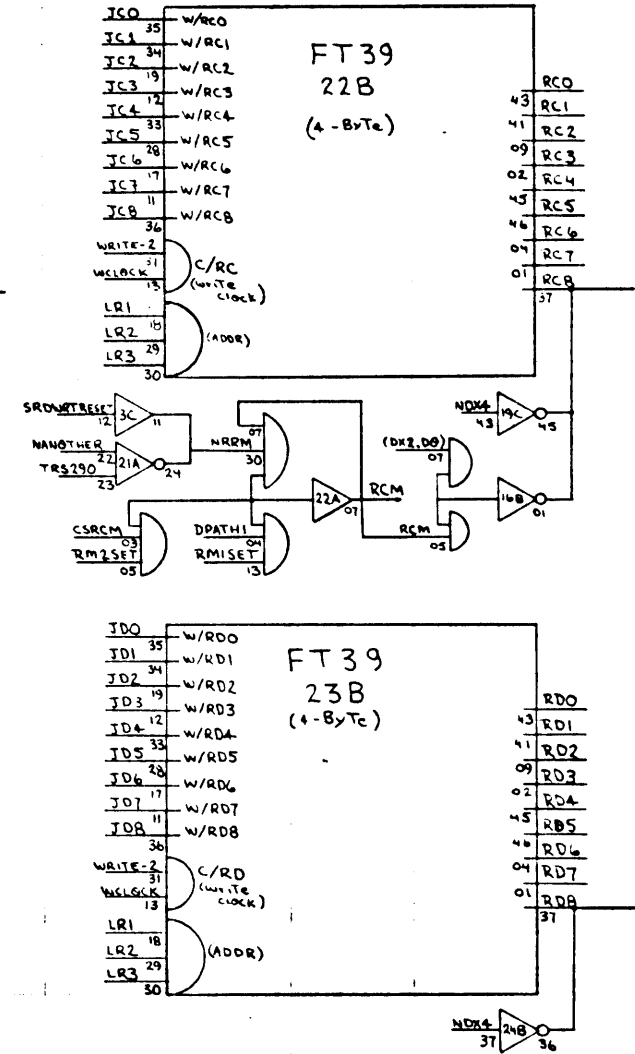
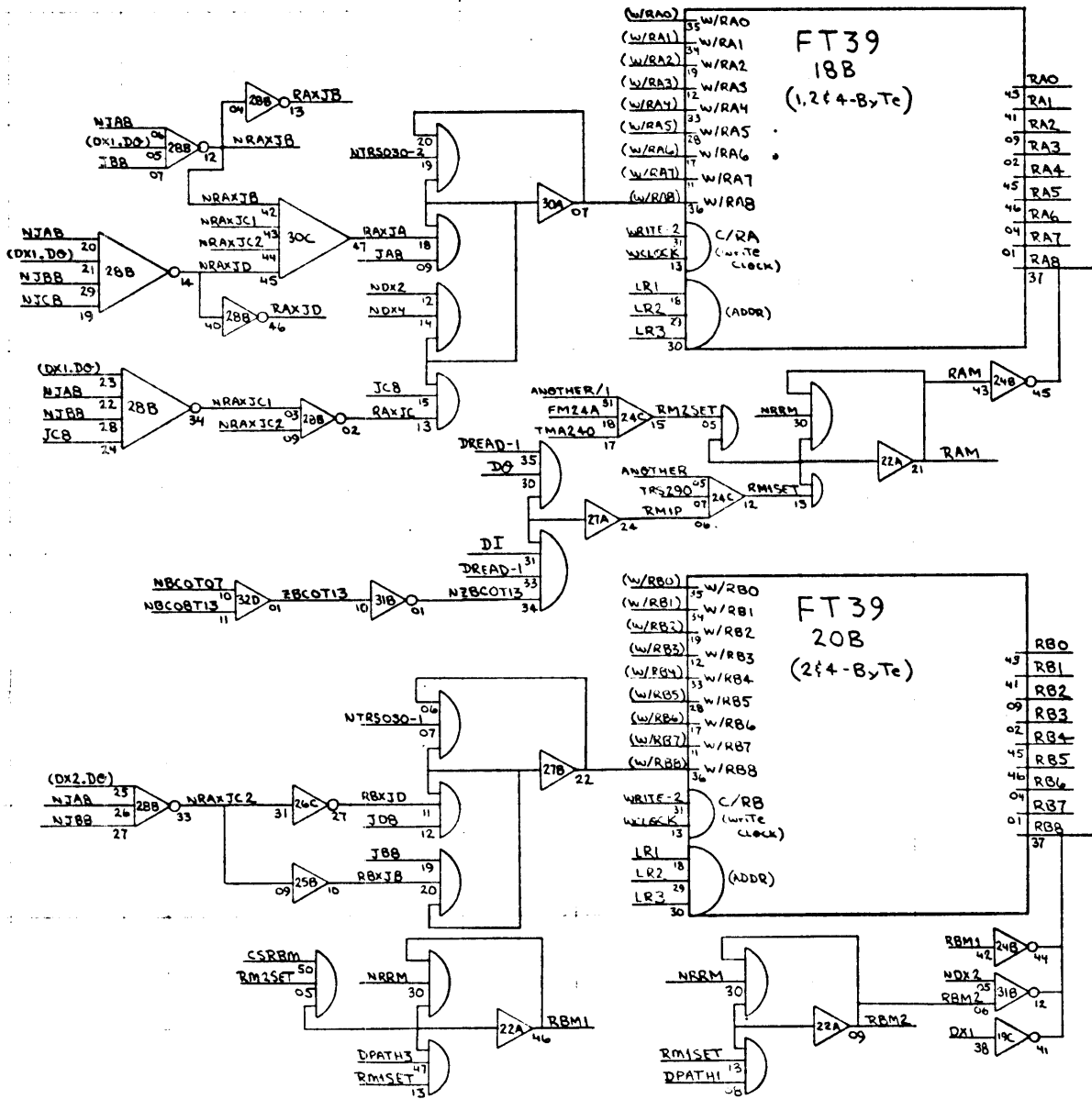
RK0	RK1	RK2	RK3	LOCATIONS FILLED
1	1	1	1	0 (empty)
1	1	1	0	1
1	1	0	1	2
1	1	0	0	3
1	0	1	1	4
1	0	1	0	5
1	0	0	1	6
0	1	1	1	8 (full)

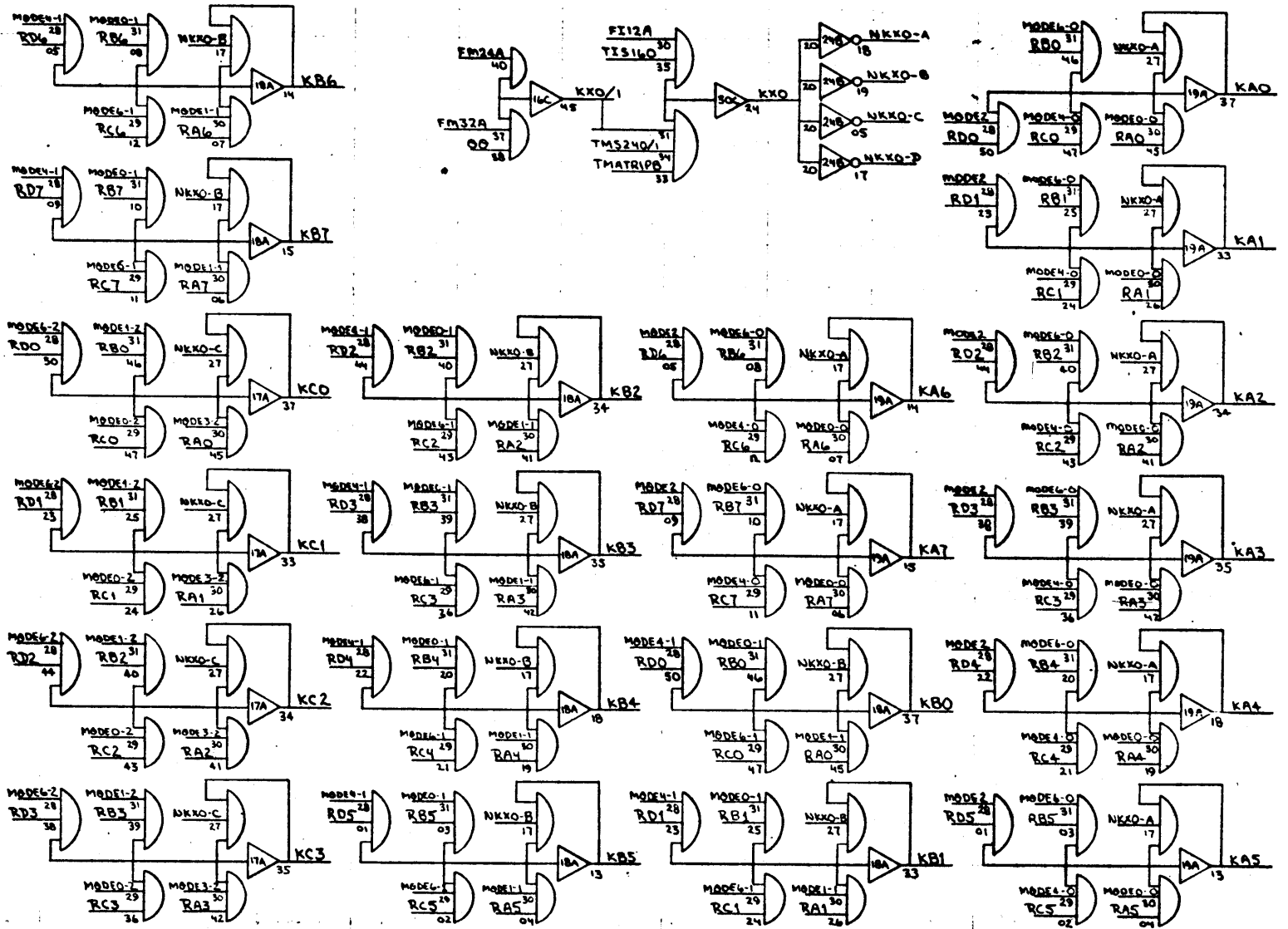
RKD => write cycle
 RKU => Read cycle

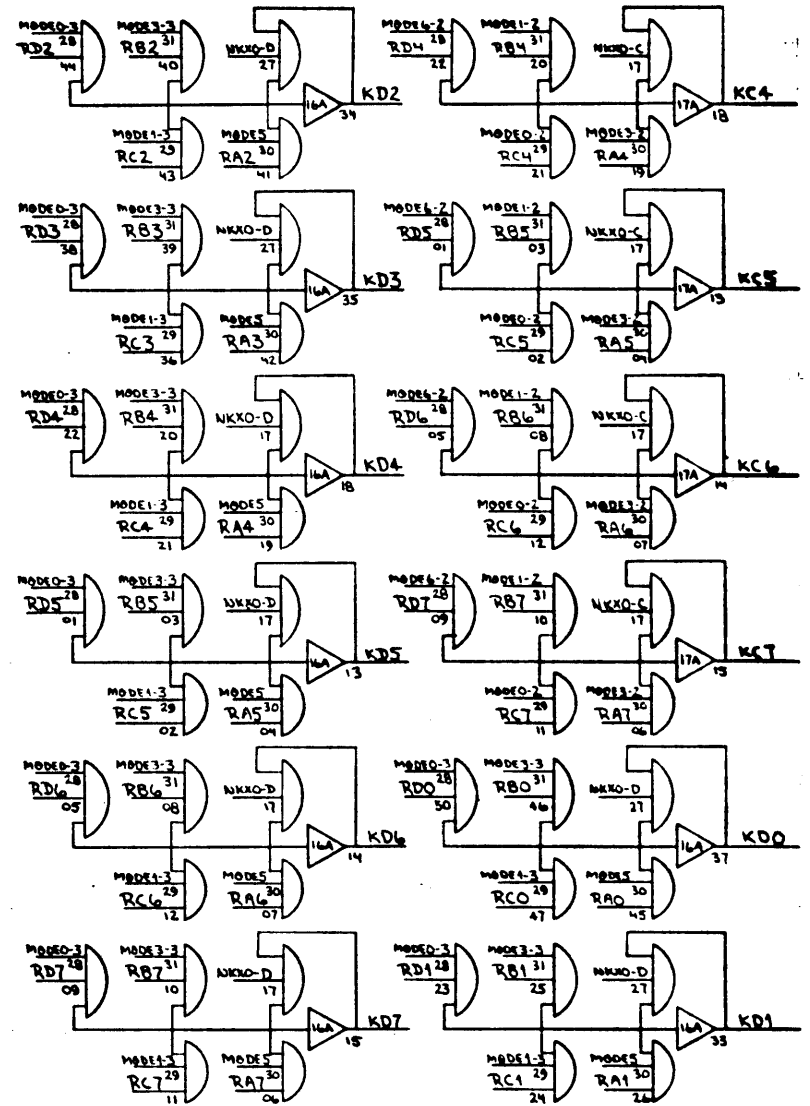
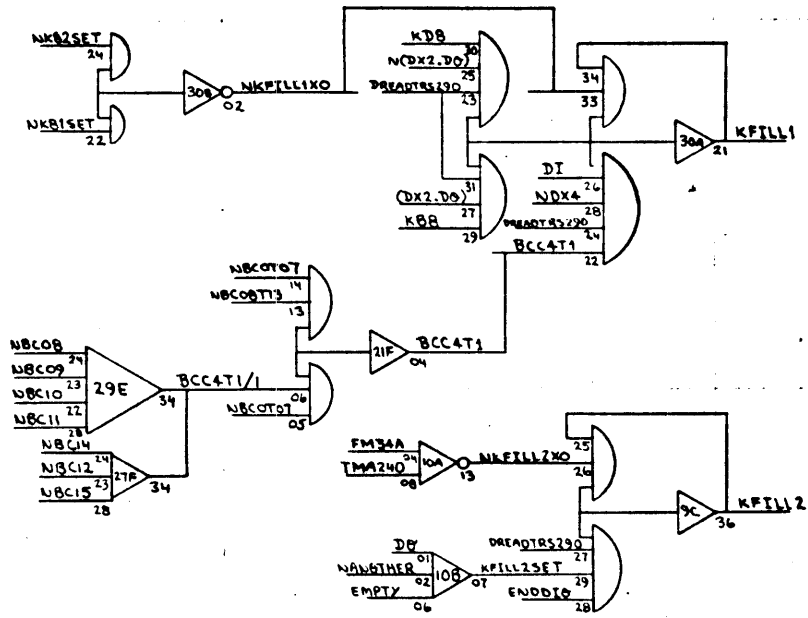


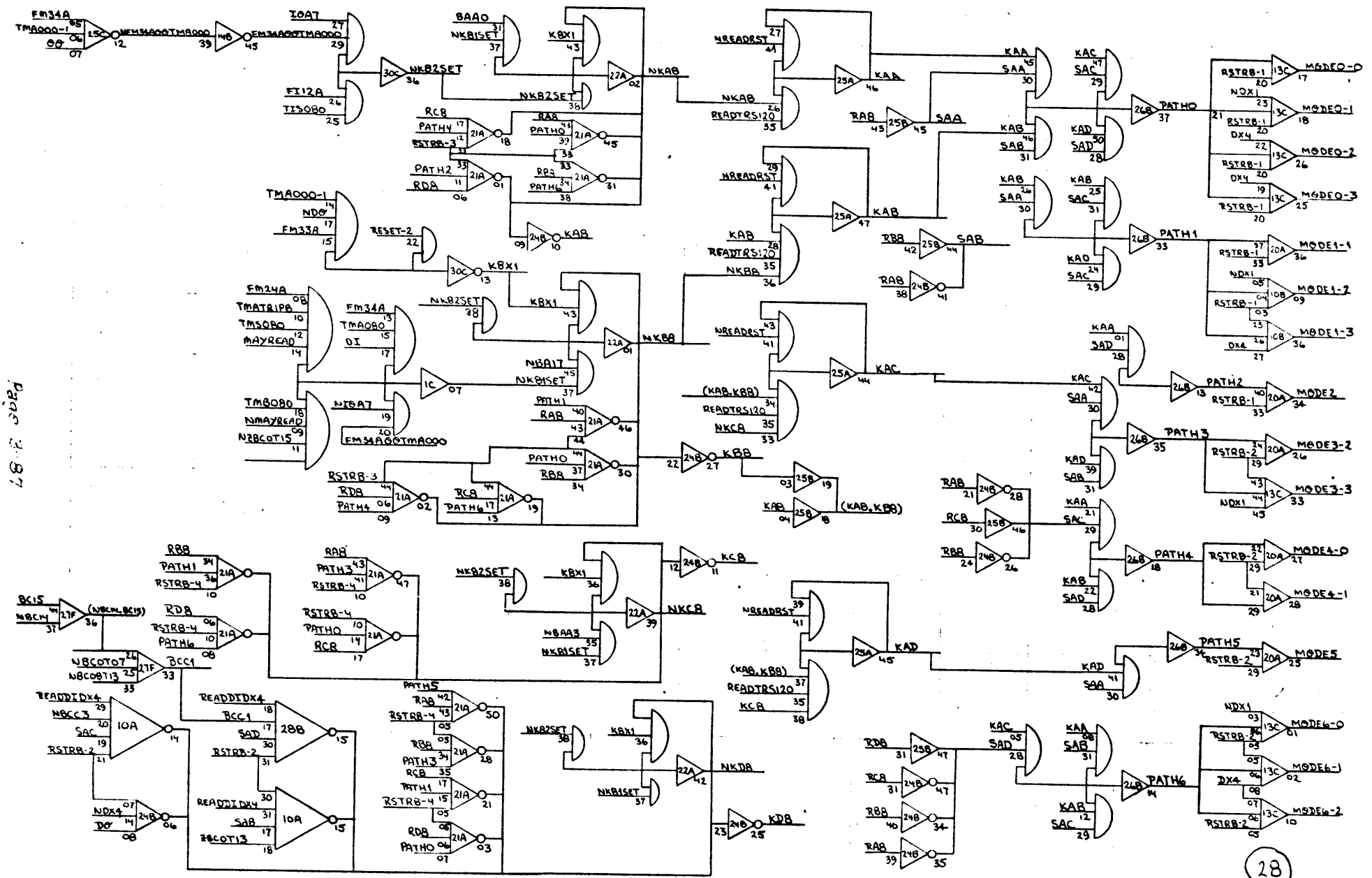
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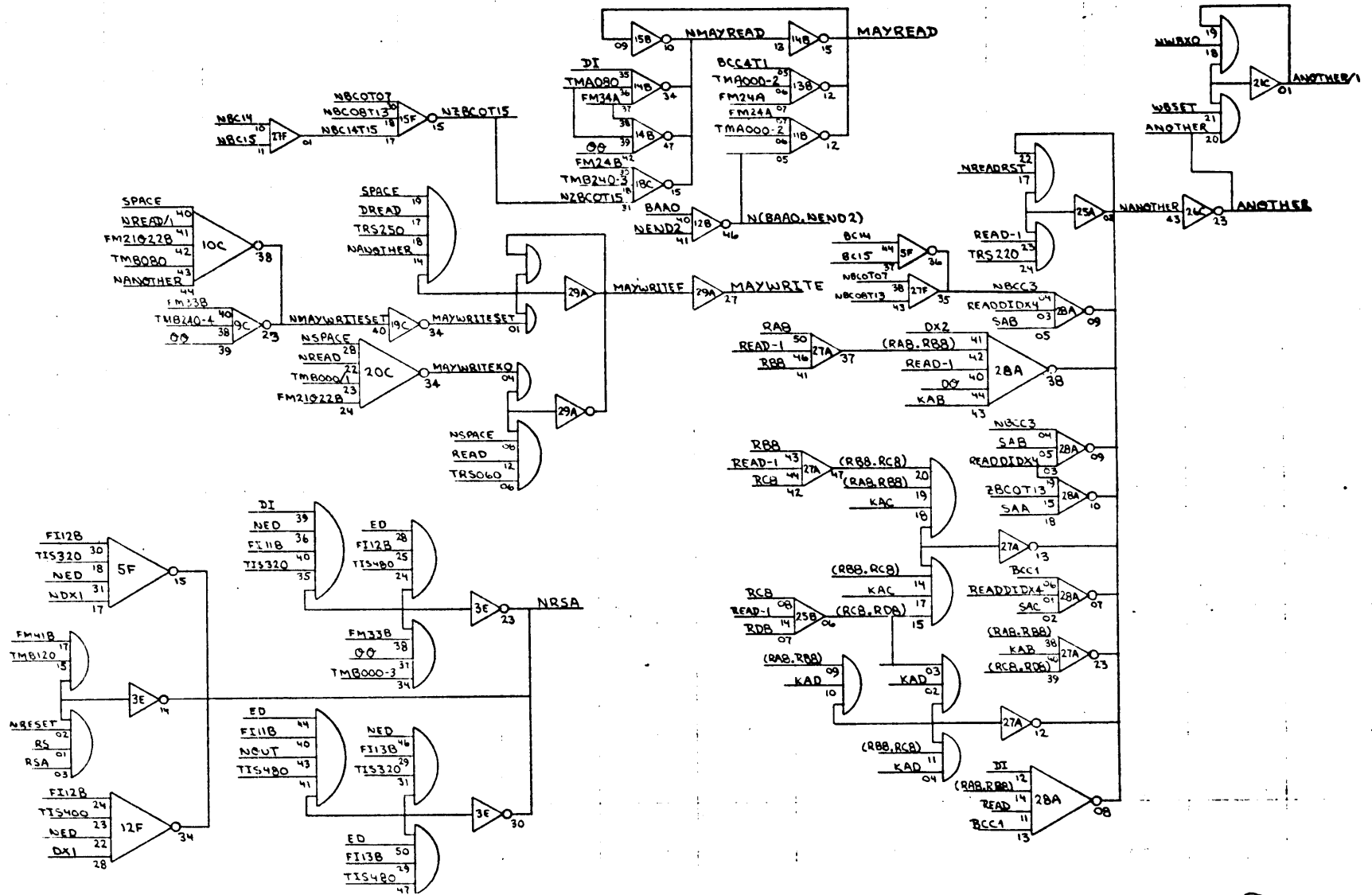




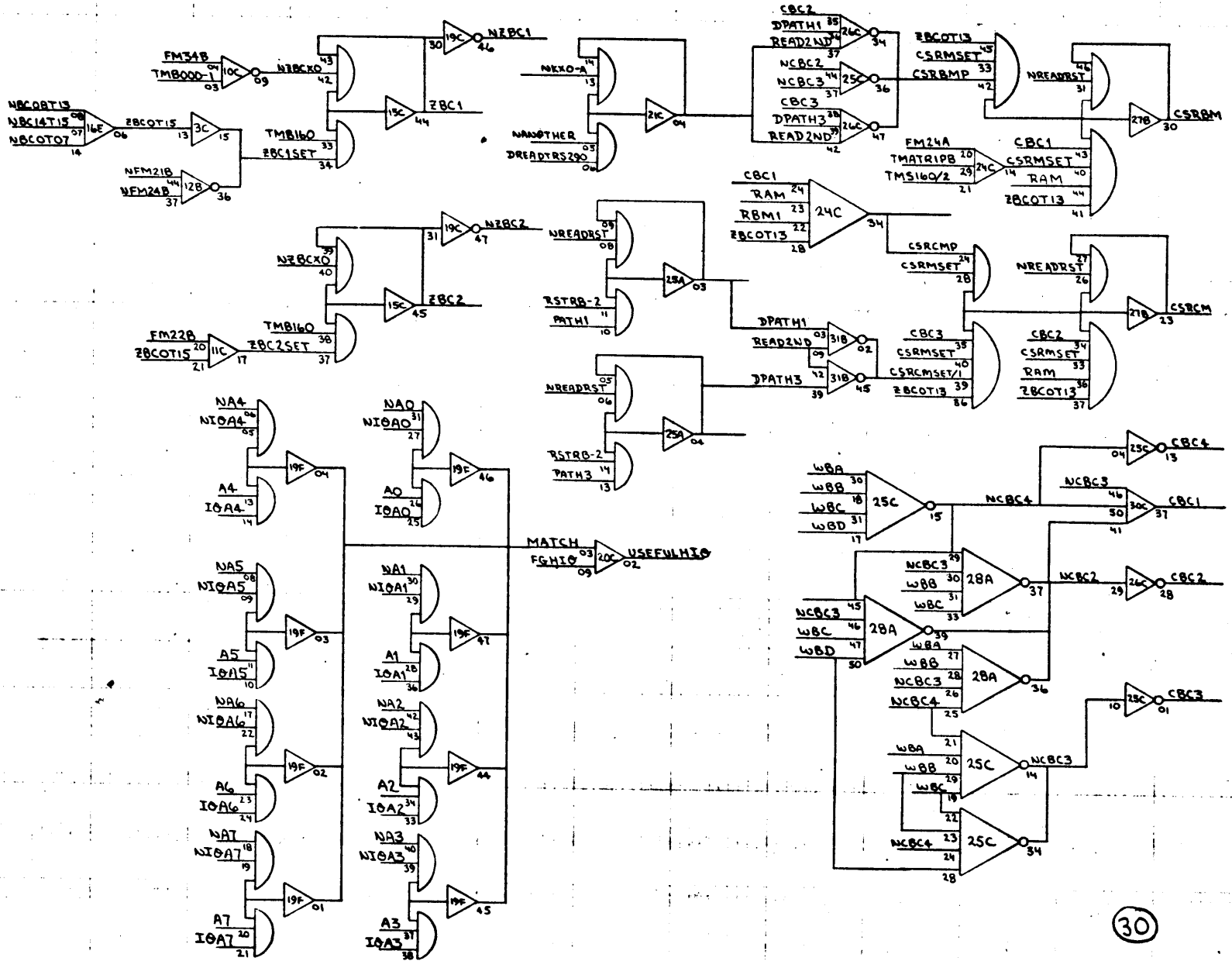




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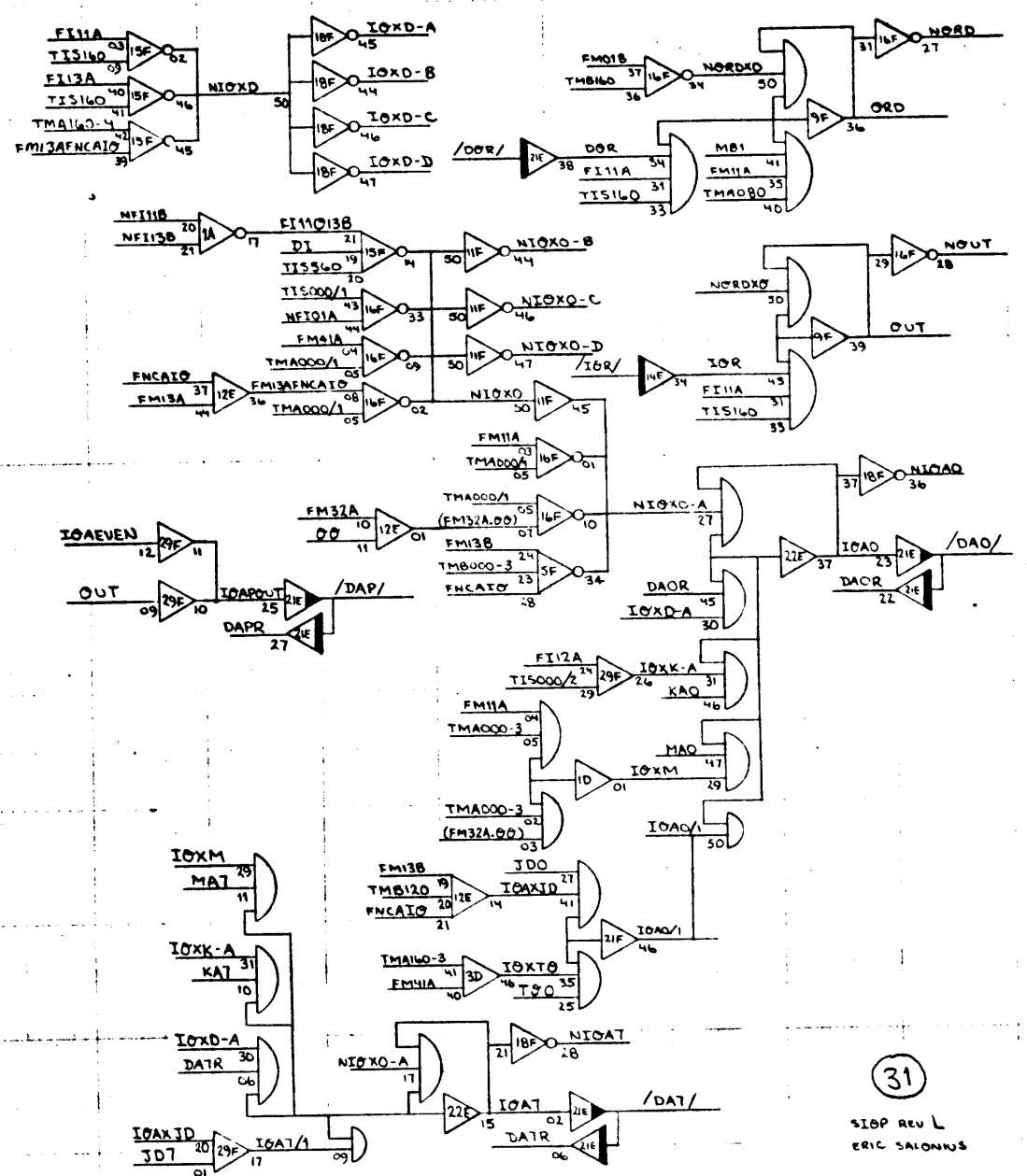
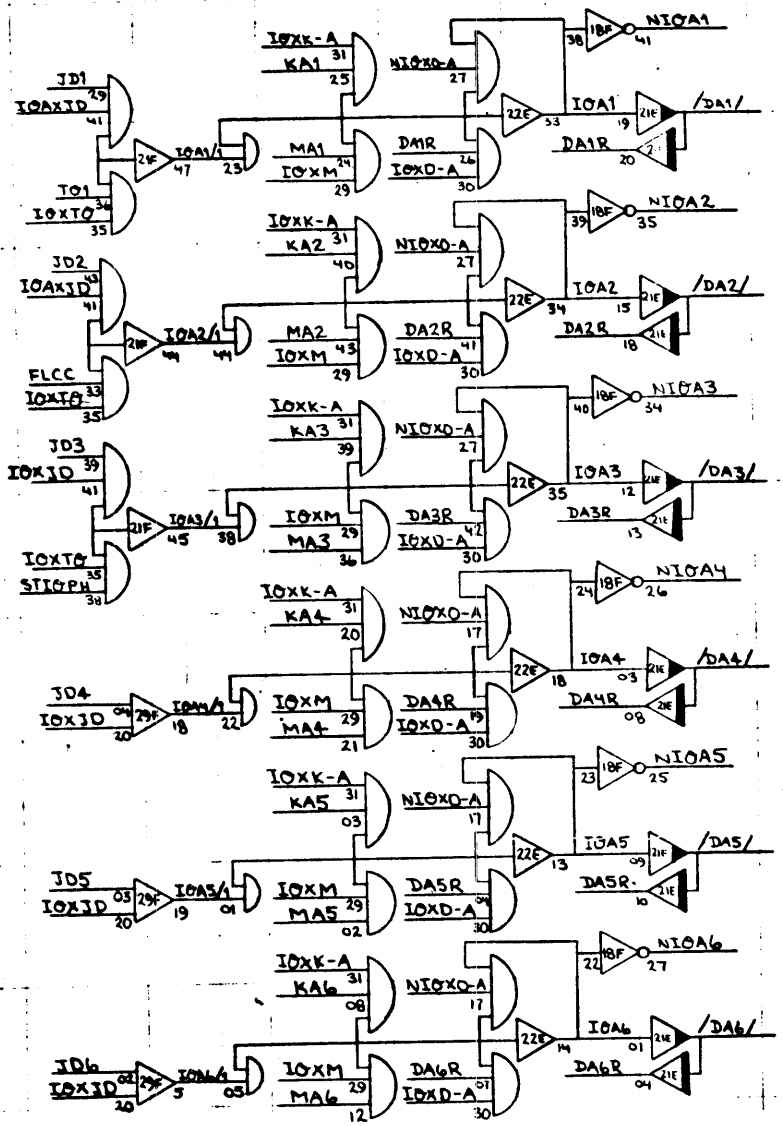


Page 29



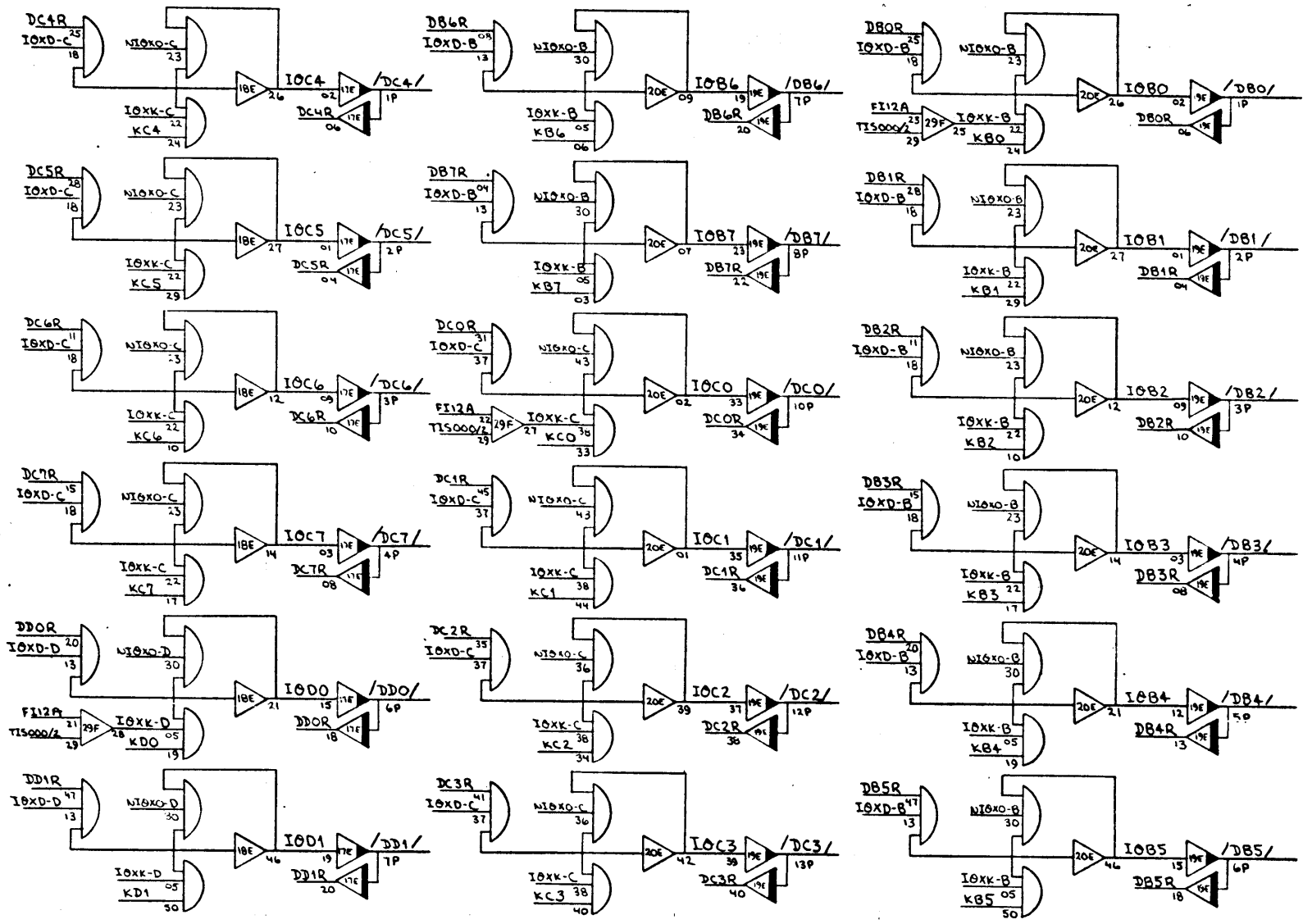
Page 3-89

Page 3-90

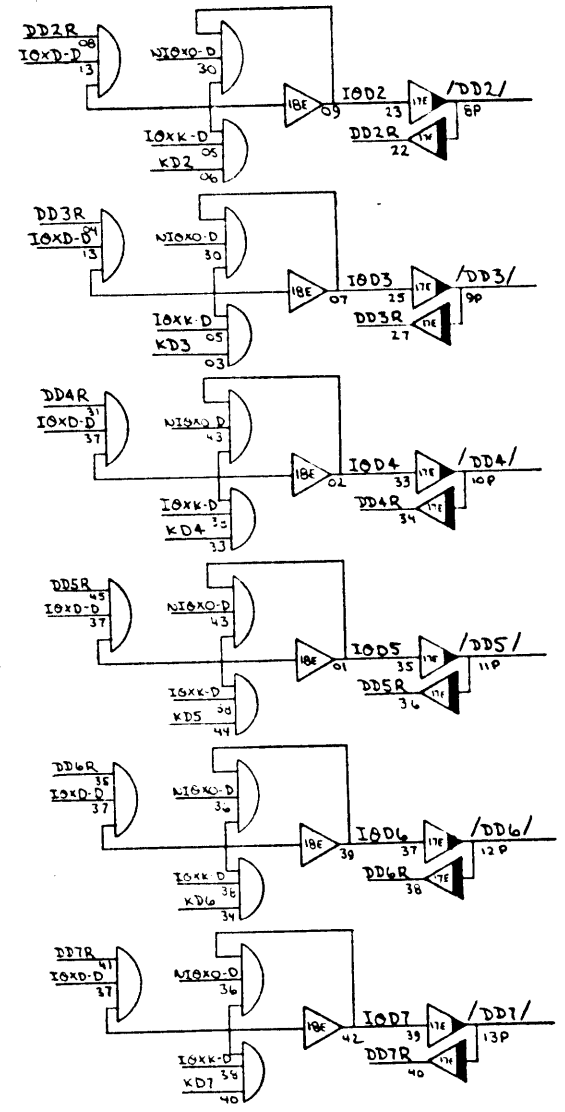
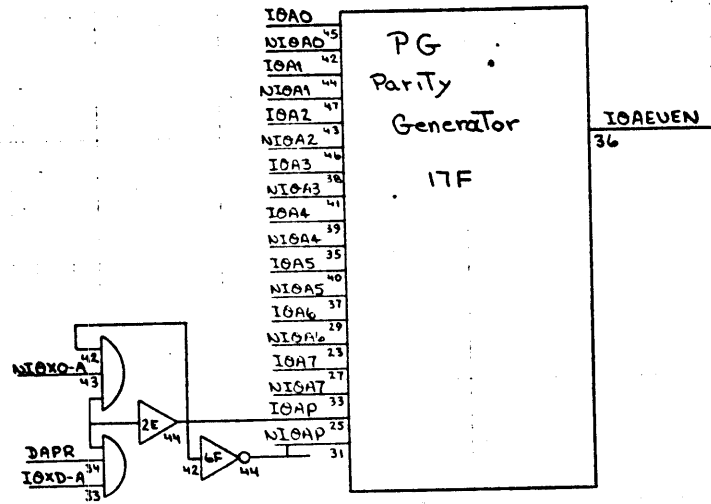


31
 SLOP REV L
 ERIC SALONNUS

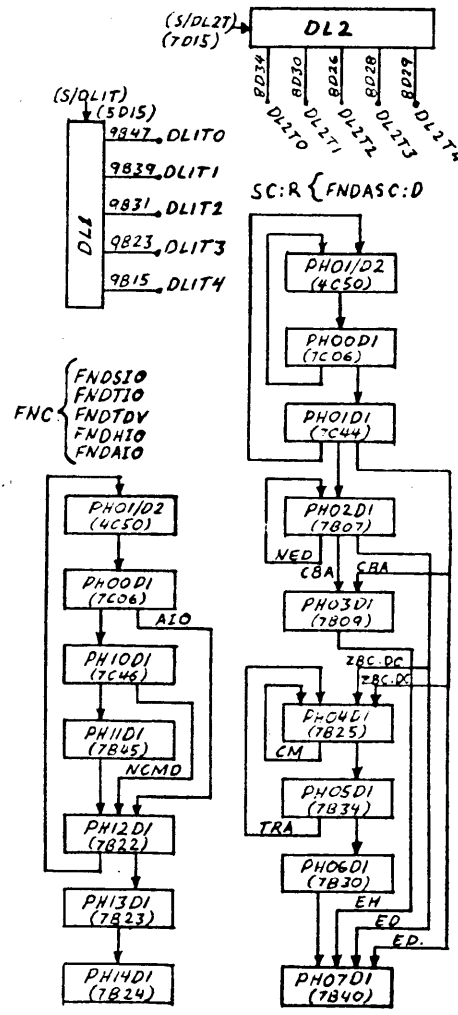
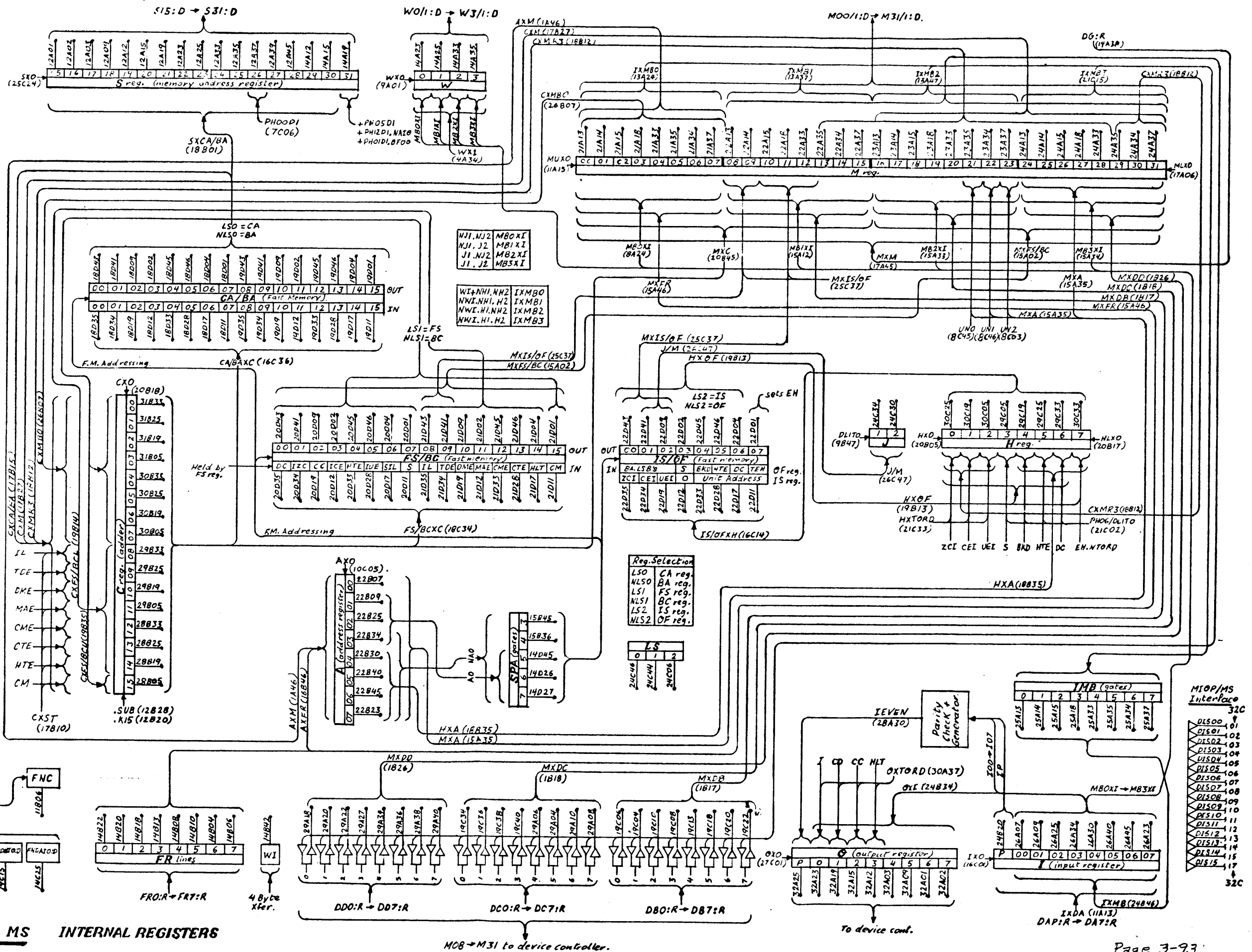
Page 3-91



SIOP Rev L
Eric Salomonus



Signal	Description
BKD	Read backward
CC	Command chain
CD	Count done
CEI	Channel end interrupt
CM	Channeling modifier
CME	IOP memory error
CTE	IOP control error
DC	Data chain
DME	Memory data error
HIT	IOP halt
HTE	Halt on transmission error
I	Interrupt
ICE	Interrupt on channel end
IL	Incorrect length
IUE	Interrupt on unusual end
IZC	Interrupt on zero byte count
MAE	Memory address error
S	Skip
SIL	Suppress incorrect length
TDE	Transmission data error
TEH	Error halt and not term. order
UEI	Unusual end interrupt
ZCI	Zero byte count interrupt



MIOP with MS INTERNAL REGISTERS

M08-M31 to device controller.

D Revision.

MIOP/MS MODULE LOCATION CHART

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	AT11	FT65	LT13	AT11	LT12	FT27	FT65	FT63	FT63	FT63	FT63	XT10	FT27	AT11	IT16	AT11	BT11	AT70	LT13	AT61	IT11	AT11	IT11	LT13	XT10	BT16	BT16	IT11	FT26	BT11	FT66	
B	XT10	FT18	FT18	FT18	FT18	FT27	BT18	XT10	FT66	BT10	FT65	FT67	IT16	IT11	BT11	IT16	IT11	BT11	AT10	FT26	FT66	FT66	BT11	AT24	FT67	FT65	LT21	BT11	XT10	LT20	BT11	BT15
C																																
D																																

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
A	AT56	DT26	AT60	LT89	AT57	LT90	AT83					LT94	LT95	LT26	BT16	AT60	LT71	AT60	FT67	AT11	FT63	AT11	FT63	AT11	FT63	FT63	IT31	BT12	BT31	BT31	BT10	FT66	FT66	FT43

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MIOP Address
(LT26 Loc. BC)

S1-1 = Bit 21 → IOPA0
 S2-1 = Bit 22 → IOPA1
 S3-1 = Bit 23 → IOPA2

LASTONE = S1-2 UP
 FOURBYTE = S2-2 UP
 AIOP = S3-2 UP

MS Address
(LT26 Loc. 2/A)

S1-1 = Bit 26 → A10
 S2-1 = Bit 25 → A09
 S3-1 = Bit 24 → A08
 S4-1 = Bit 23 → A07
 S1-2 = Bit 22 → A06
 S2-2 = Bit 21 → A05
 S3-2 = Bit 20 → A04
 S4-2 = Bit 19 → A03

MS off/on line
(LT94 Loc. 23A)

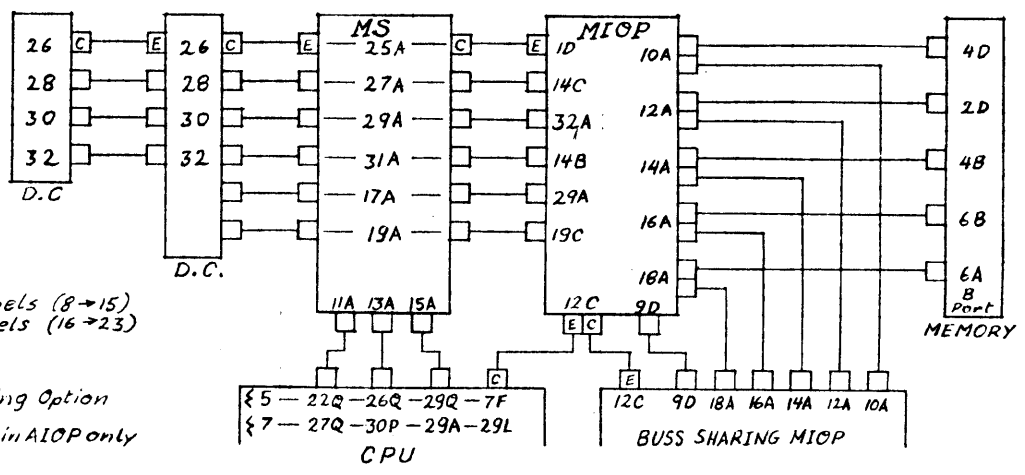
S1 Up = on line
 S1 Down = off line

Note:
 MS Test Mode is not used
 S1 Loc. 22A must be up.

Options

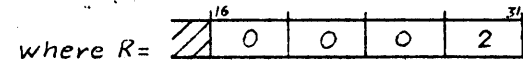
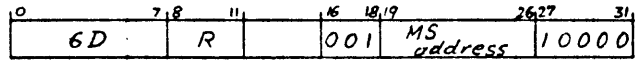
1 = 8 additional channels (8 → 15)
 2 = 8 additional channels (16 → 23)

4B = 4 Byte Option
 BS = Memory Buss Sharing Option
 ABS = Buss Sharing Option in AIOP only

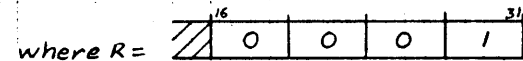
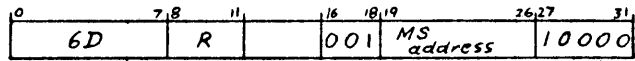


Single Phasing The MIOP.

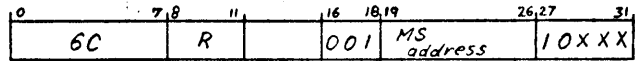
Set MIOP to Single Phase Mode



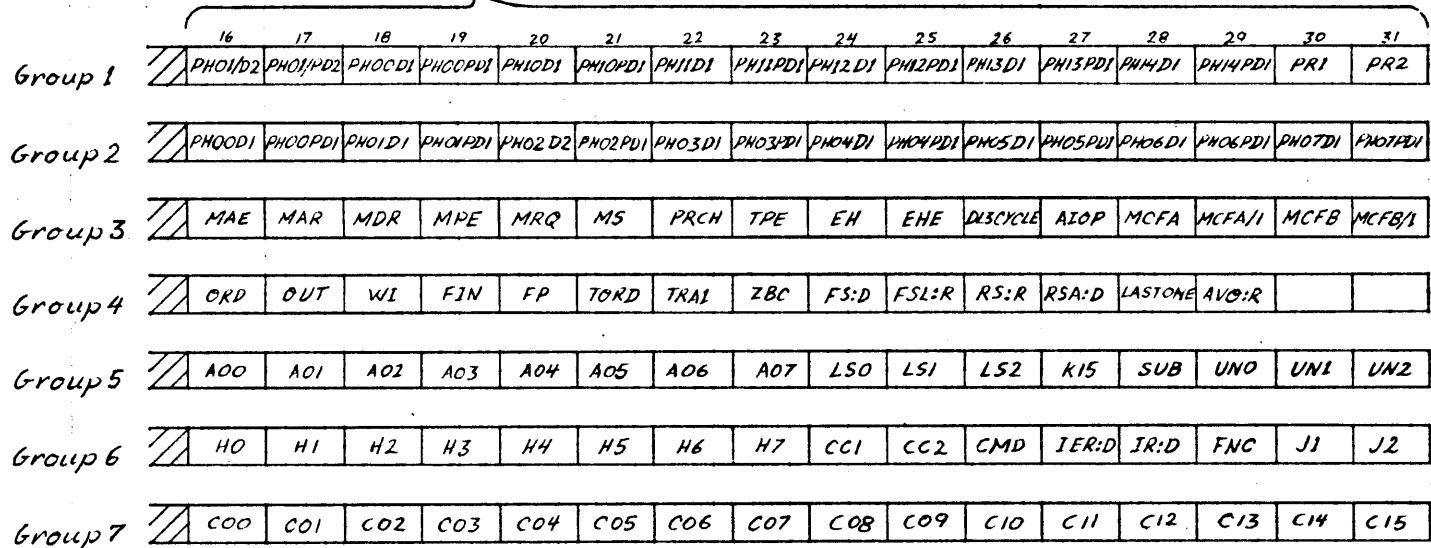
Step to next Phase



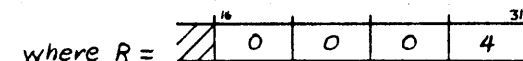
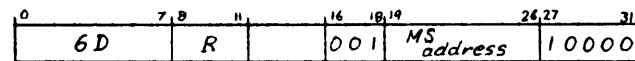
Read MIOP signals



Group 1 → 7



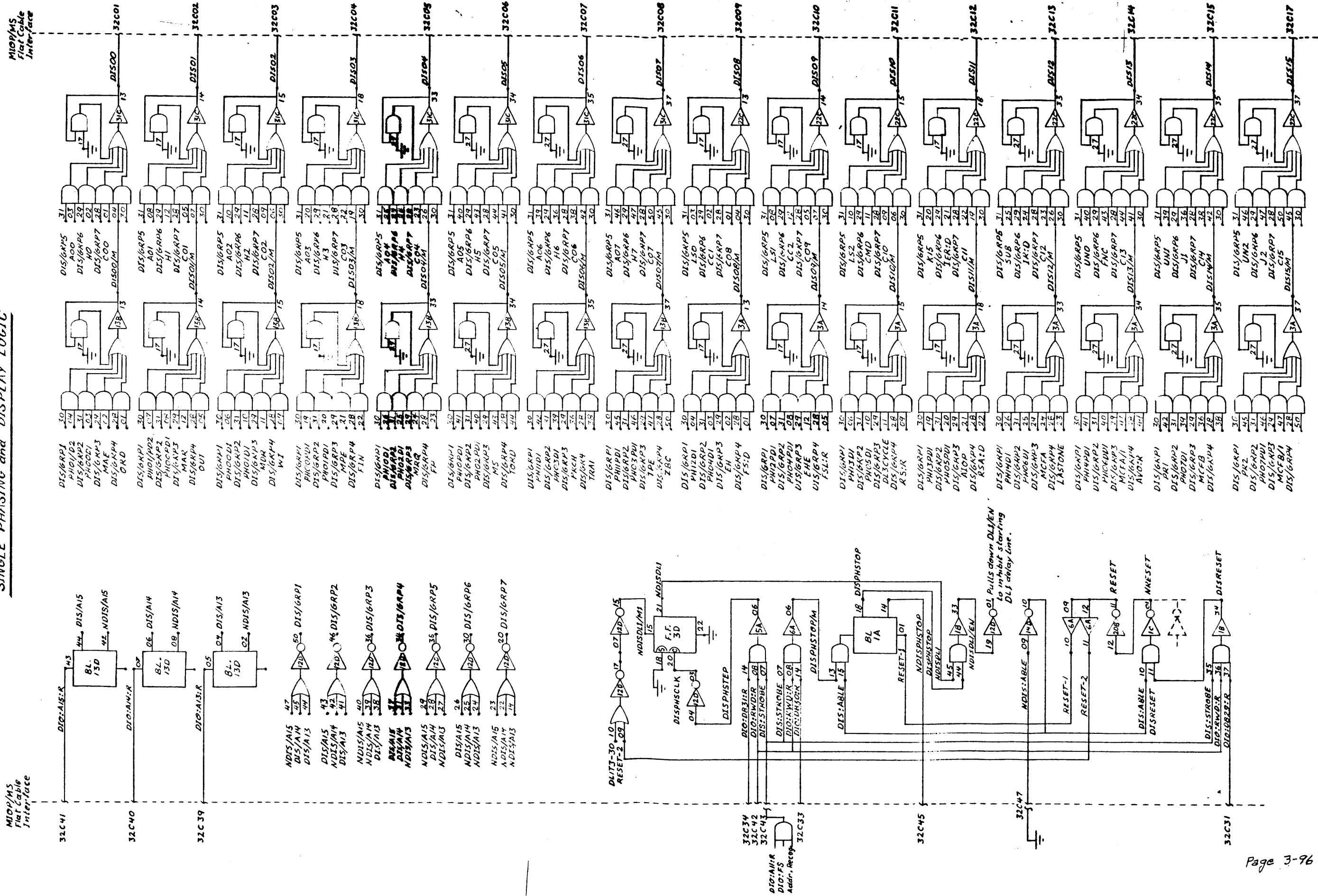
Return MIOP to normal mode



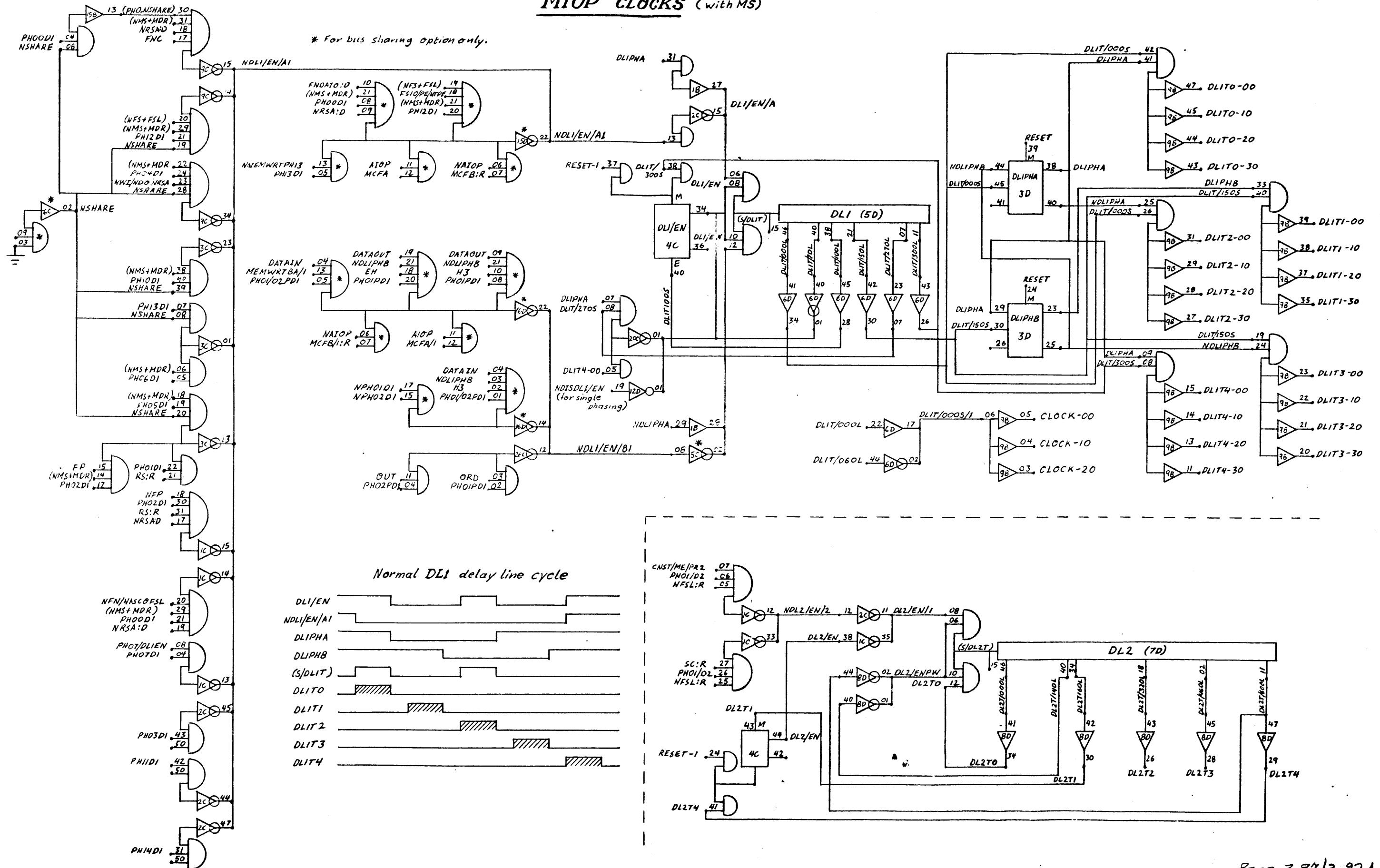
Page 3-95/3-95A

MIOP with MS

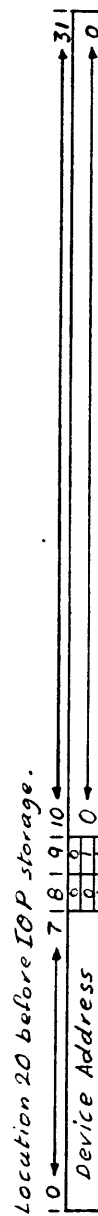
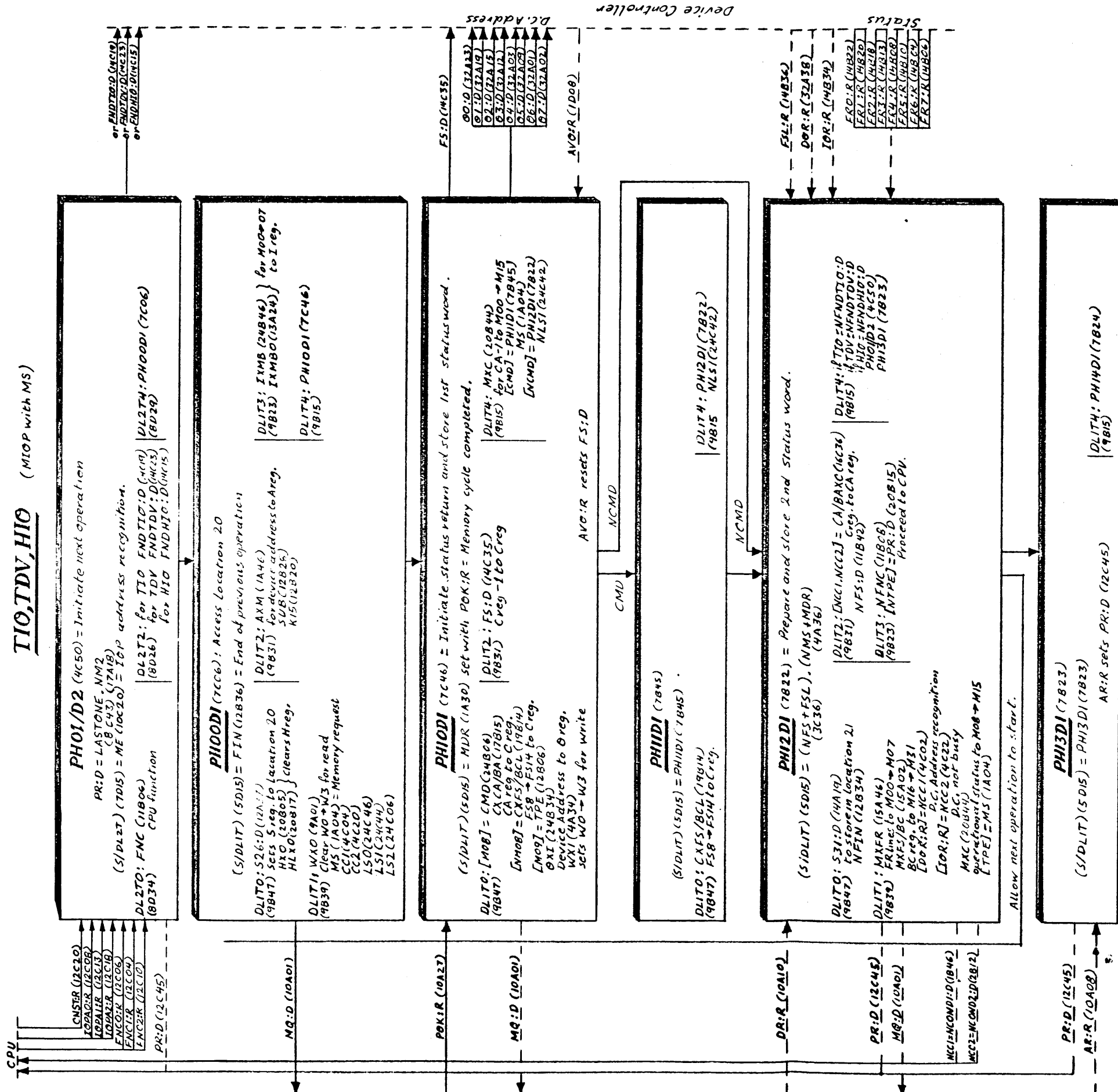
SINGLE PHASING and DISPLAY LOGIC



MIOP CLOCKS (with MS)

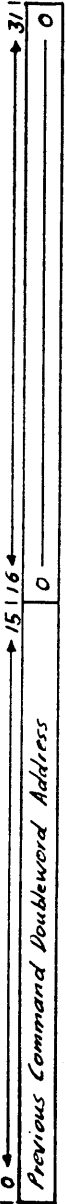


TIO, TDV, HIO (MIOP with MS)

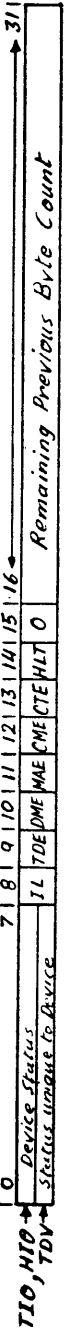


0 0 = No status returned
 0 1 = 1 word of status returned.
 1 1 = 2 words of status returned.

Location 20 after 1st Status word is stored.

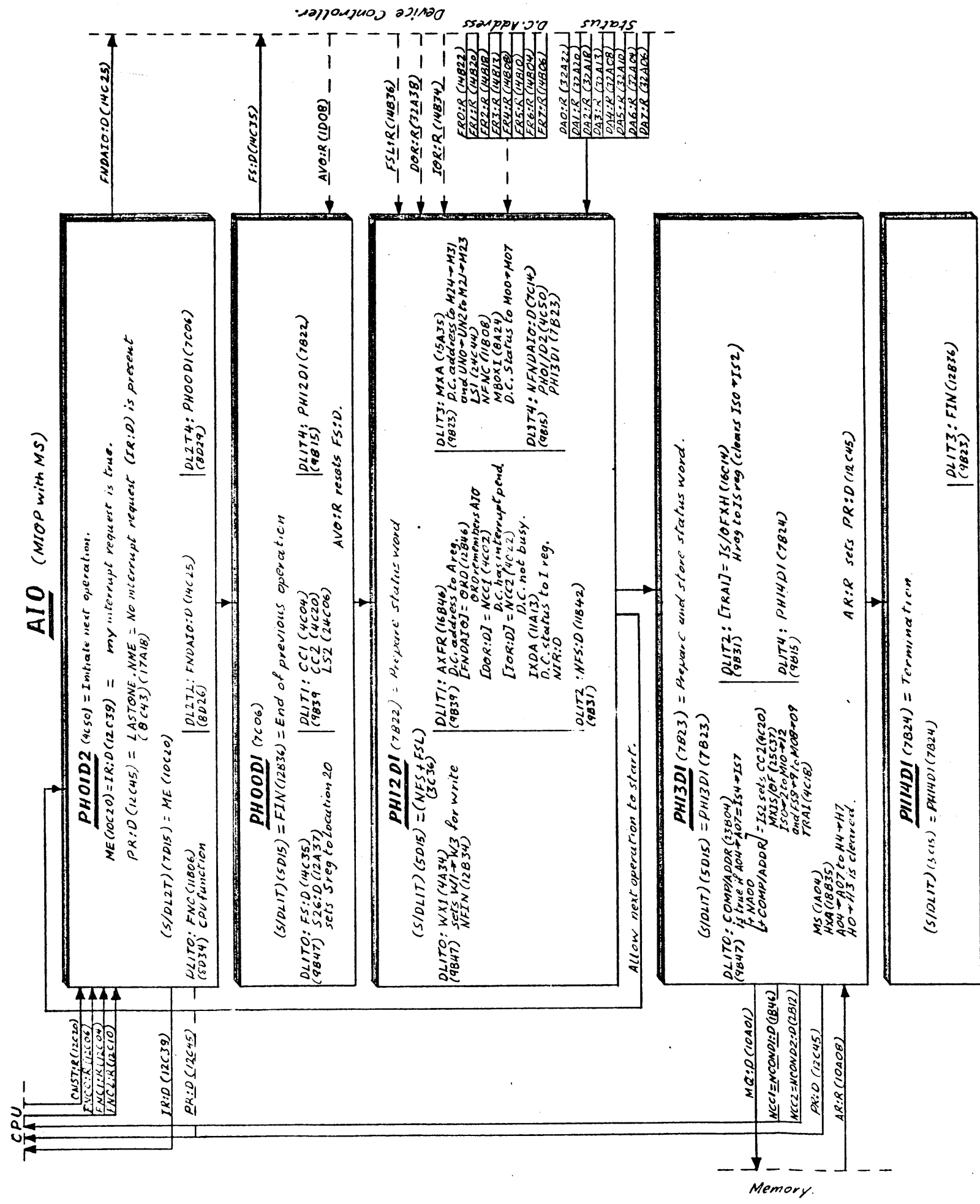


Location 21 after 2nd Status word is stored.



- CME = IOP memory error.
- CTE = IOP control error
- DME = Memory data error
- HLT = IOP halt
- IL = Incorrect length
- MAE = Memory address error
- TDE = Transmission data error

Note: Every PH01/D2 term is reset at T3 time of its delay line
 Every PH01/D2 term is set at T1 time of its delay line and reset at T0 time of its delay line.



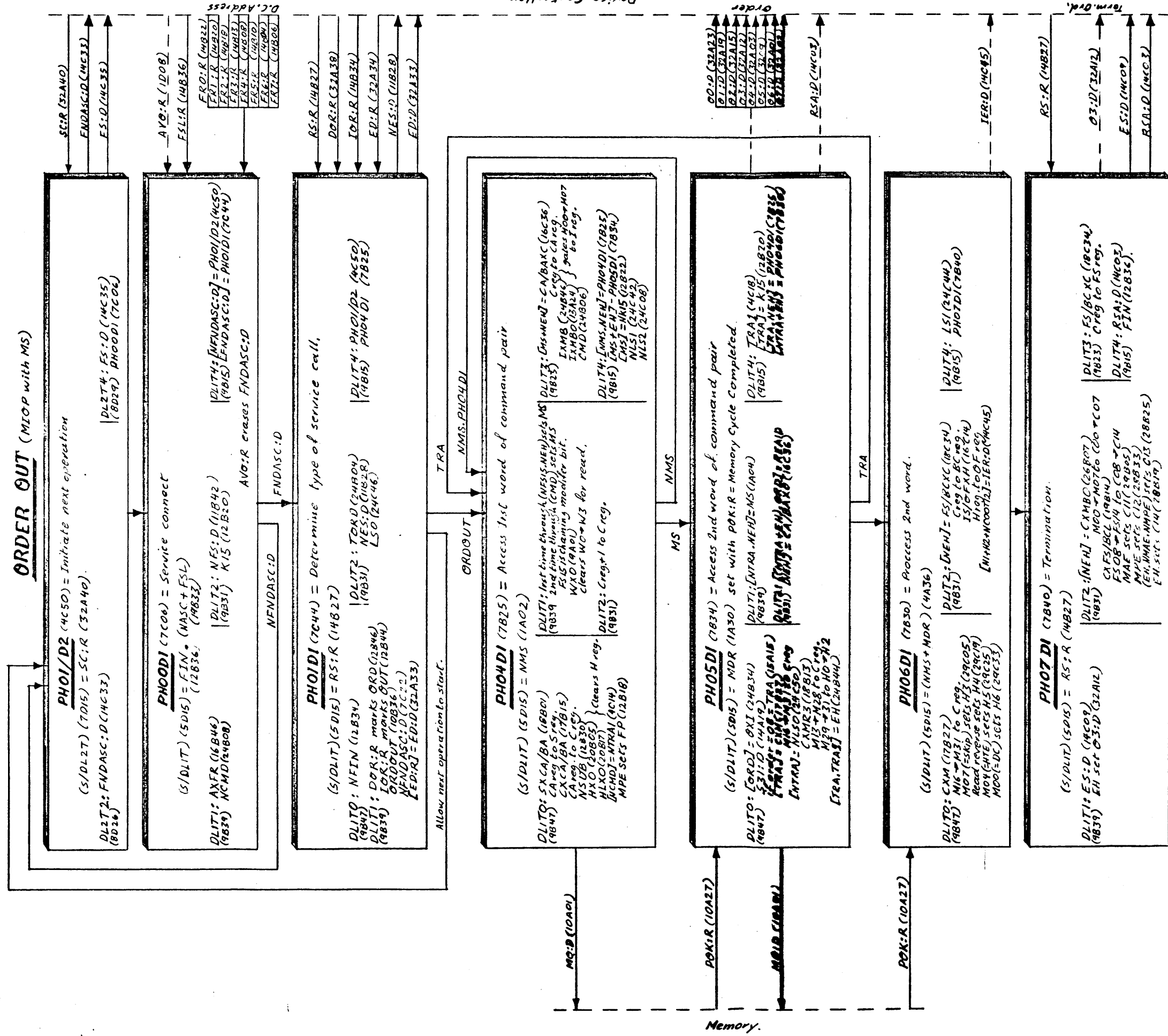
Location 20 after response is stored.

0	7	8	9	10	11	12	13	20	21	23	24	25	27	28	31
Status unique to device				IL	TDE	ZCI	UEI	0	0	TDP#	M	D.C.	D.	I.O. Address	

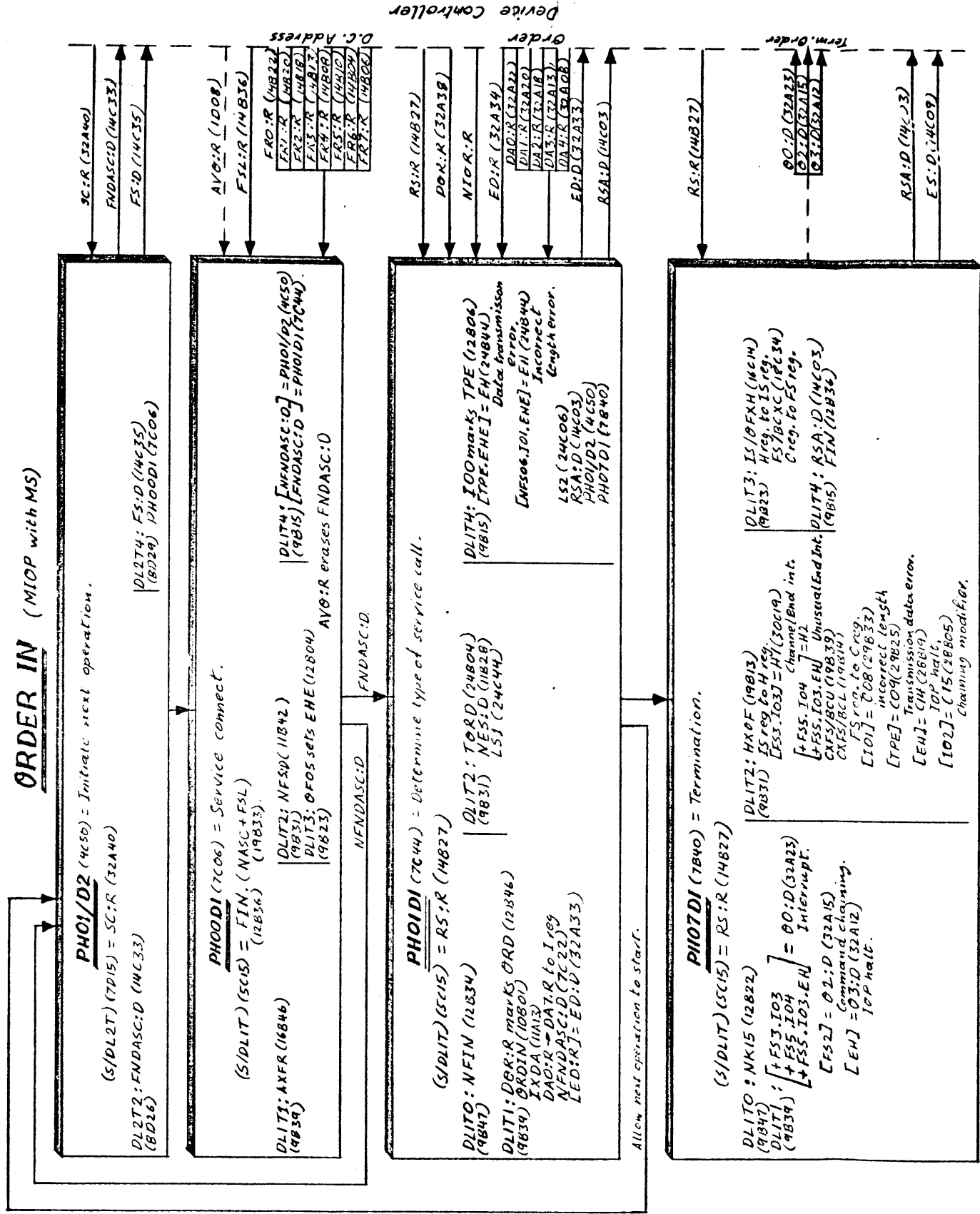
- CEI = Channel end interrupt
- IL = Incorrect length
- TDE = Transmission data error
- UEI = Unusual end interrupt
- ZCI = Zero byte count interrupt

Note: Every PH01/D2 term is reset at T3 time of its delay line. Every PH01/D2 term is set at T1 time of its delay line and reset at T0 time of its delay line.

ORDER OUT (MIOP with MS)



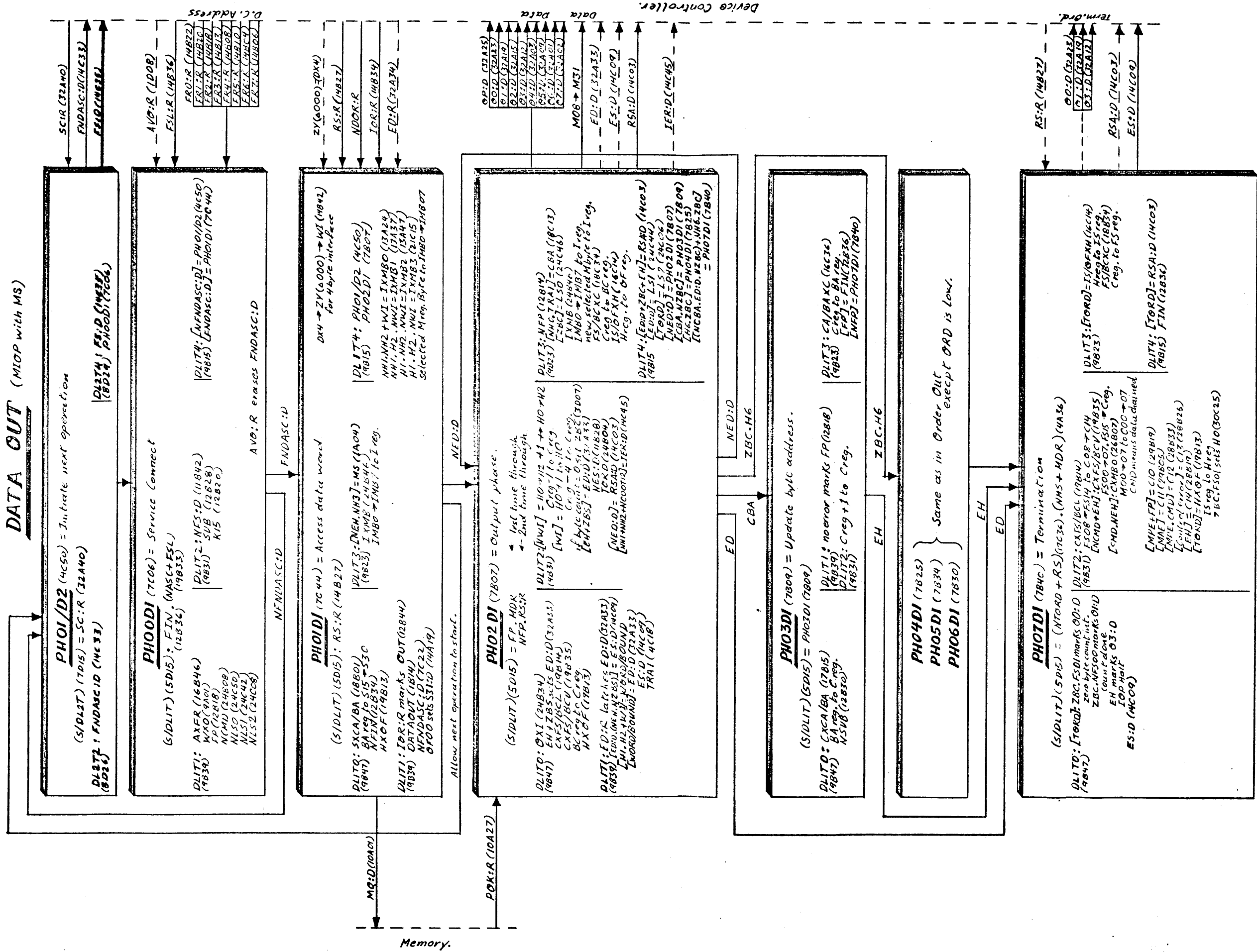
Note: Every PH# DI/D2 is reset at T3 time of its delay line.
 Every PH# DI/D2 is set at T1 time of its delay line and reset at T0 time of its delay line.



Note: Every PHMDI/D2 is reset at T3 time of its delay line.
 Every PHPOI/D2 is set at T1 time of its delay line and reset at T0 time of its delay line.

- ORDER**
 DAO:R = Transmission error
 DA1:R = Incorrect length
 DA2:R = Chaining modifier
 DA3:R = Channel end
 DA4:R = Unusual end.

DATA OUT (MIOP with MS)



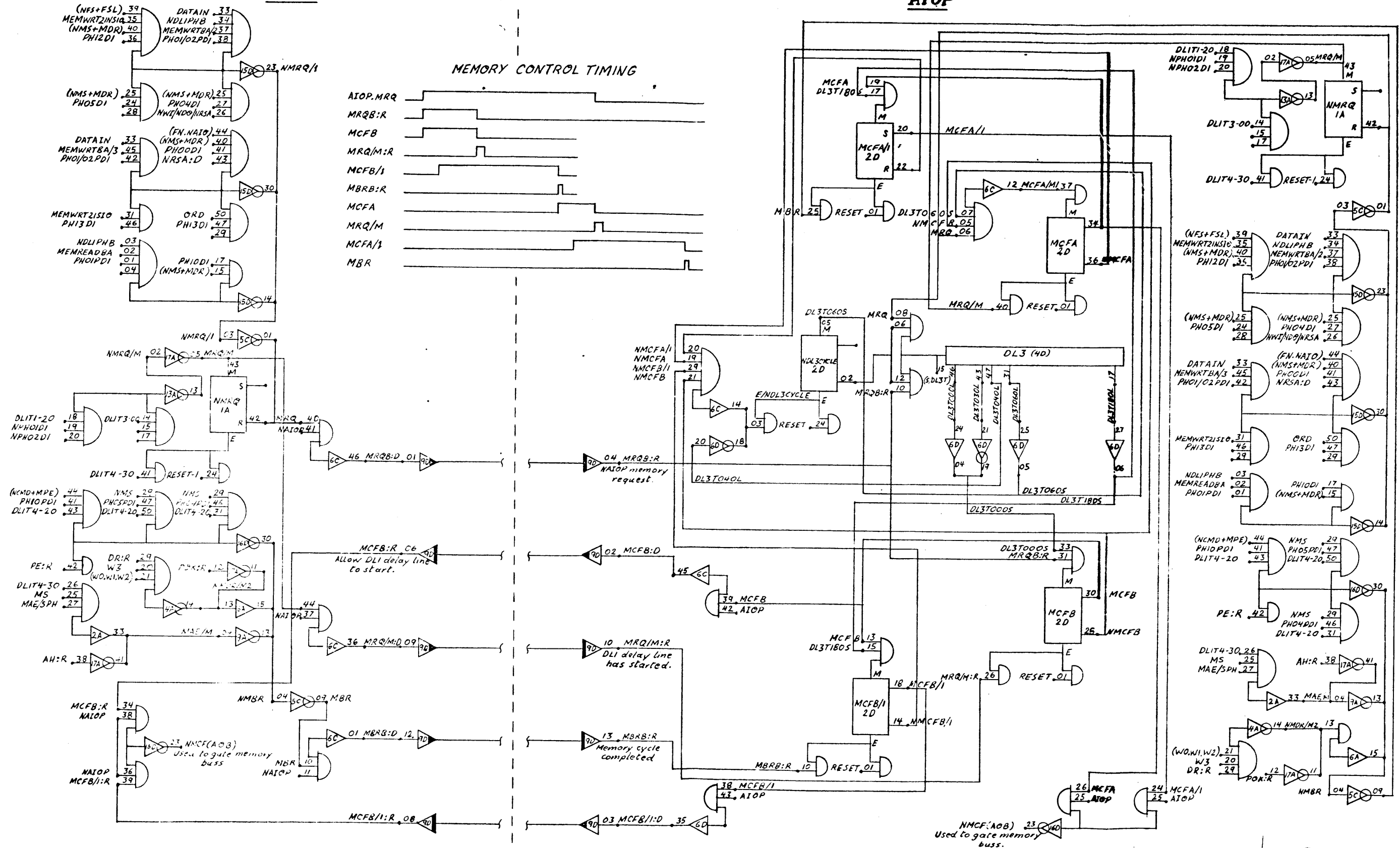
Note: Every PHO5DI/02 term is reset at T3 time of its delay line.
 Every PHO6DI/02 term is set at T1 time of its delay line and reset at T0 time of its delay line.

MIOP with MS - BUSS SHARING OPTION

NAIOP

AIOP

MEMORY CONTROL TIMING



DECIMAL UNIT

PHASE CHARTS

<i>TITLE</i>	<i>PAGE</i>
<i>MODULE LOCATION CHART</i>	<i>1</i>
<i>DECIMAL UNIT REGISTERS</i>	<i>2</i>
<i>DECIMAL LOAD</i>	<i>3</i>
<i>DECIMAL STORE</i>	<i>4</i>
<i>DECIMAL COMPARE</i>	<i>5</i>
<i>DECIMAL ADD</i>	<i>6</i>
<i>DECIMAL SUBTRACT</i>	<i>7</i>
<i>DECIMAL MULTIPLY</i>	<i>8</i>
<i>DECIMAL DIVIDE</i>	<i>9</i>
<i>DECIMAL SHIFT ARITHMETIC</i>	<i>10</i>
<i>PACK DECIMAL DIGITS</i>	<i>11</i>
<i>UNPACK DECIMAL DIGITS</i>	<i>12</i>
<i>EDIT BYTE STRING</i>	<i>13</i>

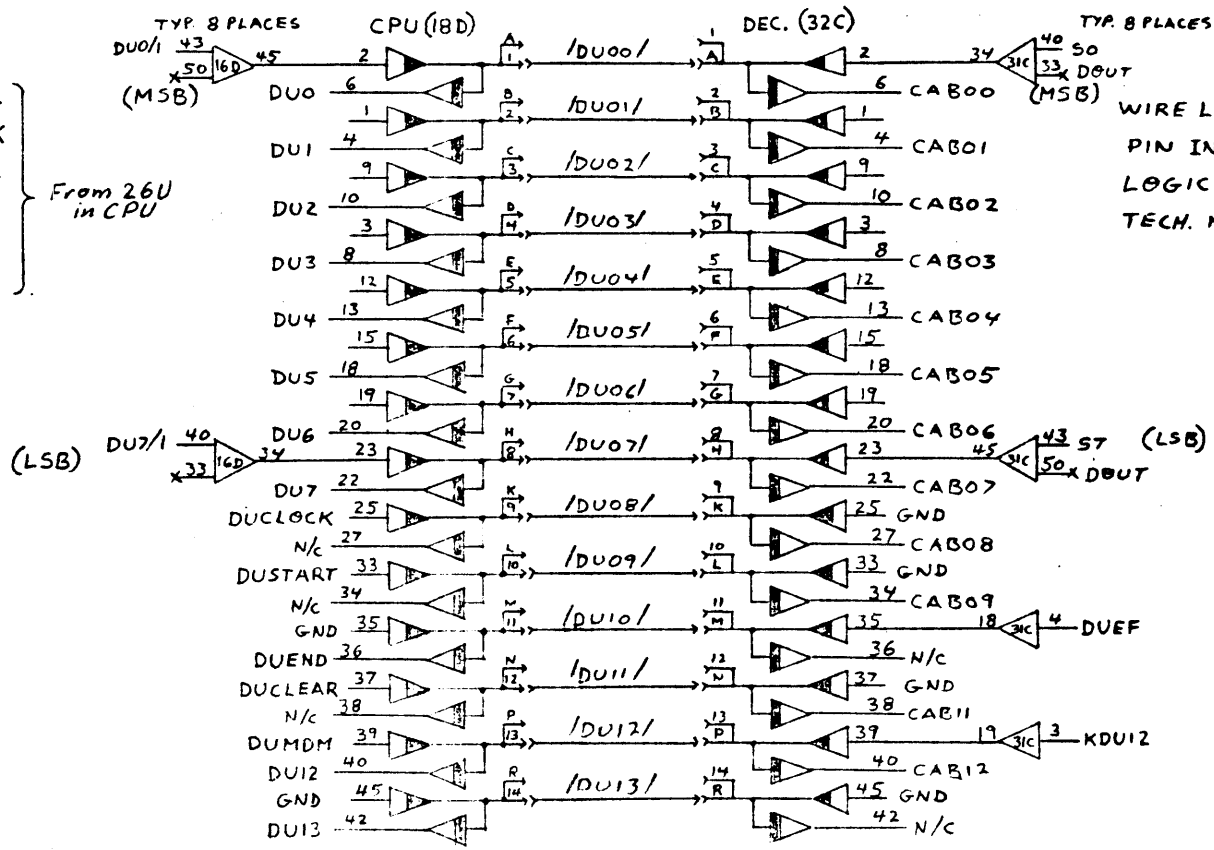
DECIMAL UNIT MOD. 8419

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
A	LT	BT	GT	FT	GT	LT	LT	FT	XT	LT	FT	BT	LT	BT	LT	LT	LT	FT	FT	FT	BT	IT	FT	LT	XT	GT	FT	GT	GT	LT	BT	IT	A	
	21	11	11	22	11	21	21	18	10	21	18	18	21	10	21	21	21	25	25	25	10	16	18	21	10	11	22	11	11	21	18	25		
																		DAO ↓ DA7	DB0 ↓ DB7	E00 ↓ E07														
B	ZT	LT	LT	LT	FT	XT	LT	IT	BT	BT	FT	FT	FT	LT	LT	LT	IT	LT	BT	FT	FT	BT	BT	FT	GT	LT	XT	BT	BT	LT	IT	LT	B	
	23	21	21	21	18	10	21	16	11	10	26	17	17	21	21	21	15	21	18	17	17	18	10	22	11	21	10	11	11	21	16	21		
	CL'S CK																																	
C	AT	BT	LT	LT	LT	LT	XT	BT	IT	LT	LT	LT	LT	LT	LT	LT	LT	BT	FT	GT	FT	BT	IT	IT									C	
	11	16	12	12	12	12	18	10	10	16	12	12	18	21	21	20	12	21	11	22	11	22	11	16	25									
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		

CLOCKS COAX

- 32B01 → 25A01 CL
- 32B03 → 13A13 CK
- 32B07 → 8A01 CL
- 32B10 → 21B01 CL
- 32B14 → 12B01 CL
- 32B18 → 13C01 CL

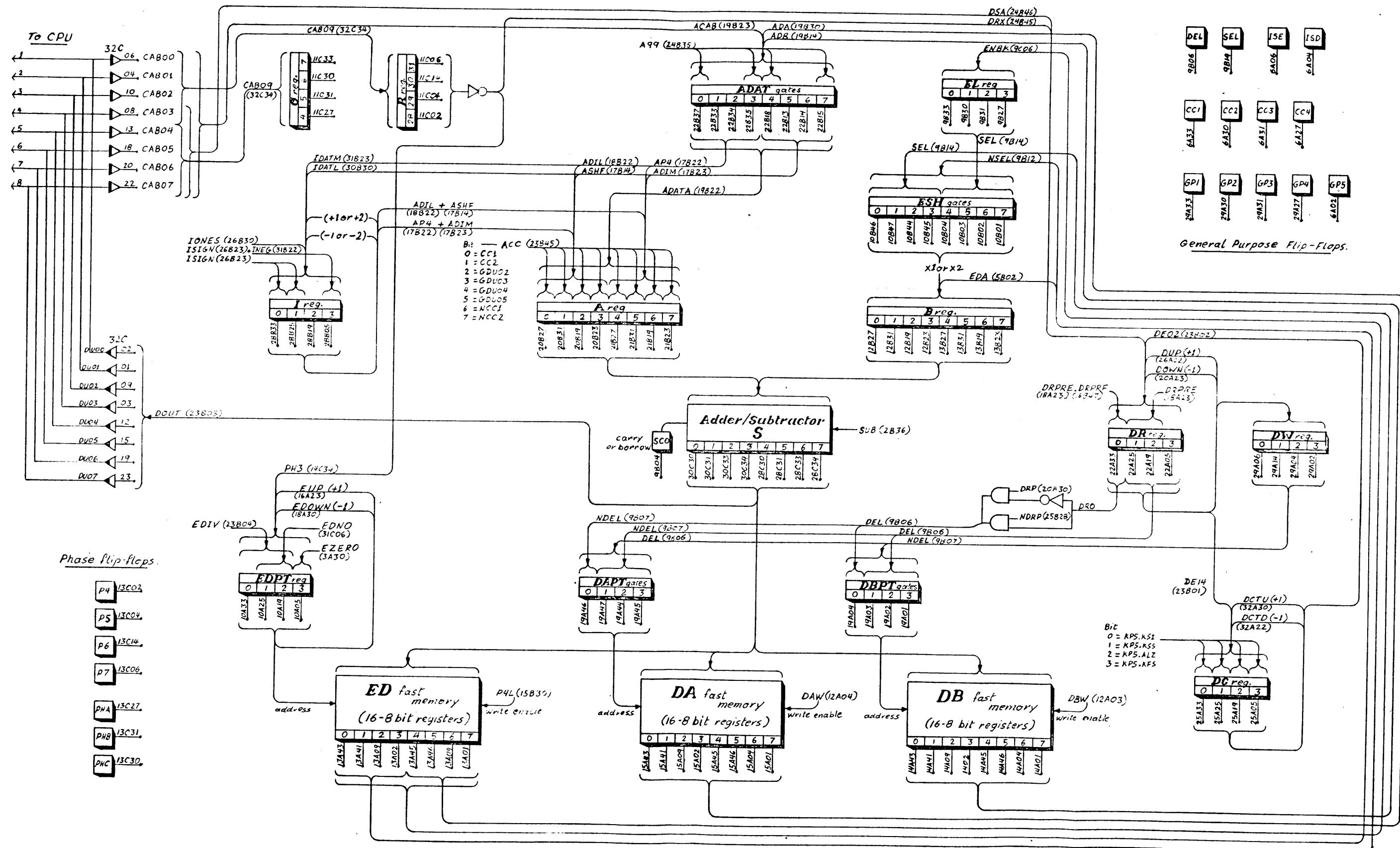
From 26U
in CPU



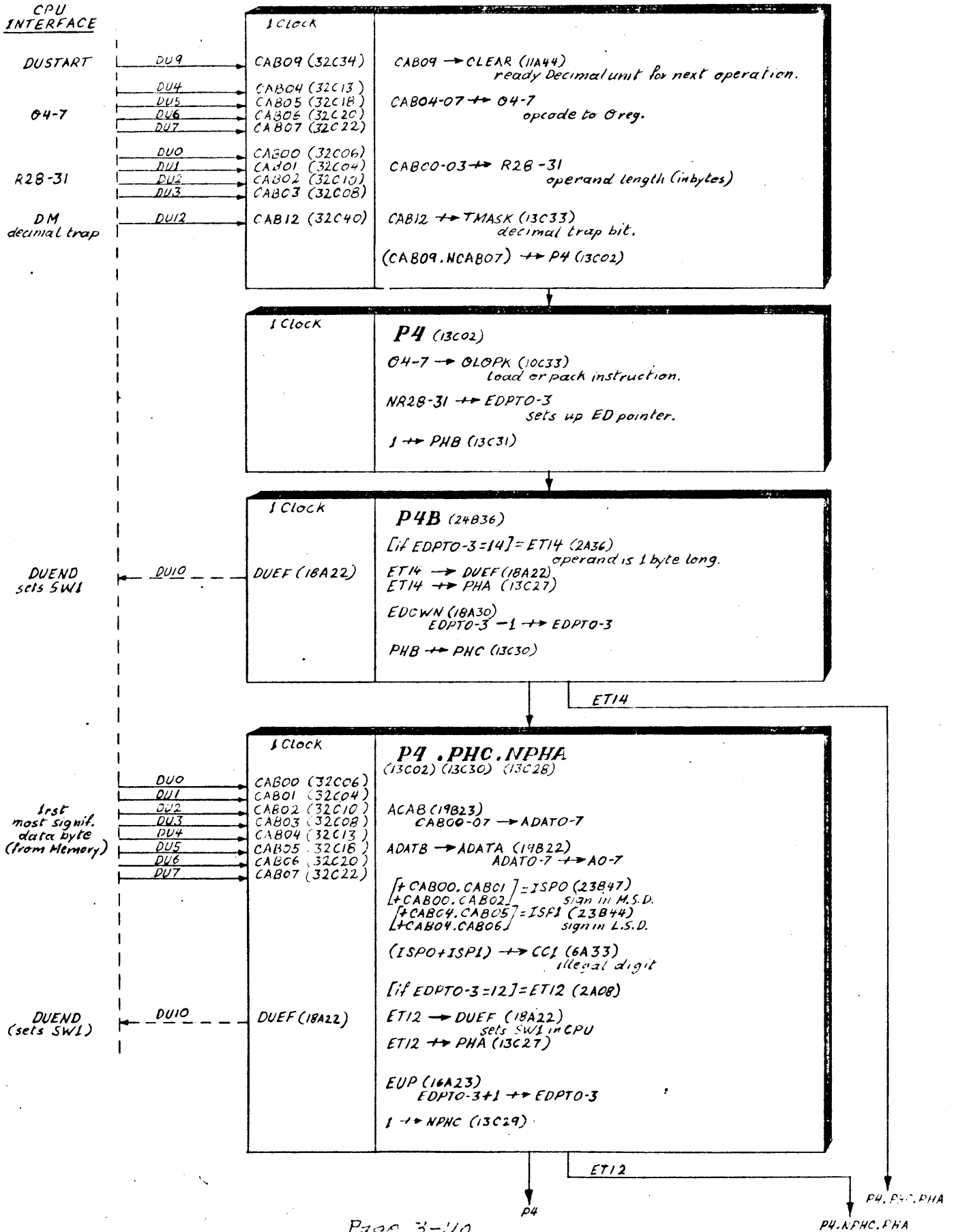
WIRE LIST 124822-001
PIN INDEX 124822-903
LOGIC EQU 124821-001
TECH. MAN. 901587A

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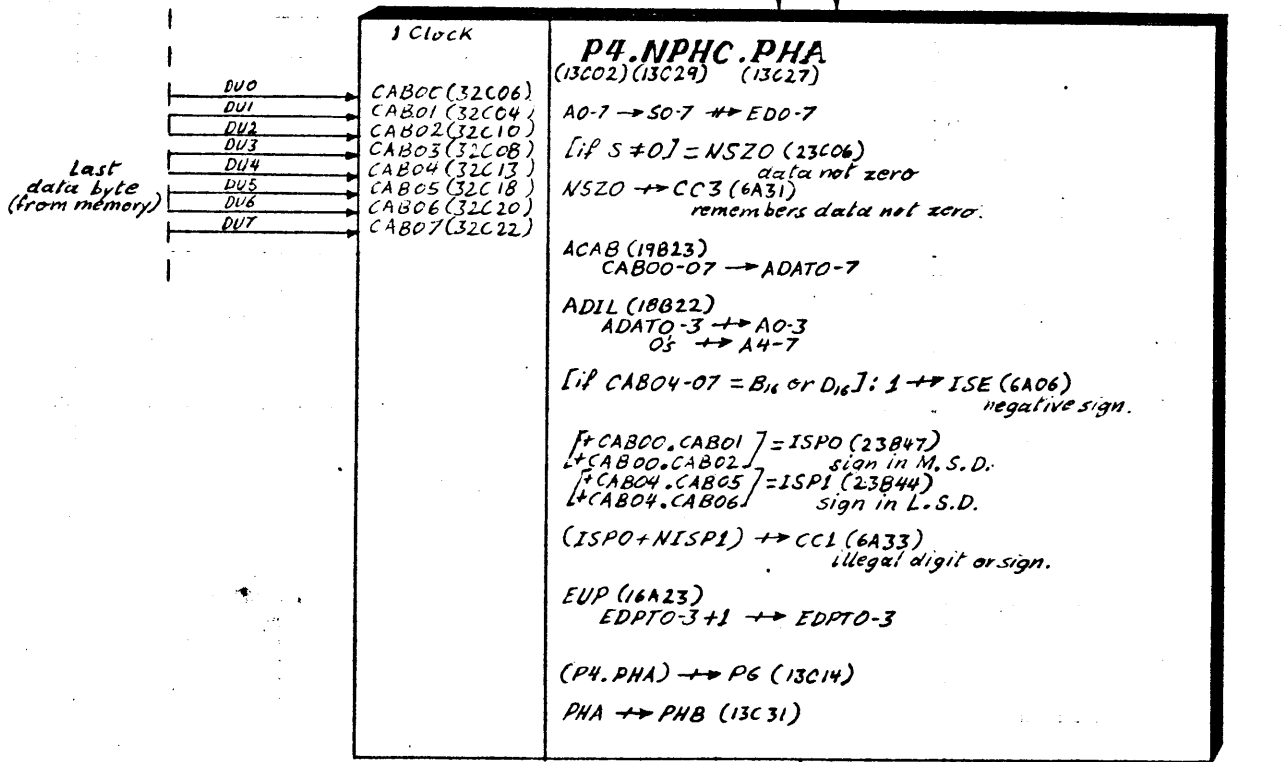
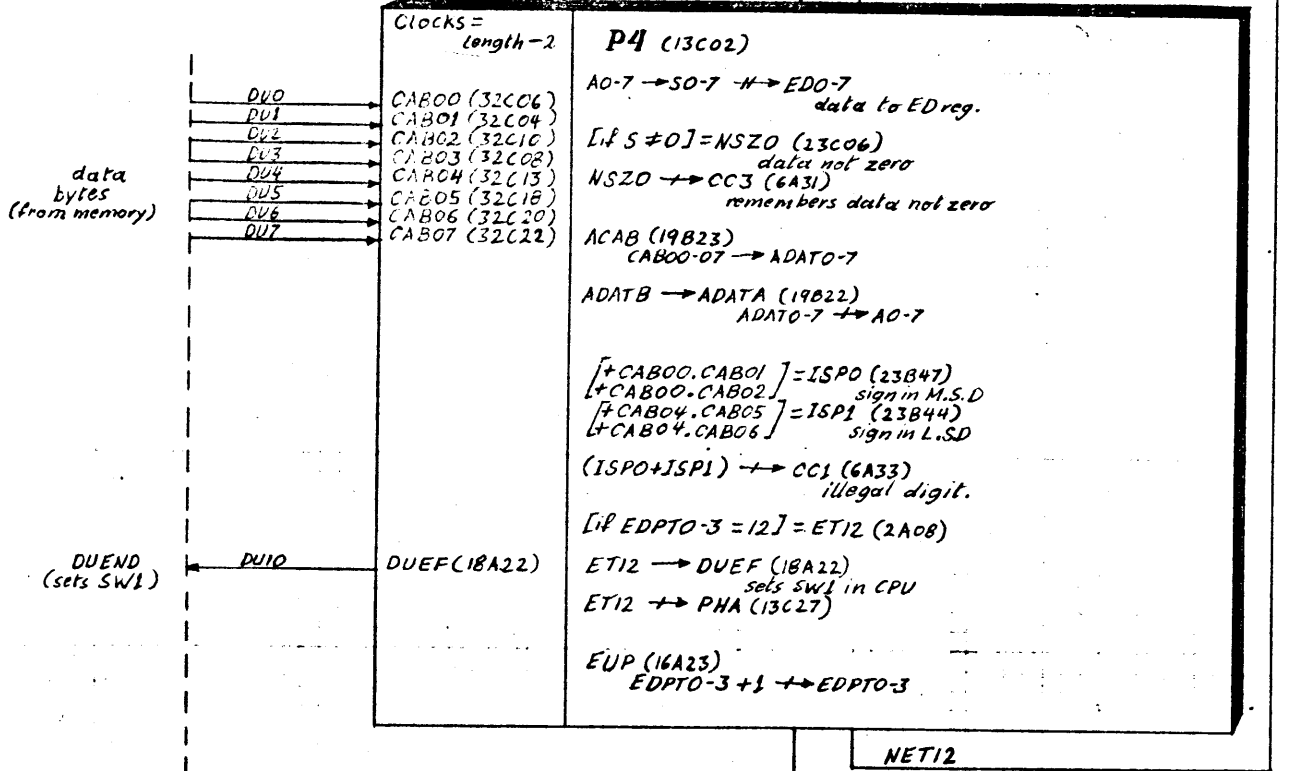
DECIMAL UNIT REGISTERS



DECIMAL LOAD (7E)

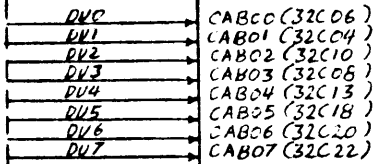


DECIMAL LOAD CONTINUED



DECIMAL LOAD CONTINUED

Single data byte (from memory)



1 Clock

P4, PHC, PHA (1 byte operand)
 (13C02) (13C30) (13C27)

ACAB (19B23)
 CAB00-07 → ADAT0-7

ADIL (18B22)
 ADAT0-3 → A0-3
 05 → A4-7

[if CAB04-07 = B₁₆ or D₁₆]: 1 → JSE (6A06)
 negative sign.

[+CAB00.CAB01] = ISPO (23B47)
 sign in M.S.D.
 [+CAB02.CAB03] = ISPI (23B44)
 sign in L.S.D.

(ISPO+NTSPI) → CC1 (6A33)
 illegal digit or sign.

EUP (16A23)
 ... EDPT0-3 + 1 → EDPT0-3

(P4.PHA) → P6 (13C14)
 PHA → PHB (13C31)

1 Clock

P6B (14C36)

A0-7 → S0-7 → EDO-7
 last byte to EDreg. (loc. 14)

[if S0-7 ≠ 0]: 1 → CC3 (6A31)

PHB → PHC (13C30)

1 Clock

P6C (14C01)

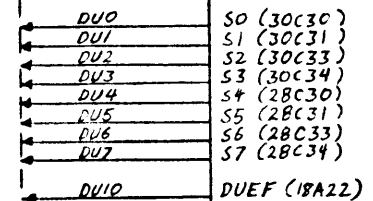
ACC (23B45)
 CC1 → A0 (20B27)
 (NISE.CC3) → A2 (21B19)
 (ISE.CC3) → A3 (21B23)
 (CC1.TMASK) → A4 (21B27)
 (CC1.NTMASK) → A5 (21B31)
 NCC1 → A6 (21B19)
 NCC2 → A7 (21B23)

EDIV (23B04)
 14 → EDPT0-3

[ISE]: D → I0-3
 [NISE]: C → I0-3

PHC → PHA (13C27)

Condition code @ abort info.



1 Clock

P6, PHA
 (13C14) (13C27)

A0-7 → S0-7

DOUT (23B03)
 S0-7 → DU0-7

DUEF (18A22)

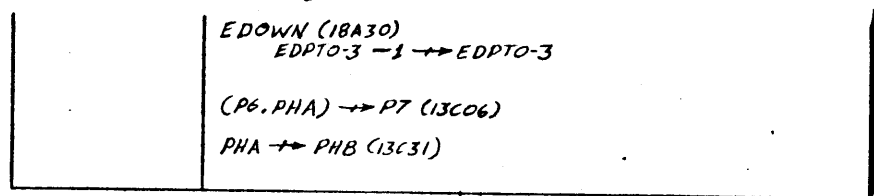
ADIL (18B22)
 I0-3 → A4-7
 sign.

ESL (9A30)
 EDO-7 → B0-7
 L.S. Byte of data

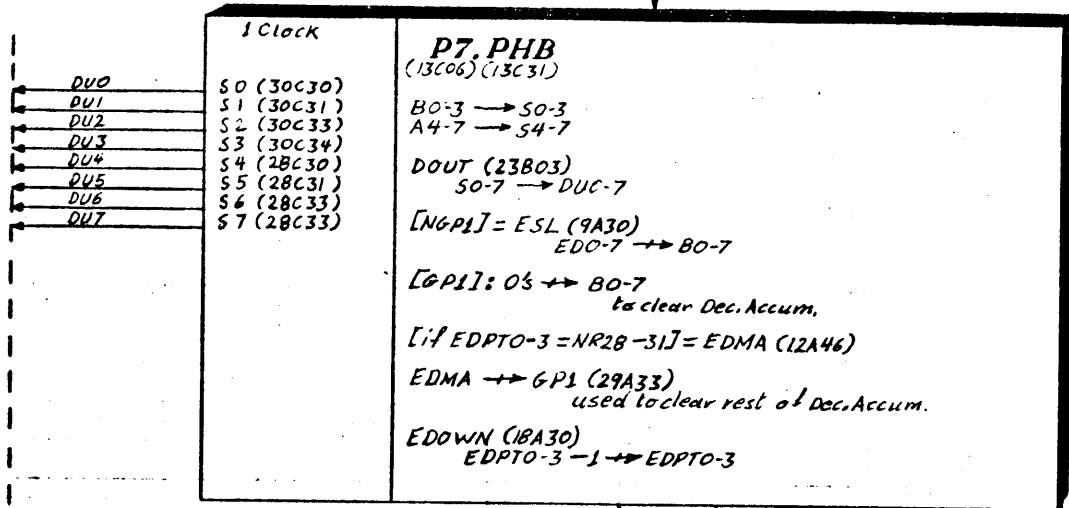
[if EDPT0-3 = NR28-31] = EDMA (12A46)

EDMA → GP1 (29A33)
 used to clear rest of Dec. Accum.

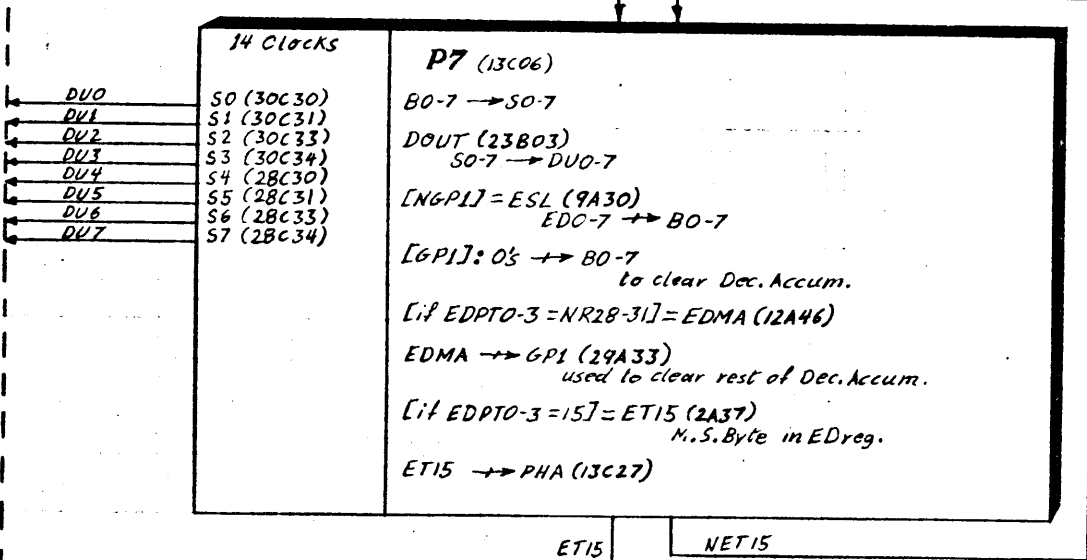
DECIMAL LOAD CONTINUED



1st
least signif.
data byte
to R15

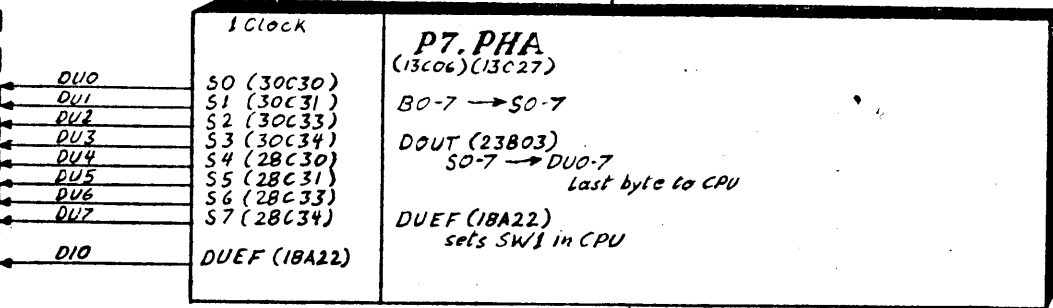


Data or 0's
to
CPU
fast memory.



NET15

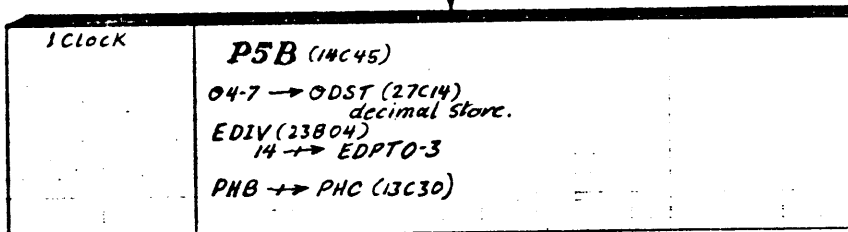
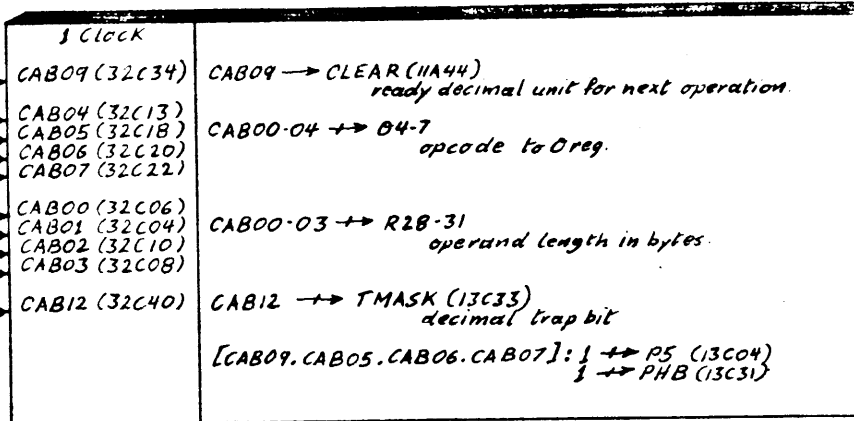
Last
data byte
to
CPU
fast memory
DUEND
(sets SW1)



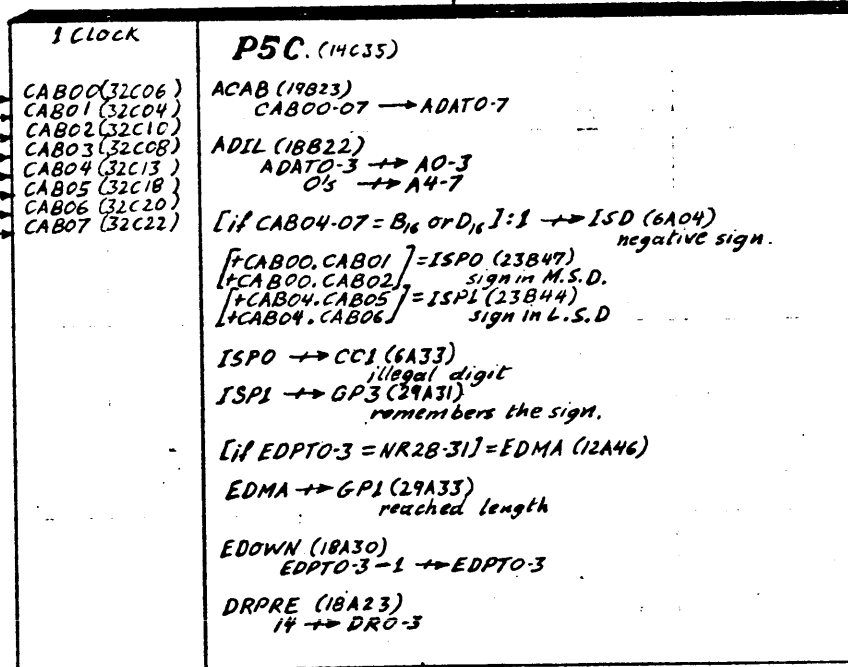
DECIMAL STORE (7F)

CPU INTERFACE

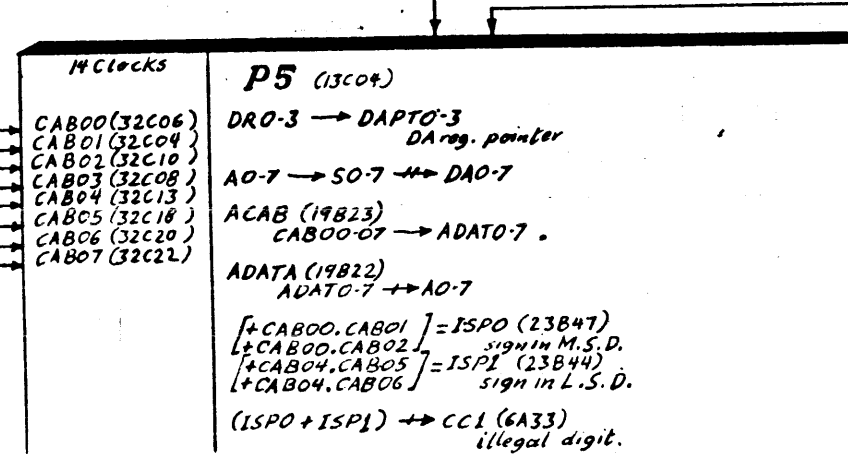
DUSTART
 04-7
 R28-31
 DM
 decimal trap.



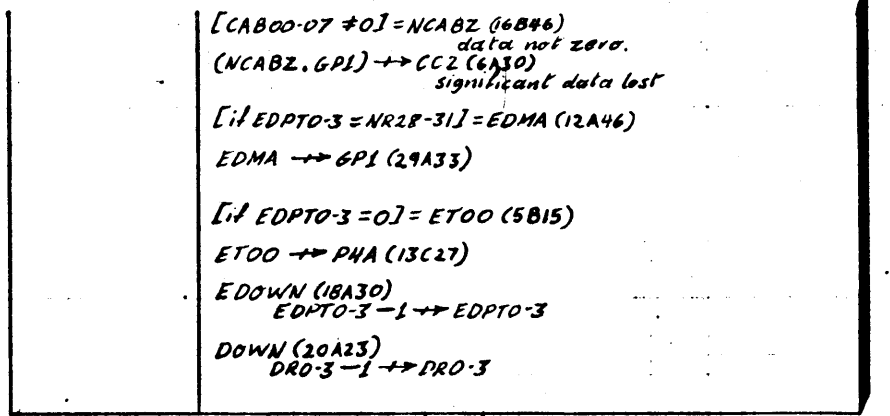
1st
least signif.
data byte
(from R15)



Data bytes
from
CPU
fast Memory

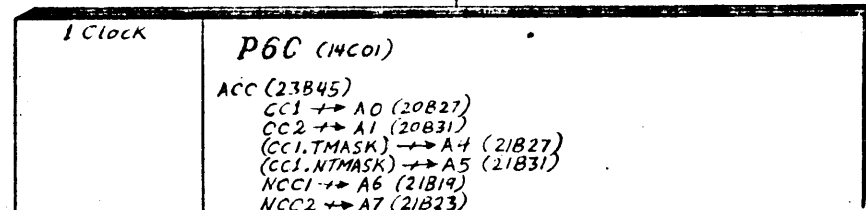
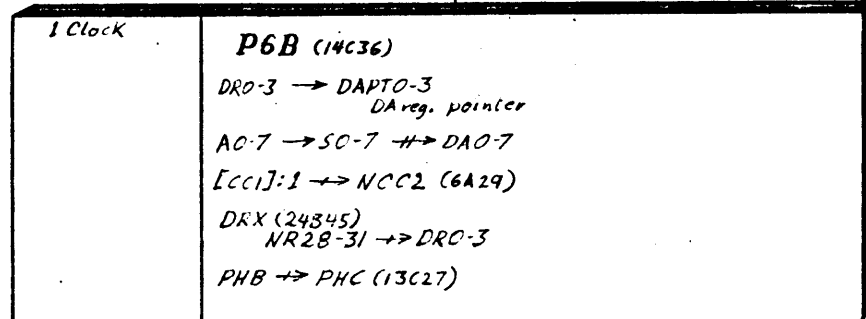
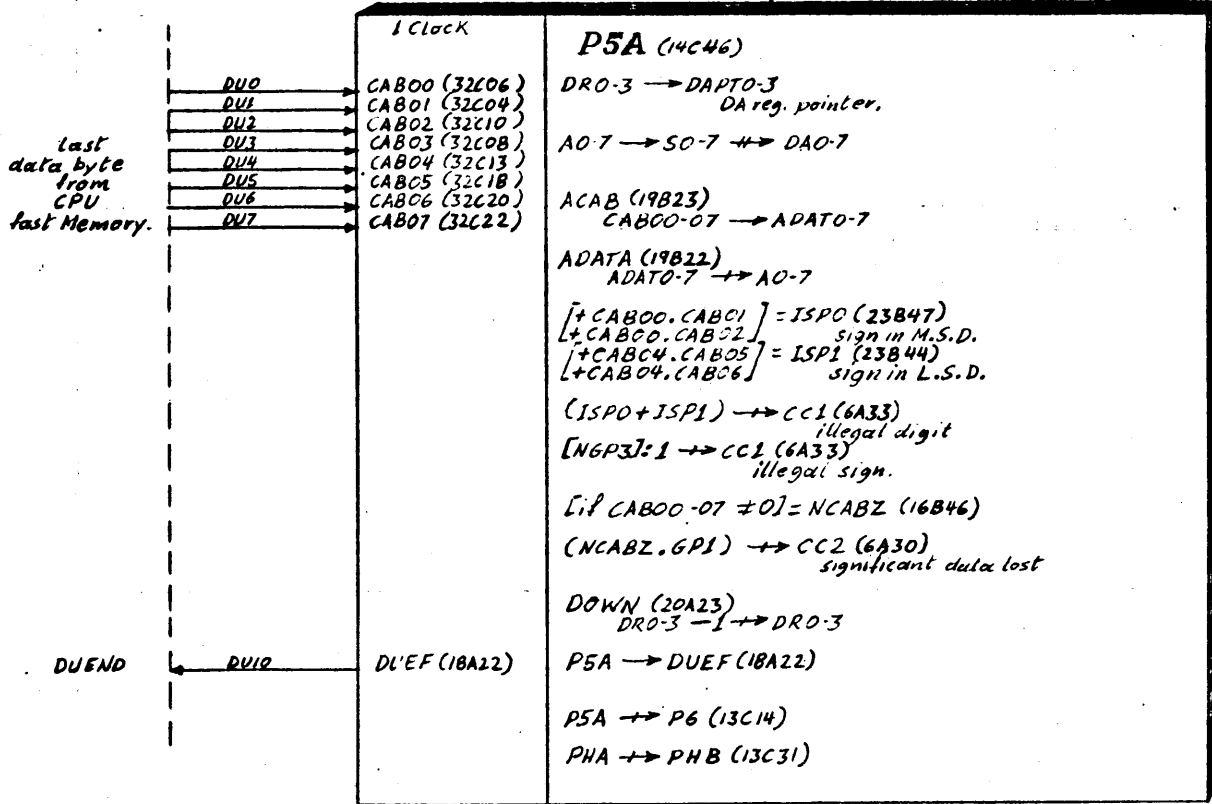


DECIMAL STORE CONTINUED

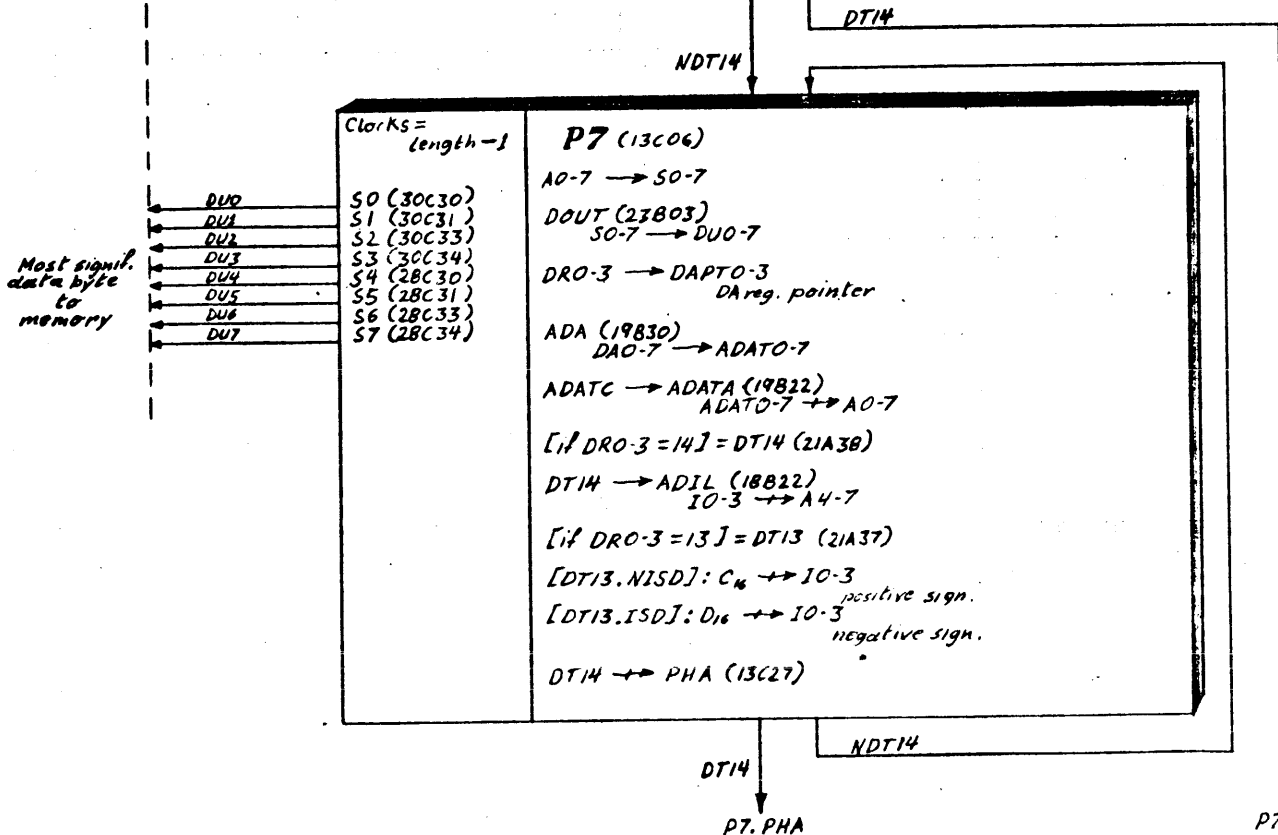
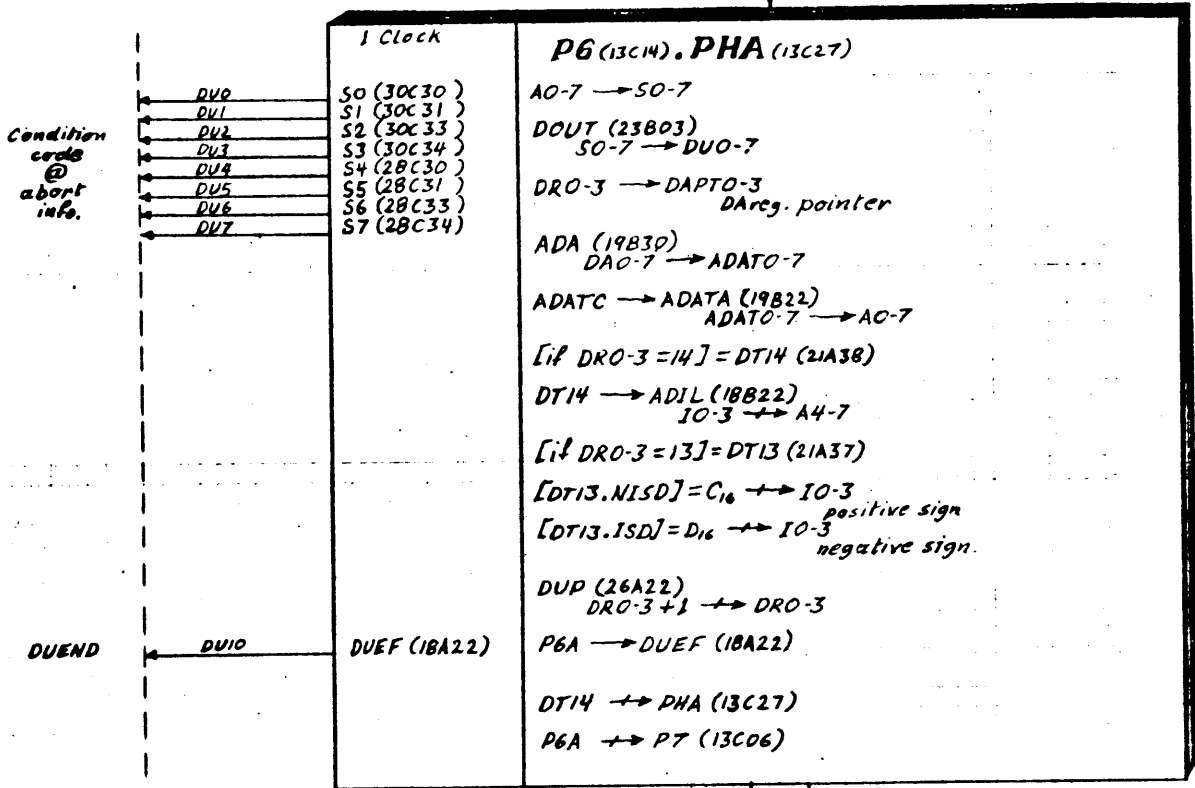
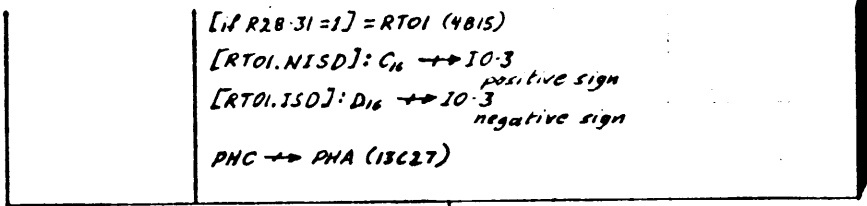


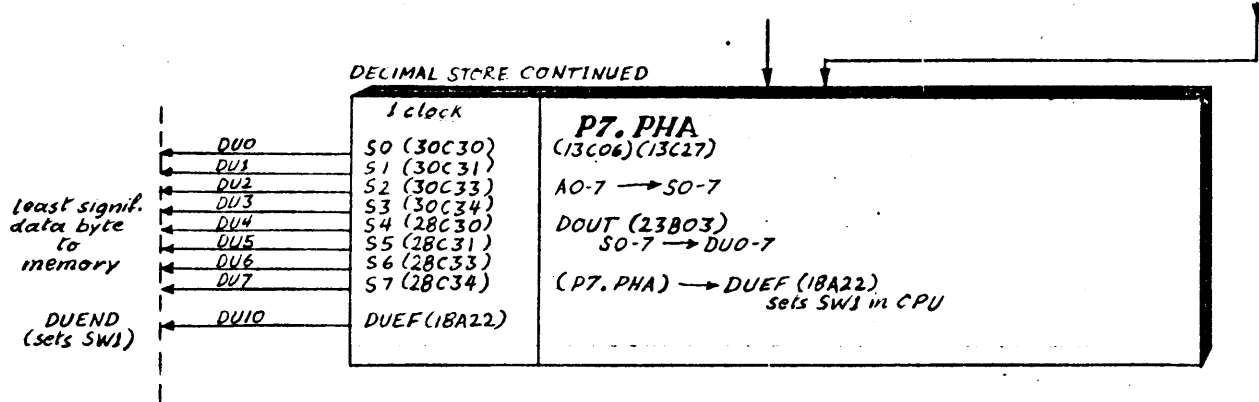
ETOO

NETOO

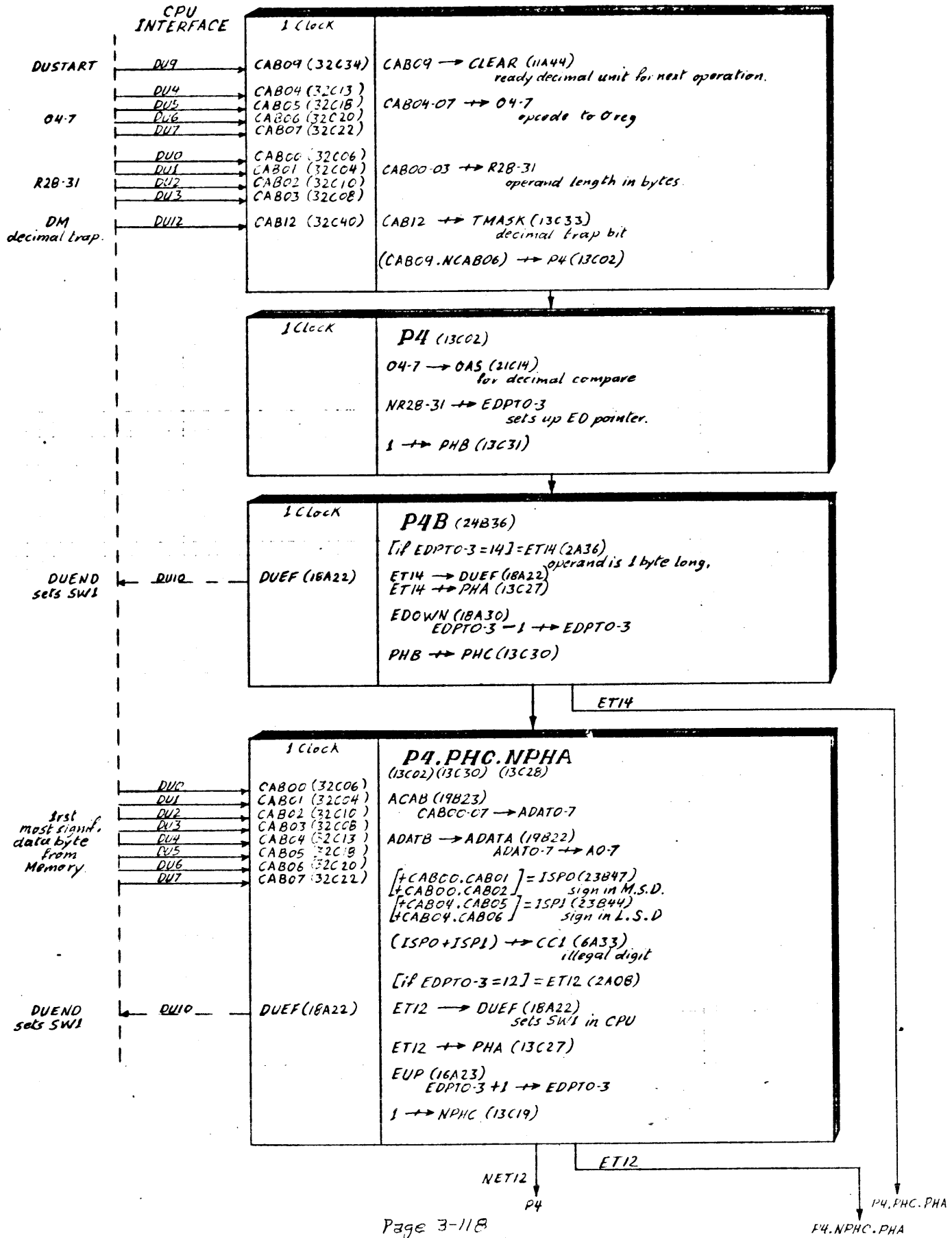


DECIMAL STORE CONTINUED

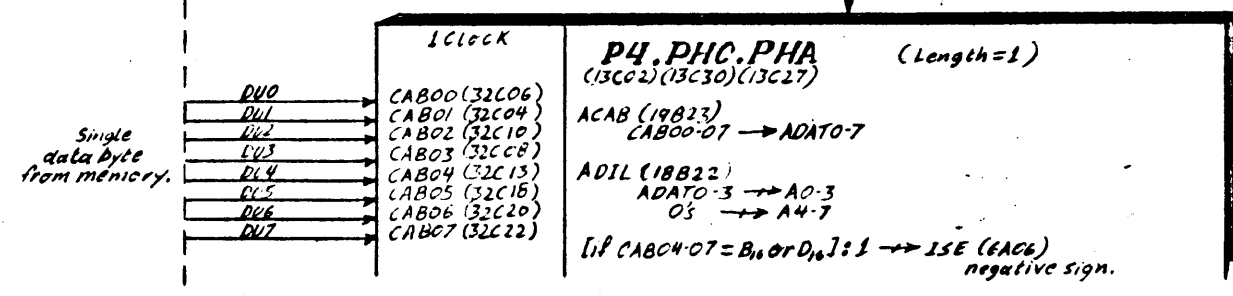
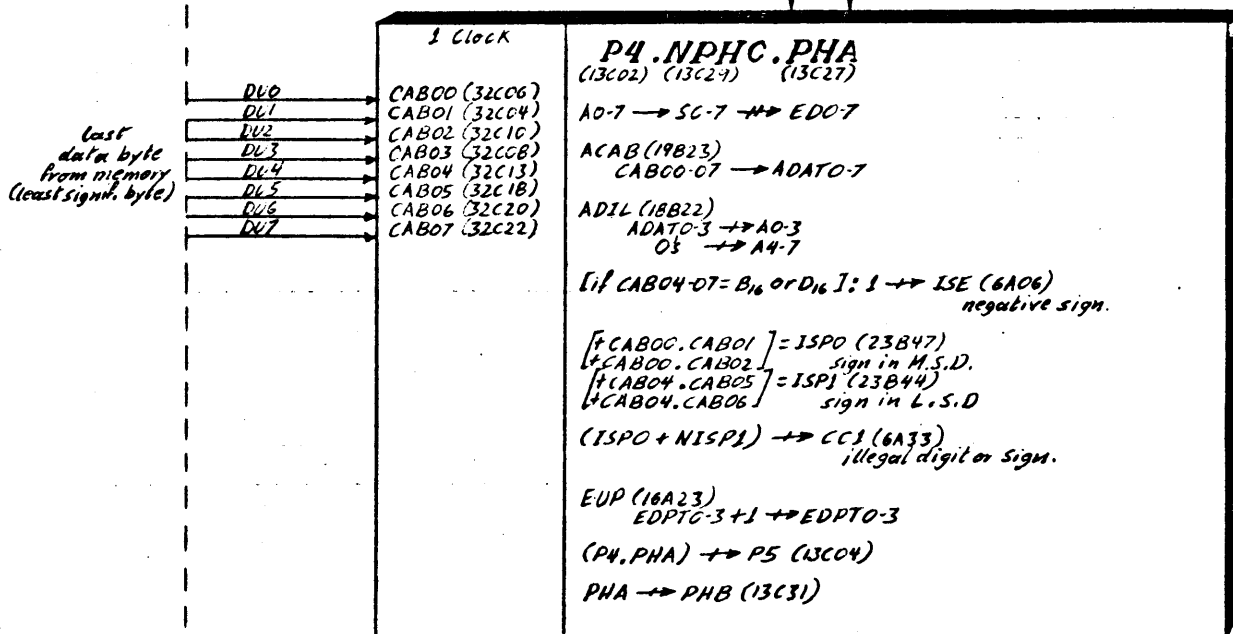
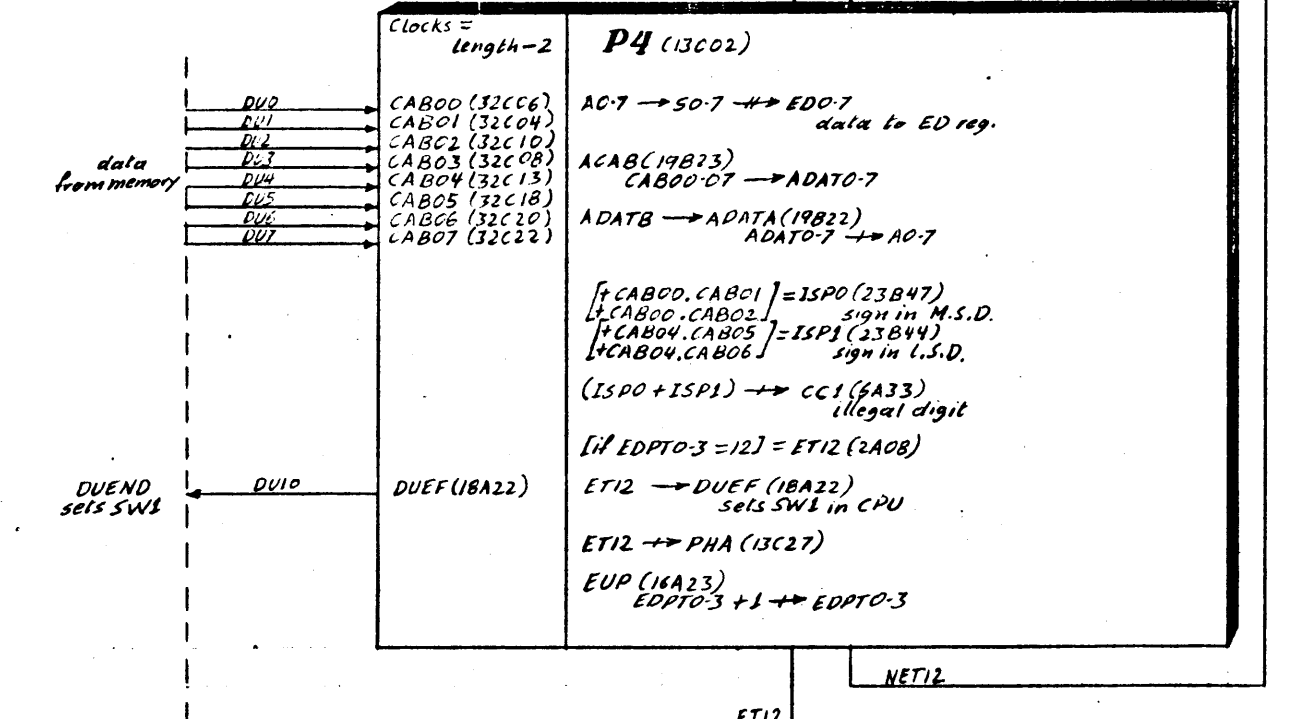




DECIMAL COMPARE (70)



DECIMAL COMPARE CONTINUED



DECIMAL COMPARE CONTINUED

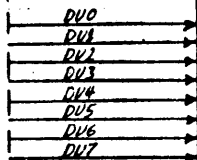
$\left[\begin{matrix} + \text{CAB00.CAB01} \\ + \text{CAB00.CAB02} \end{matrix} \right] = \text{ISPO (23B47)}$ *sign in M.S.D.*
 $\left[\begin{matrix} + \text{CAB04.CAB05} \\ + \text{CAB04.CAB06} \end{matrix} \right] = \text{ISPI (23B44)}$ *sign in L.S.D.*
 (ISPO + NISPI) \rightarrow CC1 (6A33) *illegal digit or sign.*
 EUP (16A23)
 EDPT0-3 + 1 \rightarrow EDPT0-3
 (P4.PHA) \rightarrow P5 (13C04)
 PHA \rightarrow PHB (13C31)

1 Clock

P5B (14C45)

A0-7 \rightarrow S0-7 \rightarrow ED0-7 *last data byte to ED reg. (loc. M)*
 DIV (23B04)
 14 \rightarrow EDPT0-3
 PHB \rightarrow PNC (13C30)

1st
least signif.
data byte
from R15



1 Clock

P5C (14C35)

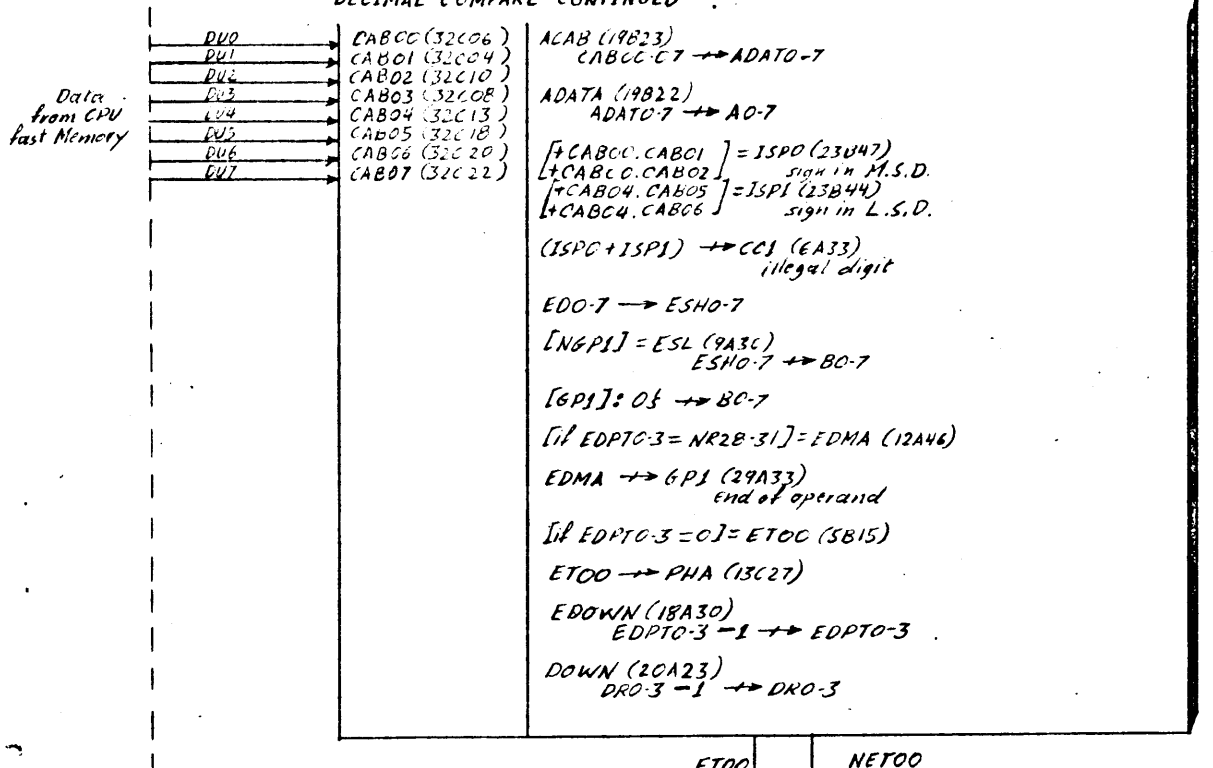
ACAB (19B23)
 CAB00-07 \rightarrow ADATA-7
 ADIL (18B22)
 ADAT0-3 \rightarrow A0-3
 OS \rightarrow A4-7
 [if CAB04-07 = B₁₆ or D₁₆]: 1 \rightarrow ISD (6A04) *negative sign.*
 $\left[\begin{matrix} + \text{CAB00.CAB01} \\ + \text{CAB00.CAB02} \end{matrix} \right] = \text{ISPO (23B47)}$ *sign in M.S.D.*
 $\left[\begin{matrix} + \text{CAB04.CAB05} \\ + \text{CAB04.CAB06} \end{matrix} \right] = \text{ISPI (23B44)}$ *sign in L.S.D.*
 ISPO \rightarrow CC1 (6A33) *illegal digit*
 ISPI \rightarrow GP3 (29A31) *remembers the sign.*
 ED0-7 \rightarrow ESH0-7
 ESL (9A30)
 ESH0-7 \rightarrow B0-7
 [if EDPT0-3 = NR28-31] = EDMA (12A46)
 EDMA \rightarrow GP1 (29A33) *end of operand*
 EDOWN (18A30)
 EDPT0-3 - 1 \rightarrow EDPT0-3
 DRPRE (18A23)
 14 \rightarrow DR0-3 *to address DA reg.*

14 Clocks

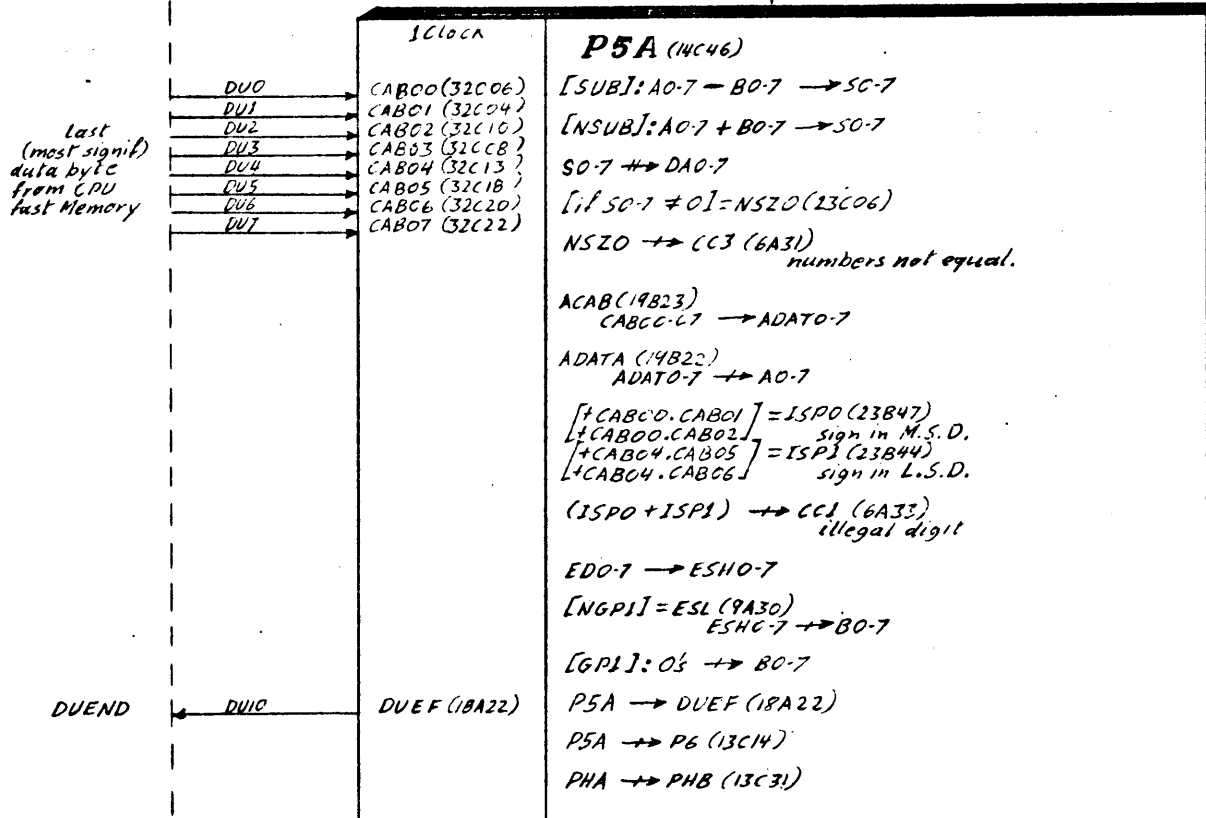
P5 (13C04)

[if ISE \neq ISD] = NSUB (17C23)
 A0-7 + B0-7 \rightarrow S0-7
 [if ISE = ISD] = SUB (23C45)
 A0-7 - B0-7 \rightarrow S0-7
 SUB \rightarrow GP5 (6A02) *remembers subtract*
 S0-7 \rightarrow DA0-7 *result to DA reg.*
 [if S \neq 0] = NSZ0 (23C06)
 NSZ0 \rightarrow CC3 (6A31) *numbers not equal.*

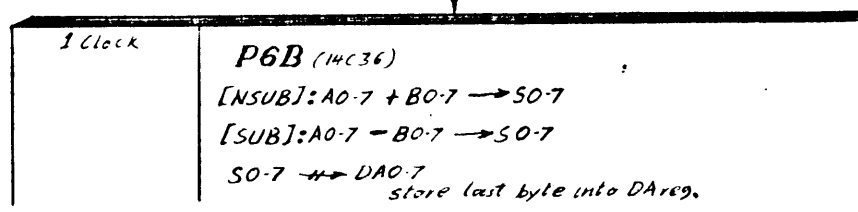
DECIMAL COMPARE CONTINUED



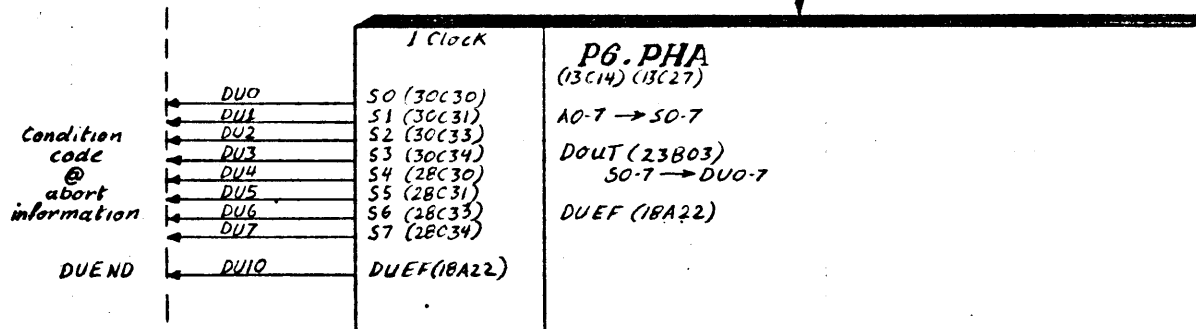
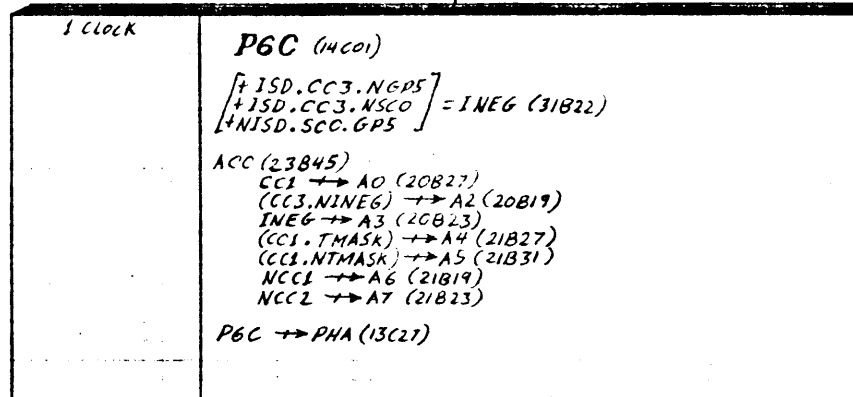
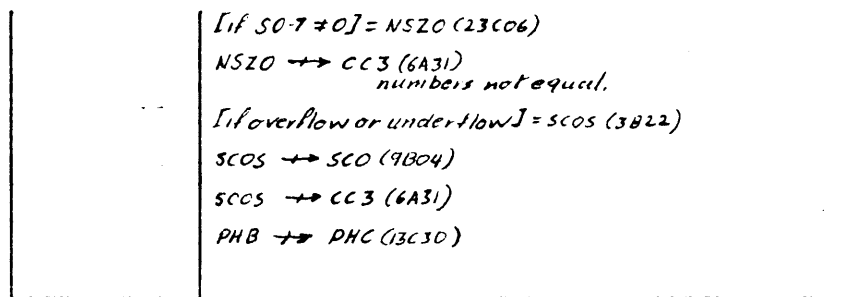
ETOO NETOO



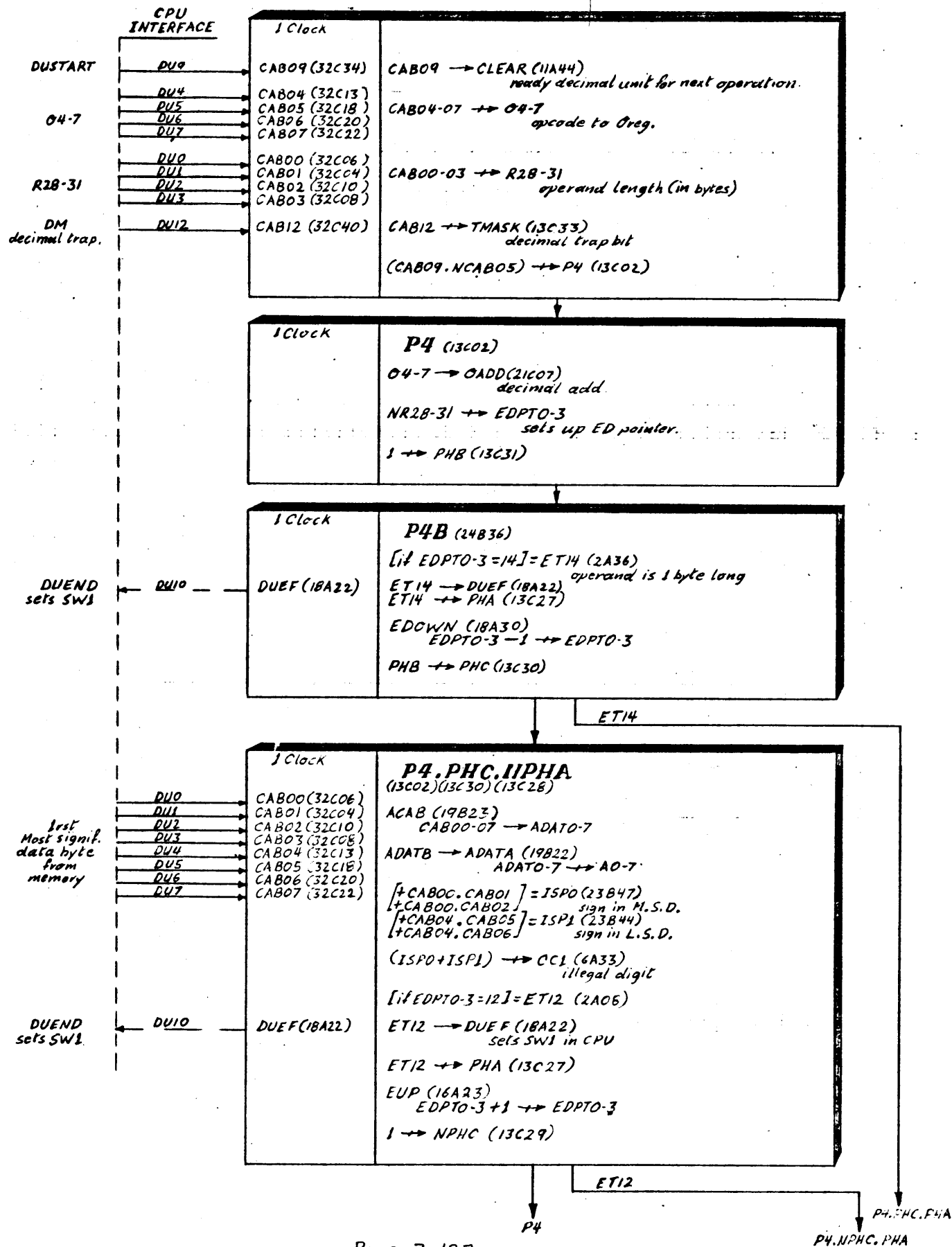
DUEND ← DUIC



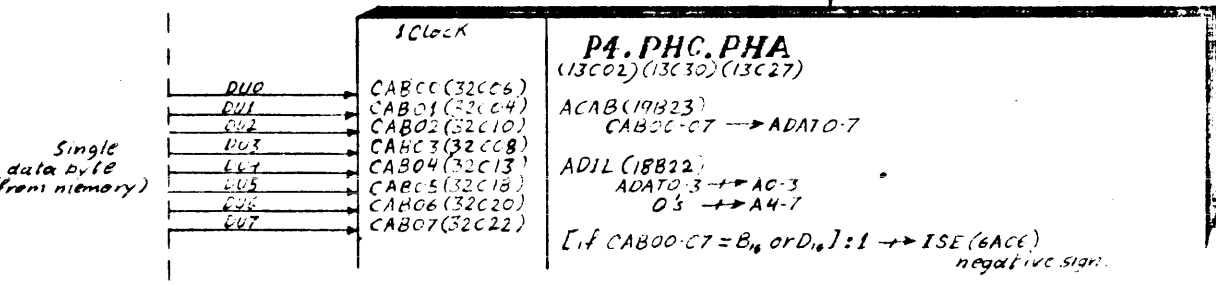
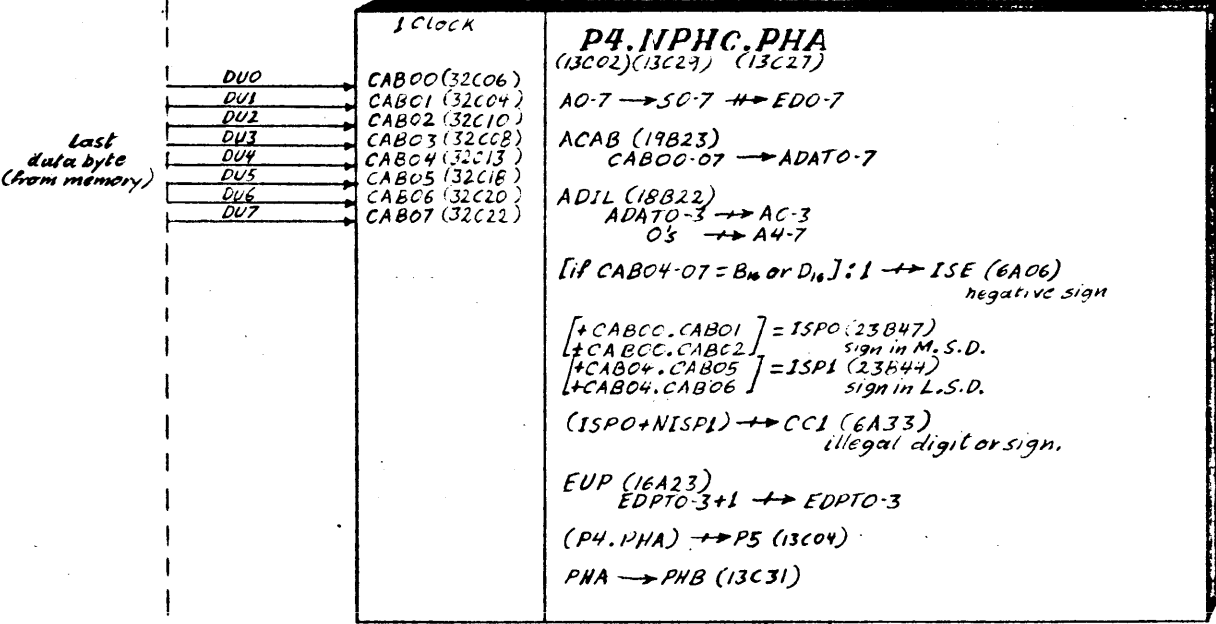
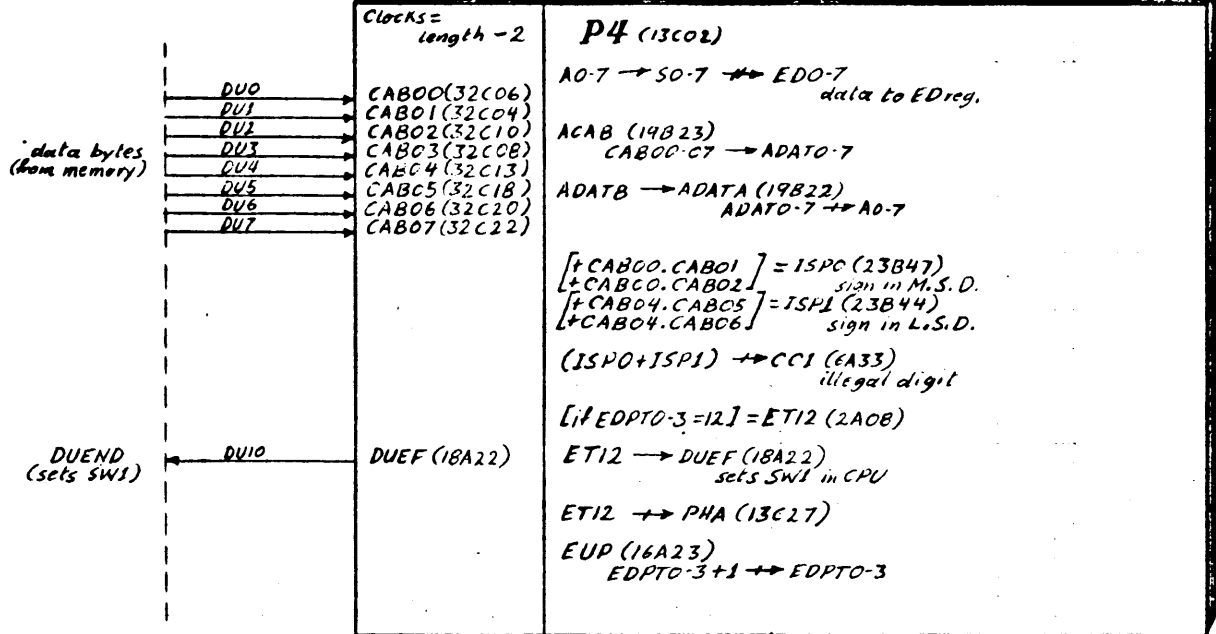
DECIMAL COMPARE CONTINUED



DECIMAL ADD (79)



DECIMAL ADD CONTINUED



DECIMAL ADD CONTINUED

$[+CAB00.CAB01] = ISPO (23B47)$
 $[+CAB00.CAB02] = \text{sign in M.S.D.}$
 $[+CAB04.CAB05] = ISPI (23B44)$
 $[+CAB04.CAB06] = \text{sign in L.S.D.}$
 $(ISPO + NISPI) \rightarrow CCL (6A33)$
illegal sign or digit
 $EUP (16A23)$
 $EDPTO-3 + 1 \rightarrow EDPTO-3$
 $(P4.PHA) \rightarrow P5 (13C04)$
 $PHA \rightarrow PHB (13C31)$

1 Clock

P5B (14C45)

$A0-7 \rightarrow S0-7 \rightarrow EDO-7$
last data byte to ED reg. (loc. 14)
 $EDIV (23B04)$
 $14 \rightarrow EDPTO-3$
to address ED reg.
 $PHB \rightarrow PHC (13C30)$

1st
least signif
data byte
from R15

1 Clock

P5C (14C35)

D00	CAB00 (32C06)
D01	CAB01 (32C04)
D02	CAB02 (32C10)
D03	CAB03 (32C0E)
D04	CAB04 (32C13)
D05	CAB05 (32C18)
D06	CAB06 (32C20)
D07	CAB07 (32C22)

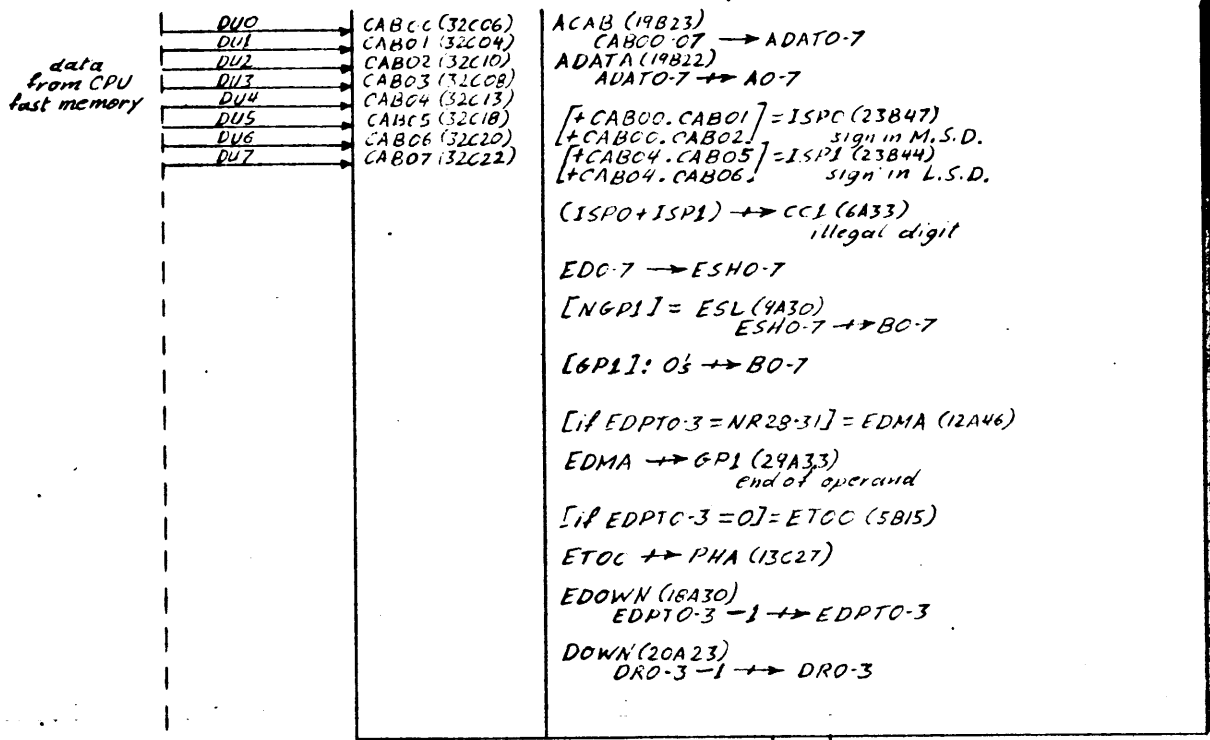
$ACAB (19B23)$
 $CABCC-07 \rightarrow ADATO-7$
 $ADIL (18B22)$
 $ADATO-3 \rightarrow A0-3$
 $05 \rightarrow A4-7$
 $[if CAB04-C7 = B_{16} \text{ or } D_{16}]: 1 \rightarrow ISD (6A04)$
negative sign
 $[+CAB00.CAB01] = ISPO (23B47)$
 $[+CAB00.CAB02] = \text{sign in M.S.D.}$
 $[+CAB04.CAB05] = ISPI (23B44)$
 $[+CAB04.CAB06] = \text{sign in L.S.D.}$
 $ISPO \rightarrow CCL (6A33)$
illegal digit
 $ISPI \rightarrow GP3 (29A31)$
remembers the sign.
 $EDO-7 \rightarrow ESHO-7$
 $ESL (9A30)$
 $ESHO-7 \rightarrow B0-7$
 $[if EDPTO-3 = NR28-31] = EDMA (12A46)$
 $EDMA \rightarrow GP8 (29A33)$
end of operand.
 $EDOWN (18A30)$
 $EDPTO-3 - 1 \rightarrow EDPTO-3$
 $DRPRE (18A23)$
 $14 \rightarrow DRO-3$
to address DA reg.

14 Clocks

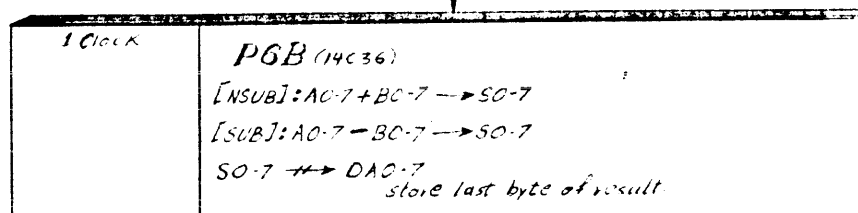
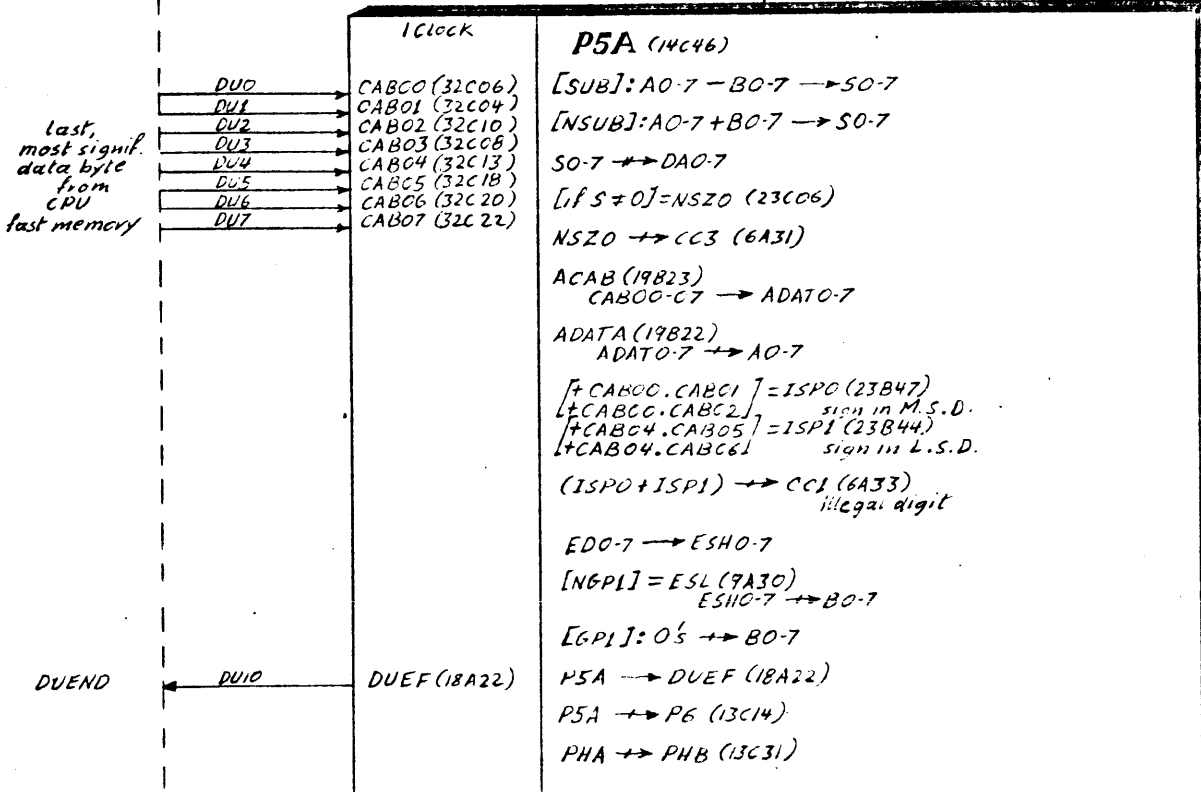
P5 (13C04)

$[if ISE = ISD] = NSUB (17C23)$
 $A0-7 + B0-7 \rightarrow S0-7$
 $[if ISE \neq ISD] = SUB (23C45)$
 $A0-7 - B0-7 \rightarrow S0-7$
 $SUB \rightarrow GP5 (6A02)$
remembers subtract.
 $S0-7 \rightarrow DAC-7$
result to DA reg.
 $[if S \neq 0] = NSZO (23C06)$
 $NSZO \rightarrow CC3 (6A31)$
result not zero.

DECIMAL ADD CONTINUED



ETOO NETOO



DECIMAL ADD CONTINUED

[if 50-7 ≠ 0] = NSZO (23C06)
 NSZO → CC3 (6A31)
 result not zero
 [if overflow or underflow] = SCOS (3B22)
 SCOS → SCO (9B04)
 remembers overflow or underflow
 SCOS → GP2 (29A30)
 for complementing result if SUB
 (NSUB.SCOS) → CC2 (6A30)
 overflow.
 PHB → PHC (13C30)

1 Clock
P6C (14C01)
 ACC (23B45)
 CC1 → A0 (20B27)
 CC2 → A1 (20B31)
 (CC3.NINEG) → A2 (20B19)
 INEG → A3 (20B23)
 (CC1.TMASK) → A4 (21B27)
 (CC1.NTMASK) → A5 (21B31)
 NCC1 → A6 (21B19)
 NCC2 → A7 (21B23)
 [+ISE.ISD.CC3]
 [+NSCO.ISD.CC3]
 [+GP5.SCO.NISD] = INEG (31B22)
 [NINEG]: C₁₆ → IO-3
 [INEG]: D₁₆ → IO-3
 DRPRE (18A23)
 14 → DRO-3
 EDIV (23B04)
 14 → EDPTO-3
 P6C → PHA (13C27)

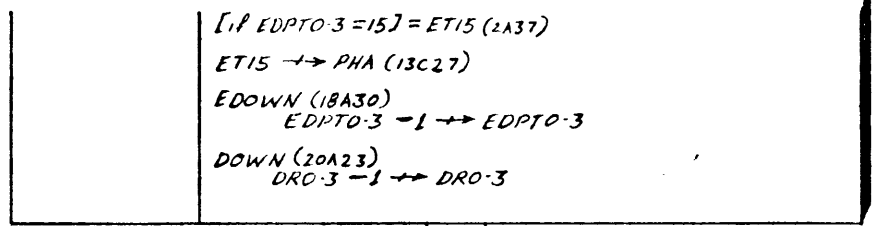
1 Clock
P6. PHA (13C14) (13C27)
 AO-7 → SO-7
 DOUT (23B03)
 SO-7 → DUO-7
 DUEF (18A22)
 sets SW1 in CPU
 ADIL (18B22)
 IO-3 → A4-7
 sign.
 EDA (5B02)
 DA0-7 → BO-7
 DOWN (20A23)
 DRO-3 - 1 → DRO-3
 EDOWN (18A30)
 EDPTO-3 - 1 → EDPTO-3
 P6A → P7 (13C06)

Condition code @ abort info.
 DU0 → 50 (30C30)
 DU1 → 51 (30C31)
 DU2 → 52 (30C33)
 DU3 → 53 (30C34)
 DU4 → 54 (28C30)
 DU5 → 55 (28C31)
 DU6 → 56 (28C33)
 DU7 → 57 (29C34)

14 Clocks
P7 (13C06)
 [GP2] = SUB (2836)
 A0-7 - B0-7 → SO-7
 [NGP2] = NSUB (17C23)
 A0-7 + B0-7 → SO-7
 DOUT (23B03)
 SO-7 → DUO-7
 EDA (5B02)
 DA0-3 → BO-7
 O's → AO-7

Result back to CPU starting with least signif. byte.
 DU0 → 50 (30C30)
 DU1 → 51 (30C31)
 DU2 → 52 (30C33)
 DU3 → 53 (30C34)
 DU4 → 54 (28C30)
 DU5 → 55 (28C31)
 DU6 → 56 (28C33)
 DU7 → 57 (29C34)

DECIMAL ADD CONTINUED

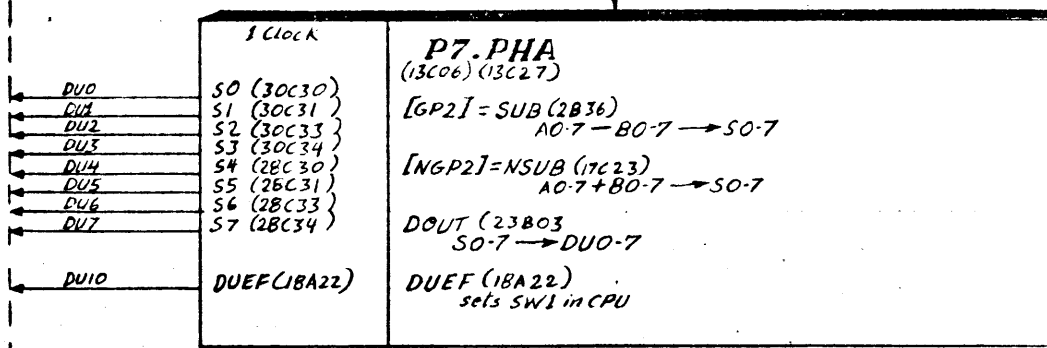


ET15

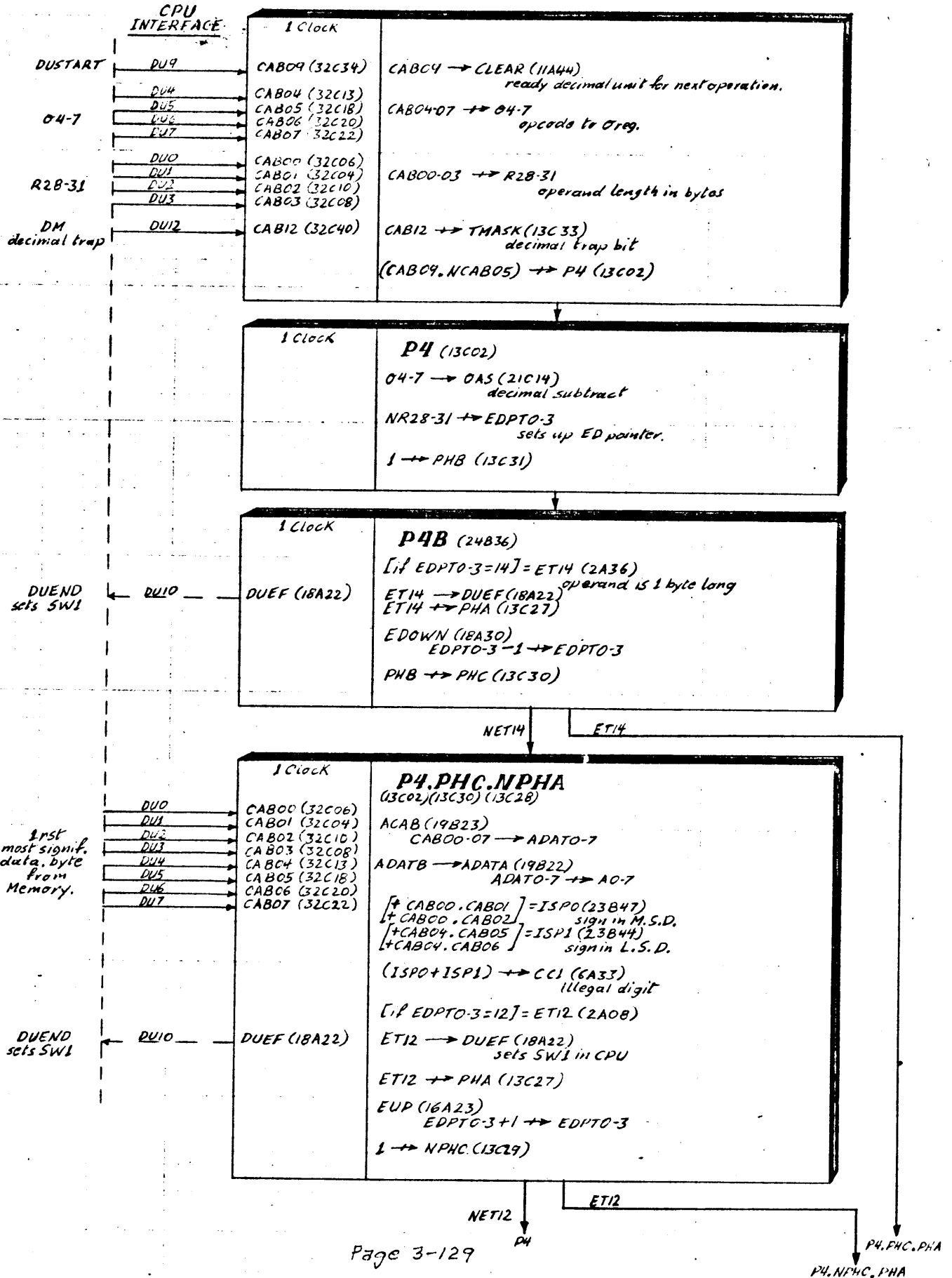
NET15

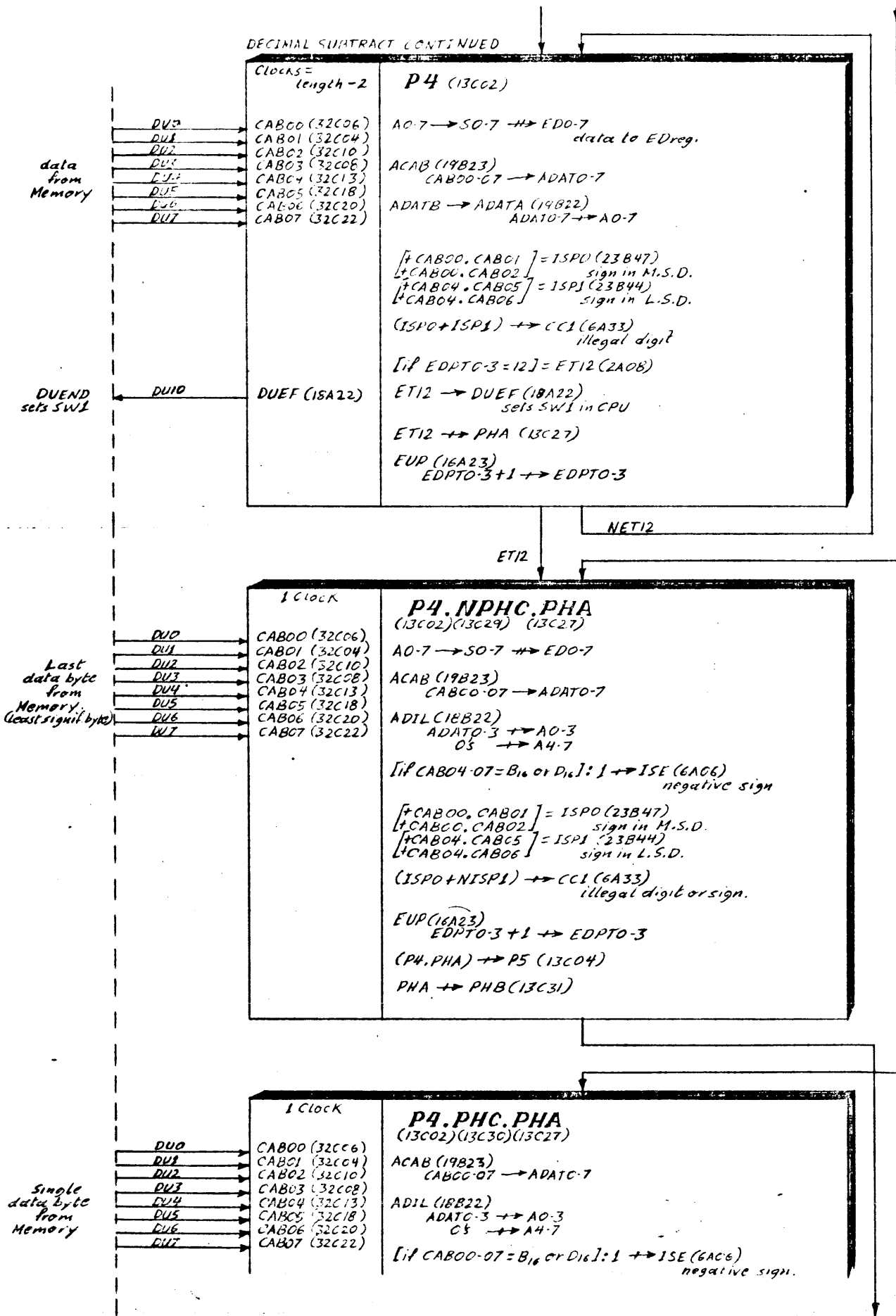
last
most signif
data byte
to
CPU
fast memory

DUEND
sets SW1



DECIMAL SUBTRACT (78)





DECIMAL SUBTRACT CONTINUED

$\{ \begin{matrix} +CAB00.CAB01 \\ +CAB00.CAB02 \end{matrix} \} = ISPO (23B47)$ sign in M.S.D.
 $\{ \begin{matrix} +CAB04.CAB05 \\ +CAB04.CAB06 \end{matrix} \} = ISPL (23B44)$ sign in L.S.D.
 $(ISPO + ISPL) \rightarrow CC1 (6A33)$ illegal digit or sign.
 EUP (16A23)
 $EDPT0-3 + 1 \rightarrow EDPT0-3$
 $(PH, PHA) \rightarrow P5 (13C04)$
 $PHA \rightarrow PHB (13C31)$

1 Clock

P5B (14C45)

$A0-7 \rightarrow S0-7 \rightarrow ED0-7$ last data byte to ED reg. (Loc. 14)
 EDIV (23B04)
 $14 \rightarrow EDPT0-3$
 $PNB \rightarrow PHC (13C30)$

1 Clock

P5C (14C35)

$DU0 \rightarrow CAB00 (32C06)$
 $DU1 \rightarrow CAB01 (32C04)$
 $DU2 \rightarrow CAB02 (32C10)$
 $DU3 \rightarrow CAB03 (32C08)$
 $DU4 \rightarrow CAB04 (32C13)$
 $DU5 \rightarrow CAB05 (32C18)$
 $DU6 \rightarrow CAB06 (32C20)$
 $DU7 \rightarrow CAB07 (32C22)$

1st least signif. data byte from R15

ACAB (19B23)
 $CAB00-07 \rightarrow ADAT0-7$
 ADIL (18B22)
 $ADAT0-3 \rightarrow A0-3$
 $05 \rightarrow A4-7$
 $[if CAB04-07 = B16 or D16]: 1 \rightarrow ISD (6A04)$ negative sign.
 $\{ \begin{matrix} +CAB00.CAB01 \\ +CAB00.CAB02 \end{matrix} \} = ISPO (23B47)$ sign in M.S.D.
 $\{ \begin{matrix} +CAB04.CAB05 \\ +CAB04.CAB06 \end{matrix} \} = ISPL (23B44)$ sign in L.S.D.
 $ISPO \rightarrow CC1 (6A33)$ illegal digit
 $ISPL \rightarrow GP3 (29A31)$ remembers the sign.
 $ED0-7 \rightarrow ESH0-7$
 ESL (9A30)
 $ESH0-7 \rightarrow B0-7$
 $[if EDPT0-3 = NR28-31] = EDMA (12A46)$
 $EDMA \rightarrow GP1 (29A33)$ end of operand
 $EDOWN (18A30)$
 $EDPT0-3 - 1 \rightarrow EDPT0-3$
 $DRPRE (18A23)$
 $14 \rightarrow DRO-3$ to address DA reg

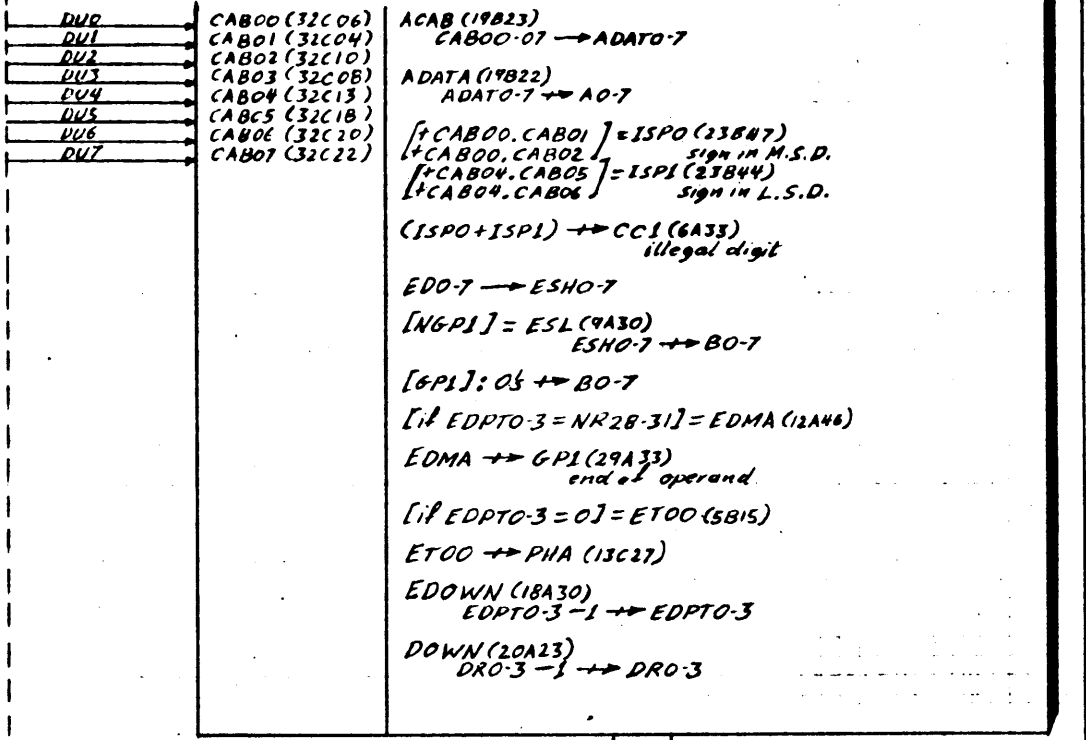
14 Clocks

P5 (13C04)

$[if ISE \neq ISD] = NSUB (17C23)$
 $A0-7 + B0-7 \rightarrow S0-7$
 $[if ISE = ISD] = SUB (23C45)$
 $A0-7 - B0-7 \rightarrow S0-7$
 $SUB \rightarrow GP5 (6A02)$ remembers subtract.
 $S0-7 \rightarrow DAO-7$ result to DA reg.
 $[if S \neq 0] = NSZO (23C06)$
 $NSZO \rightarrow CC3 (6A31)$ result not zero.

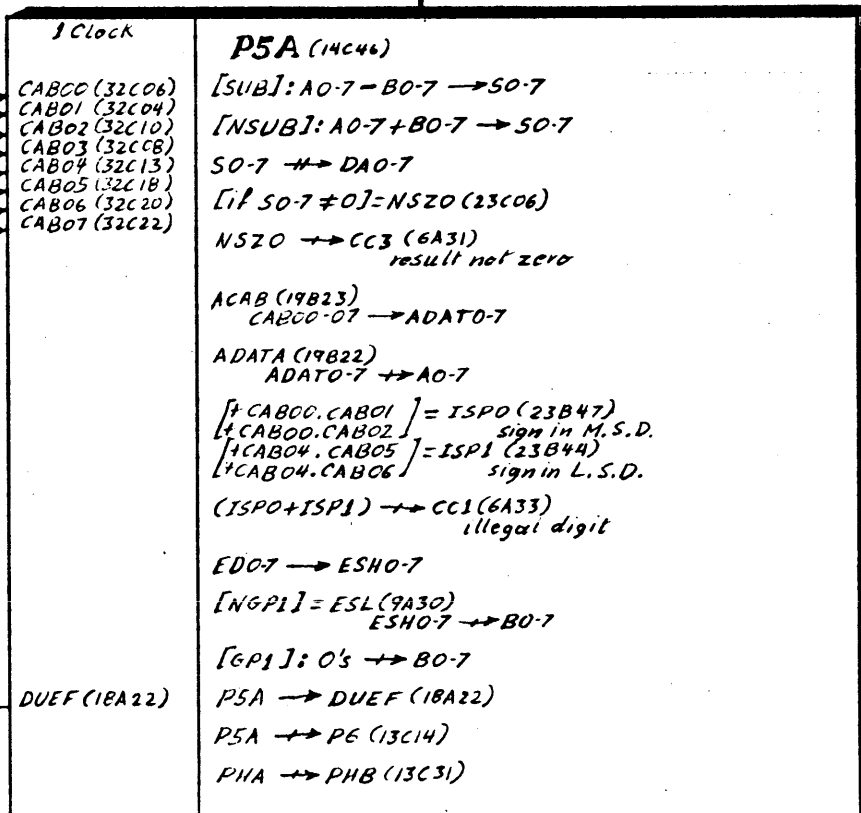
DECIMAL SUBTRACT CONTINUED

data from CPU last memory

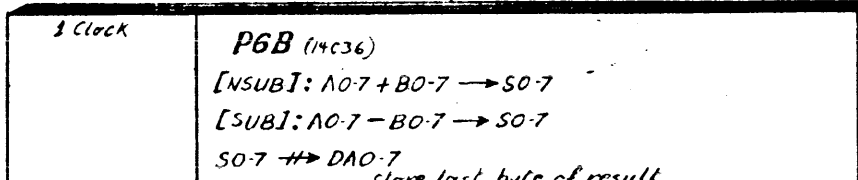


ETOO NETOO

last (most signif.) data byte from CPU last memory



DUEND



DEDIMAL SUBTRACT CONTINUED

[if 50-7 ≠ 0] = NSZO (23C06)
 NSZO → CC3 (6A31)
 result not zero

[if overflow or underflow] = SCOS (3B22)
 SCOS → SCO (9B04)
 remembers overflow or underflow

SCOS → GP2 (29A30)
 for complementing result if SUB

(NSUB.SCOS) → CC2 (6A39)
 overflow

PHB → PHC (13C30)

1 Clock

P6C (14C01)

$$\begin{bmatrix} +ISD.CC3.NGPS \\ +ISD.CC3.NSCO \\ +NISD.SCO.GP5 \end{bmatrix} = INEG (31B22)$$

ACC (23B45)
 CC1 → A0 (20B27)
 CC2 → A1 (20B31)
 (CC3.NINEG) → A2 (20B19)
 INEG → A3 (20B23)
 (CC1.TMASK) → A4 (21B27)
 (CC1.NTMASK) → A5 (21B31)
 NCC1 → A6 (21B19)
 NCC2 → A7 (21B23)

[NINEG]: C₁₆ → IO-3
 [INEG]: D₁₆ → IO-3

DRPRE (18A23)
 14 → DRO-3

EDIV (23B04)
 14 → EDPTO-3

P6C → PHA (13C27)

1 Clock

P6 (13C14) . PHA (13C27)

D00	SC (30C30)	A0-7 → S0-7
D01	S1 (30C31)	
D02	S2 (30C33)	DOUT (23B03)
D03	S3 (30C34)	S0-7 → DUO-7
D04	S4 (28C30)	DUEF (18A22)
D05	S5 (28C31)	sets SW1 in CPU
D06	S6 (28C33)	ADIL (18B22)
D07	S7 (28C34)	IO-3 → A4-7
		05 → A0-3
		sign to A reg.
		EDA (5B02)
		DA0-7 → B0-7
		DOWN (20A23)
		DRO-3 - 1 → DRO-3
		EDOWN (18A30)
		EDPTO-3 - 1 → EDPTO-3
		P6A → P7 (13C06)

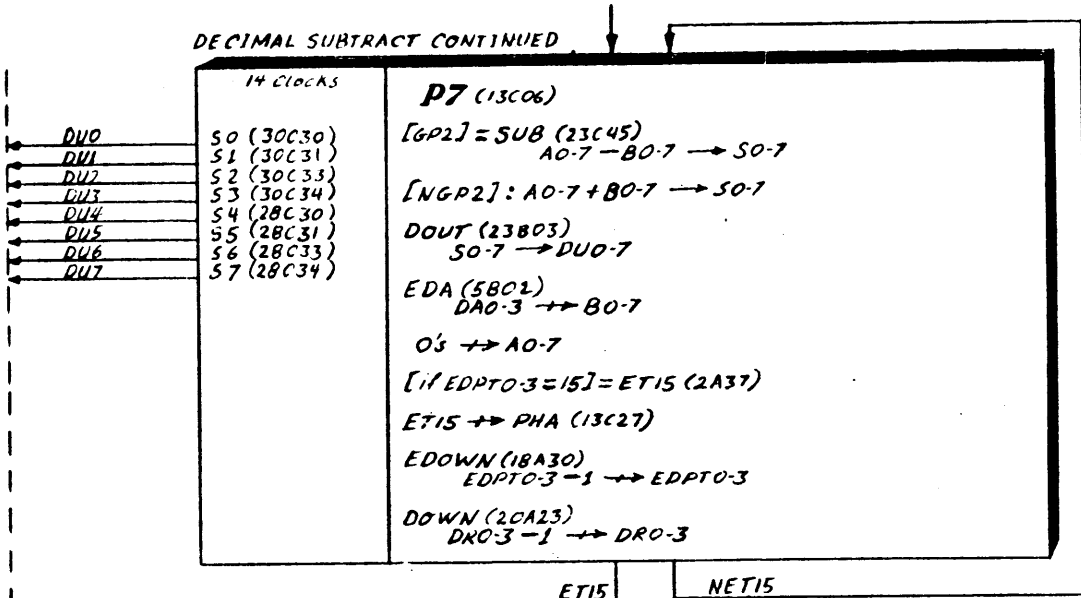
Condition code @ abort information

D00
D01
D02
D03
D04
D05
D06
D07

P7

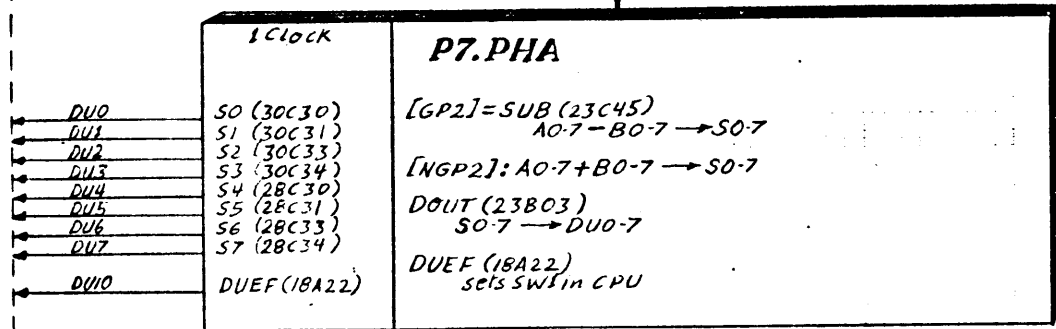
DECIMAL SUBTRACT CONTINUED

Result
back to CPU
starting with
least signif.
byte.

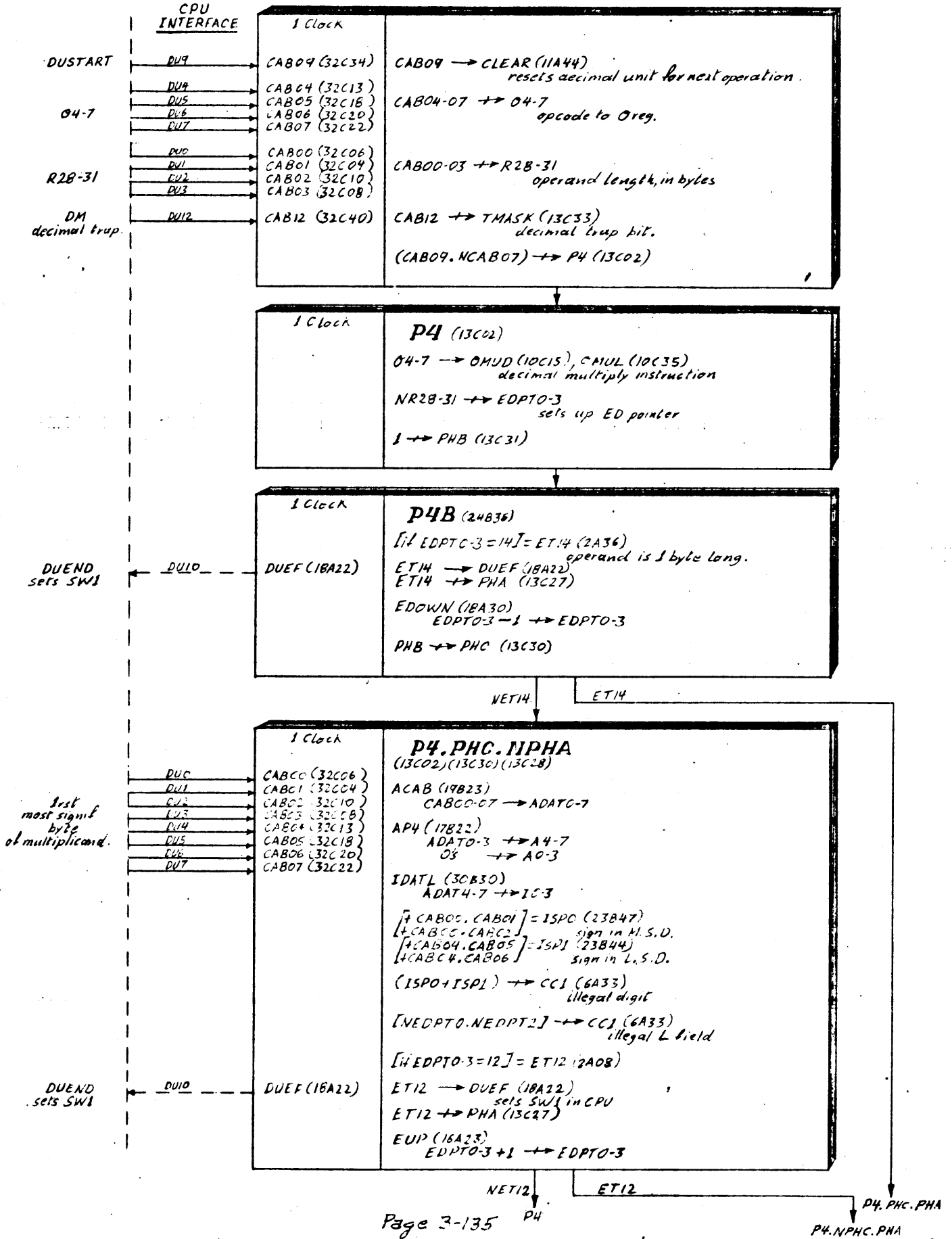


fast
most signif.
byte of result
to CPU
fast memory.

DUEND
sets SW1

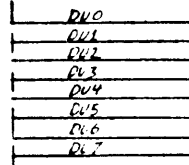


DECIMAL MULTIPLY (7B)



DECIMAL MULTIPLY CONTINUED

Multiplicand



P4 (13C02)

A0-7 → S0-7 → EDC-7
data to EDreg.

[if S0-7 ≠ 0] = NSZO (23C06)
data not zero
 NSZO → CC4 (6A27)

ACAB (19B23)
 CAB00-07 → ADAT0-7

IDATL (30B30)
 ADAT4-7 → IO-3

AP4 (17B22)
 IO-3 → AO-3
 ADAT0-3 → AH-7

[+ CAB00.CAB01] = ISPO (23B47)
sign in M.S.D.
 [+ CAB00.CAB02] = ISPI (23B44)
sign in L.S.D.
 [+ CAB04.CAB05]
 [+ CAB04.CAB06]

(ISPO+ISPI) → CC1 (6A33)
illegal digit

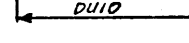
[if EDPT0-3 = 12] = ET12 (2A08)
sets SWs in CPU
 ET12 → PHA (13C27)

ET12 → DUEF (18A22)

(NEDPT0.NEDPT2) → CC1 (6A33)
illegal L field.

EUP (16A23)
 EDPT0-3+1 → EDPT0-3

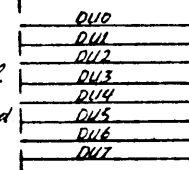
DUEND sets SW1



NET12

ET12

least signif. byte of multiplicand



P4.NPHC.PHA (13C02)(13C29)(13C27)

A0-7 → S0-7 → EDC-7

[if S0-7 ≠ 0] = NSZO (23C06)
data not zero
 NSZO → CC4 (6A27)

ACAB (19B23)
 CAB00-07 → ADAT0-7

IDATL (30B30)
 ADAT4-7 → IO-3

AP4 (17B22)
 IO-3 → AO-3
 ADAT0-3 → AH-7

[+ CAB00.CAB01] = ISPO (23B47)
sign in M.S.D.
 [+ CAB00.CAB02] = ISPI (23B44)
sign in L.S.D.
 [+ CAB04.CAB05]
 [+ CAB04.CAB06]

(ISPO+ISPI) → CC1 (6A33)
illegal digit or sign.

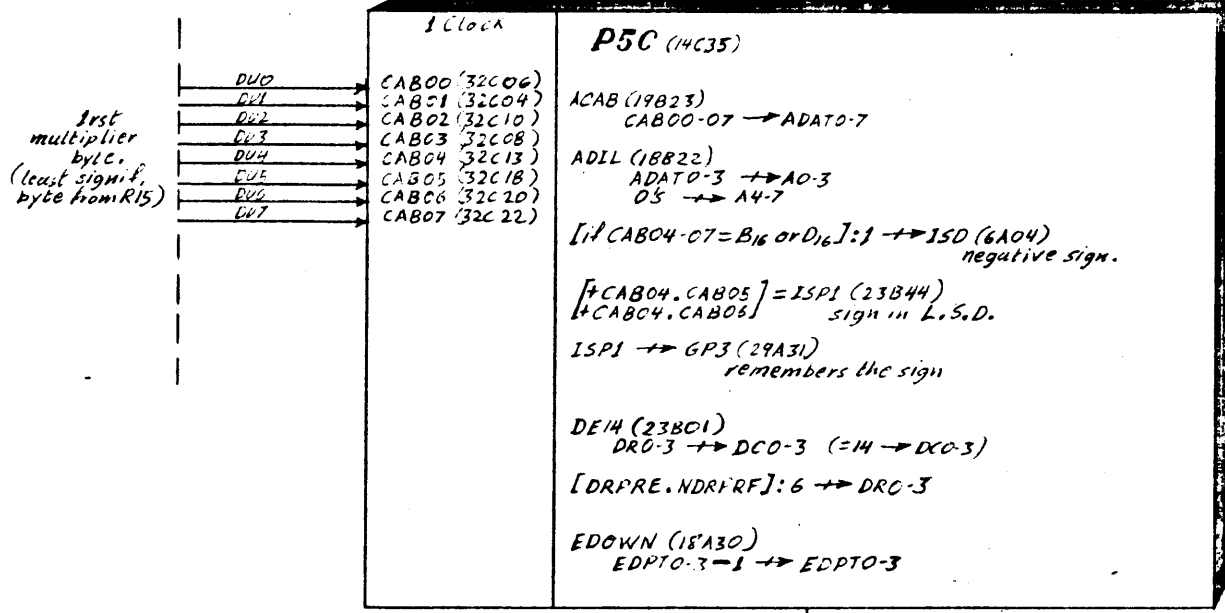
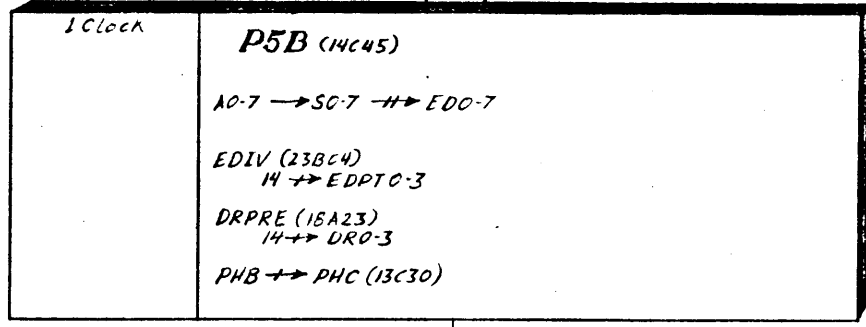
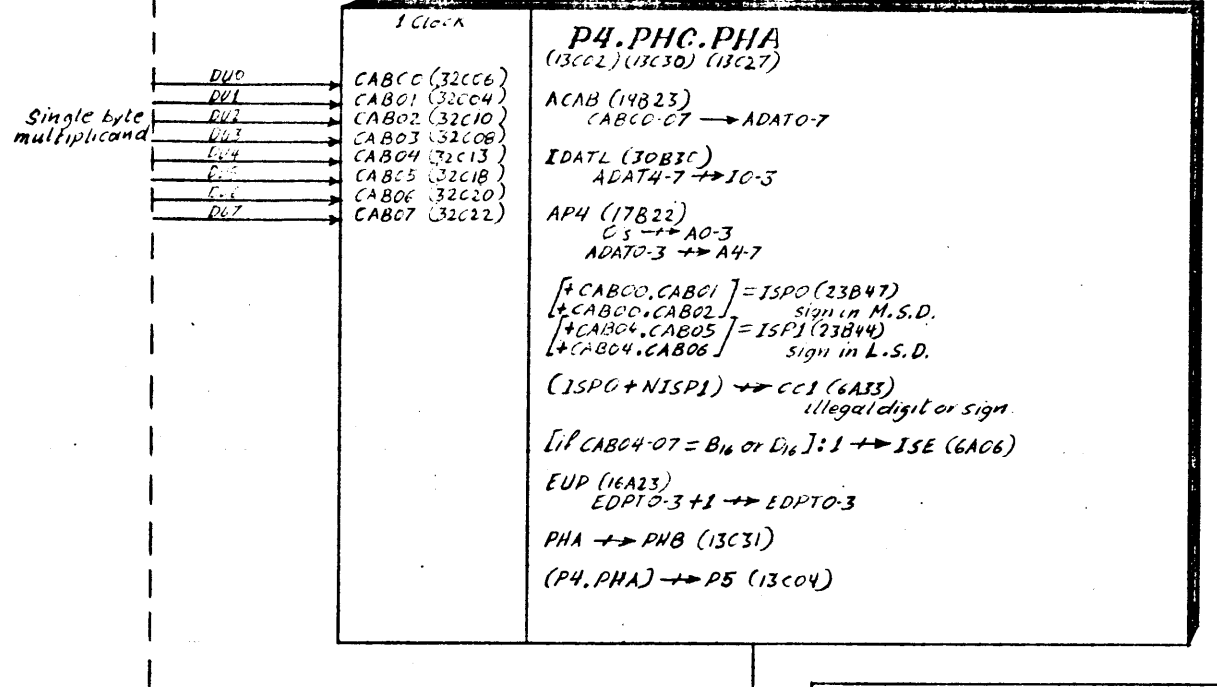
[if CAB04-07 = B₁₆ or D₁₆]: 1 → ISE (6A06)
negative sign.

EUP (16A23)
 EDPT0-3+1 → EDPT0-3

PHA → PHB (13C31)
 (P4.PHA) → P5 (13C04)

P5B

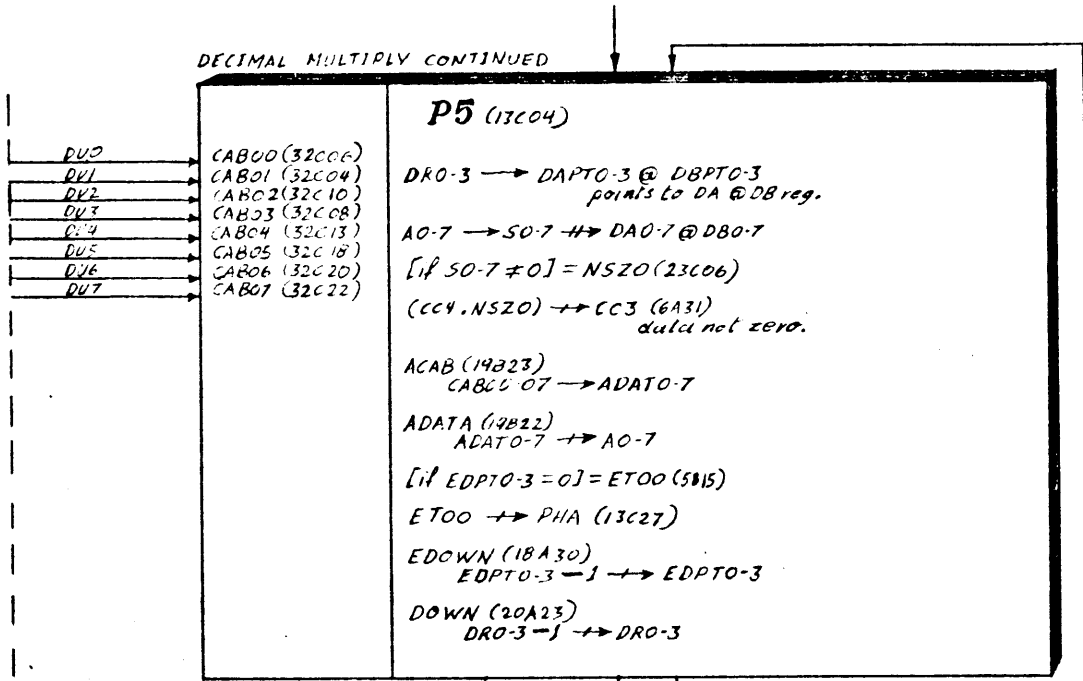
DECIMAL MULTIPLY CONTINUED



P5

DECIMAL MULTIPLY CONTINUED

Multiplier.

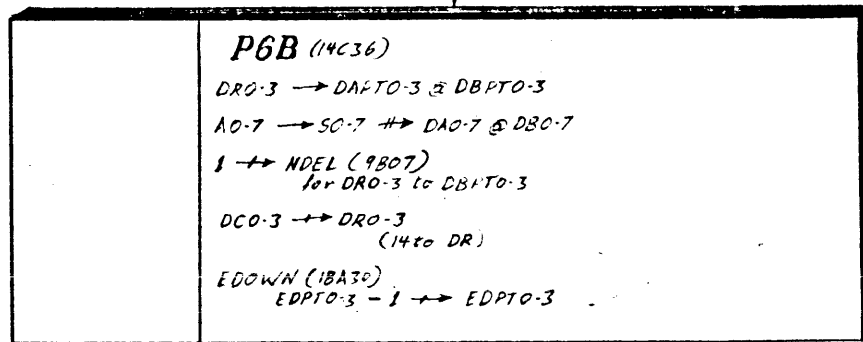
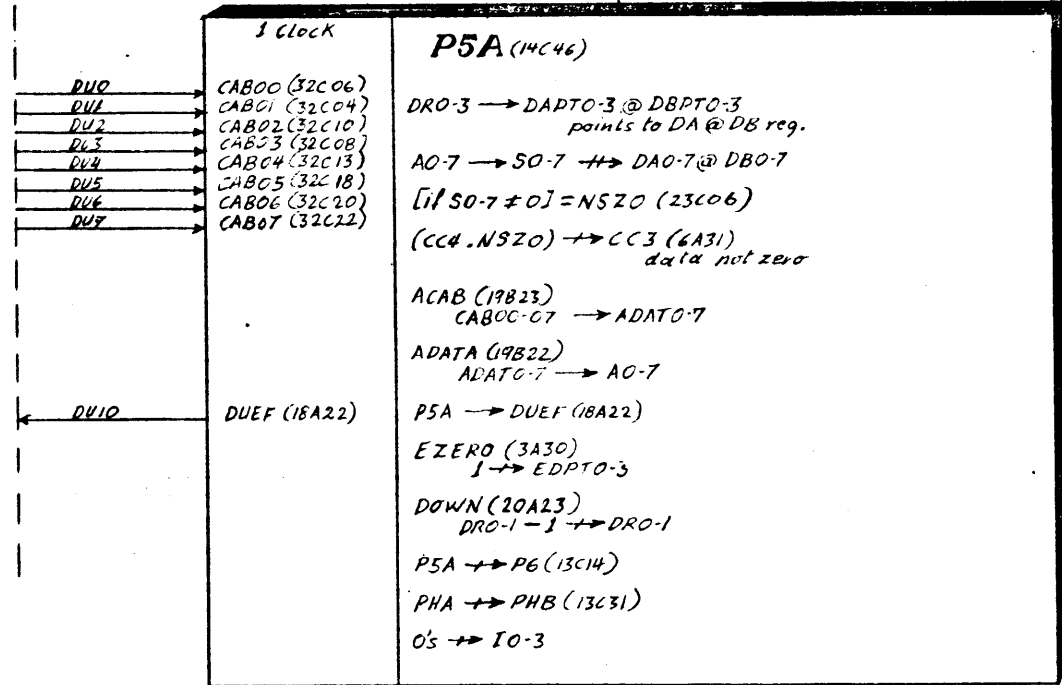


ETOO

NETOO

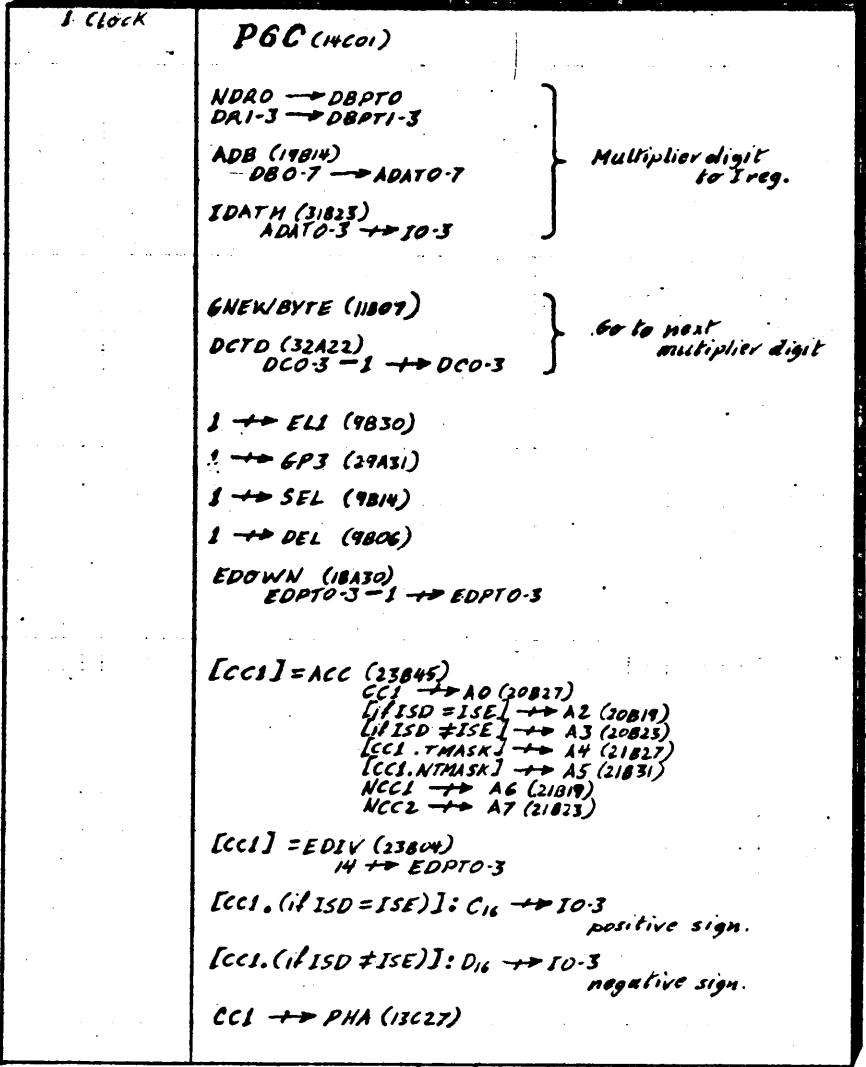
Last most signif. byte of multiplier.

DUEND.



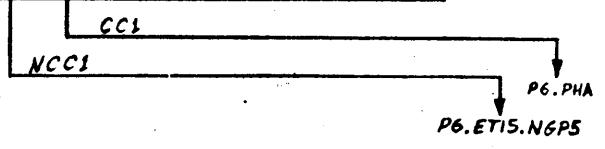
P6C

DECIMAL MULTIPLY CONTINUED



Multiplier digit to I reg.

Go to next multiplier digit



DECIMAL MULTIPLY CONTINUED

P6. ET01
(13C14) (5B14)

[DEL]: DWO-3 → DBPTO-3
DB reg. pointer.
SO-7 → DBO-7

[NDEL]: DWO-3 → DAPTO-3
DA reg. pointer.
SO-7 → DAO-7

} Store last byte of product

[if I=0] = IZERO (15B14)

[IZERO]: DEL → NDEL (9B07)
or
NDEL → DEL (9B06)

} If previous multiplier digit was zero, invert DEL

DCO-3 → DRO-3
for adding multiplicand to proper partial product digit
and for accessing prev or multiplier digit.

[if IO-3=1]: IO-3-1 → IO-3
[if IO-3=2 or 3 or 4 or 5]: IO-3-2 → IO-3
[if IO-3=6 or 7 or 8]: IO-3+2 → IO-3
[if IO-3=9]: IO-3+1 → IO-3

} If Ireg is not 0 or 10
increment or decrement Ireg.

EDOWN (18A30)
EDPTO-3-1 → EDPTO-3
gives us ET00

P6. ET00
(13C14) (5B15)

[DEL]: NDRO → DAPTO
DRI-3 → DAPT1-3
address multiplier in DAreq.
ADA (19B30)
DAO-7 → ADATO-7

[NDEL]: NDRO → DBPTO
DRI-3 → DBPT1-3
address multiplier in DBreg.
ADB (19B14)
DBO-7 → ADATO-7

} Multiplier digit to Ireg
if IZERO

[if IO-3=0 or 10] = IZERO (15B14)

[IZERO.SEL] = IDATL (30B30)
ADAT4-7 → IO-3

[IZERO.NSEL] = IDATM (31B23)
ADATO-3 → IO-3

[IZERO.NSEL] = 6NEWBYTE (11B07)

[6NEWBYTE] = DCTO (32A22)
DCO-3-1 → DCO-3

} Go to next multiplier byte.

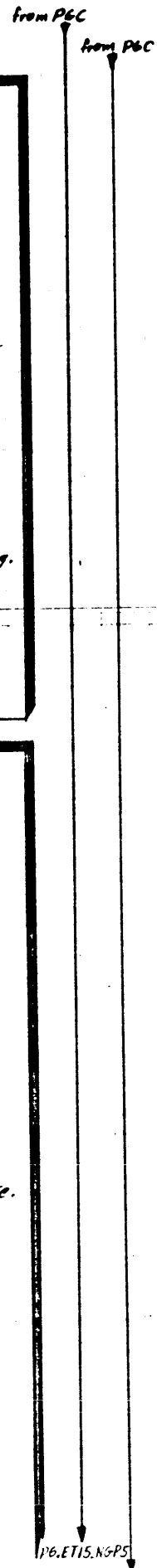
6NEWBYTE → EL1 (9B30)
remembers 6NEWBYTE

[if IO-3=10]: 1 → 6P2 (29A30)
remembers previous subtraction.

IZERO → 6P3 (29A31)
remembers IZERO

[IZERO]: SEL → NSEL (9B12)
or
NSEL → SEL (9B14) } Invert SEL

DEL → NDEL (9B07)
NDEL → DEL (9B06) } Invert DEL



P6.ETO1

from P6C

from P6C

DECIMAL MULTIPLY CONTINUED

[SEL] = DUP (26A22)
DRO-3+1 → DRO-3

EDOWN (18A30)
EDPTO-3-1 → EDPTO-3

(NDRO.NDR3) → ELAST (31A46)
last iteration.

14 → DRO-3

[ELAST.NSEL] = ACC (23B45)
[(ISD=ISE).CC3] → A2 (20A19)
[(ISD≠ISE).CC3] → A3 (20A23)
NCC1 → A6 (21B19)
NCC2 → A7 (21B23).

[ELAST.NSEL] = EDIV (23B04)
14 → EDPTO-3

[ELAST.NSEL.(if ISD=ISE)]: C₁₆ → IO-3
positive sign.

[ELAST.NSEL.(if ISD≠ISE)]: D₁₆ → IO-3
negative sign.

(ELAST.NSEL) → PHA (13C27).

Supersedes previous logic

ELAST.NSEL

P6.ET15.NGP5

(13C14) (2A37) (6A21)

GP3 → GP5 (6A02)
remembers IZERO

(GP3.EL1) → EL1 (9B30)
remembers GNEWBYTE

[GP2]: IO-3+1 → IO-3
increment multiplier digit (multiplicand x10)
if previous multiplier digit was =>6 and
multiplicand was subtracted.

DRO-3 → DW0-3

[NGP3] = EDOWN (18A30)
EDPTO-3-1 → EDPTO-3

GP3

NGP3

P6.ET15.GP5

(13C14) (2A37) (6A02)

GP5 → GM15/5 (18C14)

[if IO-3=0] = IT00 (4B34)
new multiplier digit is zero

[GM15/5.IT00] = EZERO (3A30)
1 → EDPTO-3

[NEZERO] = EDOWN (18A30)
EDPTO-3-1 → EDPTO-3

[NEL1] = DOWN (20A23)
DRO-3-1 → DRO-3

0's → ELO-3

DRO-3 → DW0-3

EZERO

P6

P6

P6.PHA

from P6

DECIMAL MULTIPLY CONTINUED

P6 (13C14)

[DEL]: DRO-3 → DAPTO-3
 DA reg. pointer
 ADA (19830)
 DAO-7 → ADATO-7

[INDEL]: DRO-3 → DBPTO-3
 DB reg. pointer.
 ADB (19814)
 DBO-7 → ADATO-7

ADATA (19822)
 ADATO-7 → AO-7

Partial product to Areg.

EDO-3 ↔ ELO-3

[SEL]: ED4-7 → ESHO-3
 ELO-3 → ESH4-7

[NSEL]: EDO-7 → ESHO-7

[if IO-3 = 2-8]: ESHO-7.X2 ↔ BO-7

[if IO-3 = 1 or 9]: ESHO-7 ↔ BO-7

Multiplicand to Breg.

[if IO-3 = 5] = NSUB (17C23)
 AO-7 + BO-7 → SO-7

[if IO-3 = 6] = SUB (2836)
 AO-7 - BO-7 → SO-7

Add or subtract A and B.

[DEL]: DWO-3 → DBPTO-3
 DB reg. pointer

SO-7 ↔ DBO-7

[INDEL]: DWO-3 → DAPTO-3
 DA reg. pointer

SO-7 ↔ DAO-7

Store result.

[if EDPTO-3 = NR28-31] = EDMA (12A46)

EDMA → EZERO (3A30)
 1 ↔ EDPTO-3

[NEZERO] = EDOWN (16A30)
 EDPTO-3 - 1 ↔ EDPTO-3

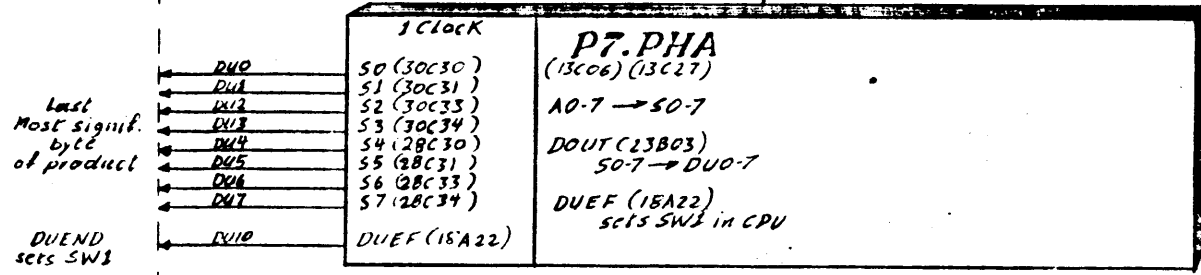
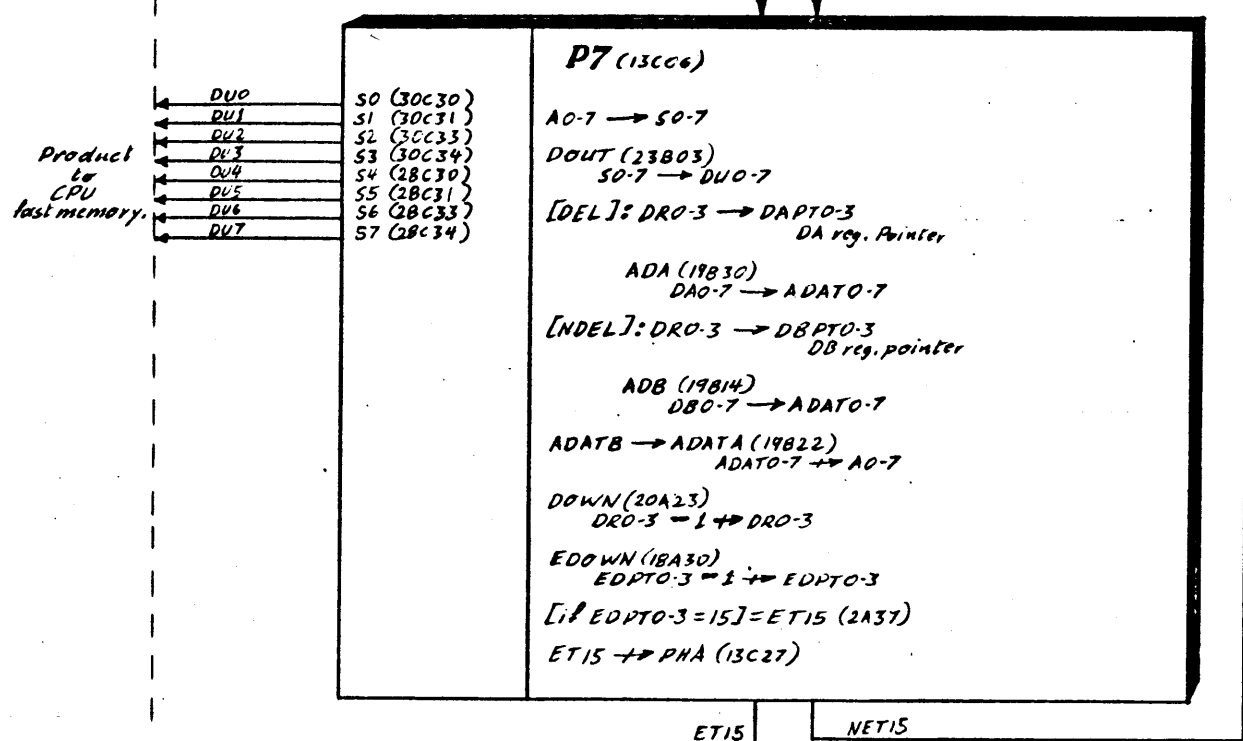
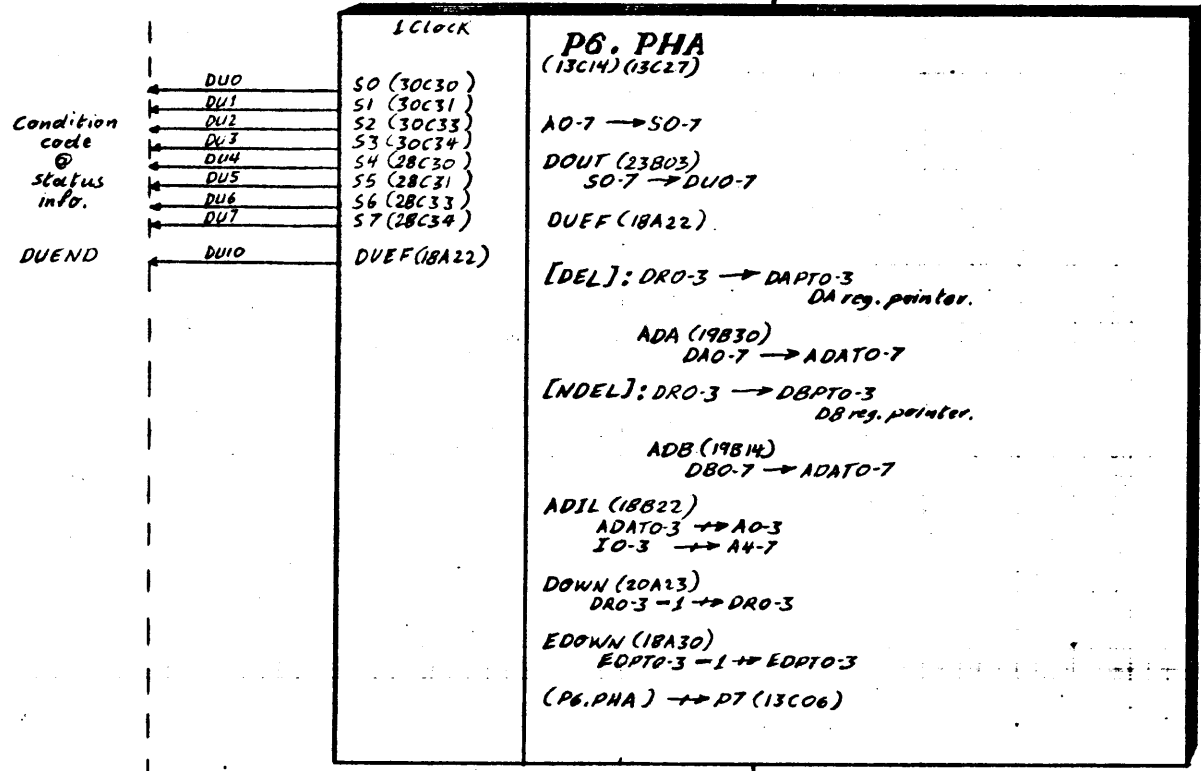
DOWN (20A23)
 DRO-3 - 1 ↔ DRO-3

DRO-3 ↔ DWO-3

NEZERO

EZERO

DECIMAL MULTIPLY CONTINUED



DECIMAL MULTIPLY INTERRUPTED

(differences only)

INT → DUI2 → CAB12 (32C40)
 (incPU) (CAB12.P6.ET00) → RSTA (6A14)
 wait for next ET01

P6. ET01
 (13C14) (5B14)
 no change in DEL (9806)
 no change in Ireg. (multiplier digit)

P6. ET00
 (13C14) (5B15)
 [SEL] = DCTU (32A30)
 DCO-3 + 1 → DCO-3
 no change in DEL (9806) or Ireg. (multiplier digit)
 RSTA → PHA (13C27)

P6. PHA
 (13C14) (13C27)
 ADIL (18B22)
 ADAT0-3 → A0-3
 IO-3 → A4-7 (multiplier digit)
 DCTU (32A30)
 DCO-3 + 1 → DCO-3

P7 (13C06)
 [if DCO-3 = 6] = RST7 (3A07)
 time to insert multiplier sign.
 [NRST7] = ADATA (14B22)
 ADAT0-7 → A0-7
 1st partial product
 then multiplier to Areg.
 [GP2.ISD]: B → IO-3
 [GP2.NISD]: A → IO-3
 [NGP2.ISD]: D → IO-3
 [NGP2.NISD]: C → IO-3
 [RST7.SEL] = ADIM (17B23)
 IO-3 → A0-3
 ADAT4-7 → A4-7
 [RST7.NSEL] = ADIL (18B22)
 ADAT0-3 → A0-3
 IO-3 → A4-7
 Generates multiplier sign
 remembers GP2
 DCTU (32A30)
 DCO-3 + 1 → DCO-3

ET15

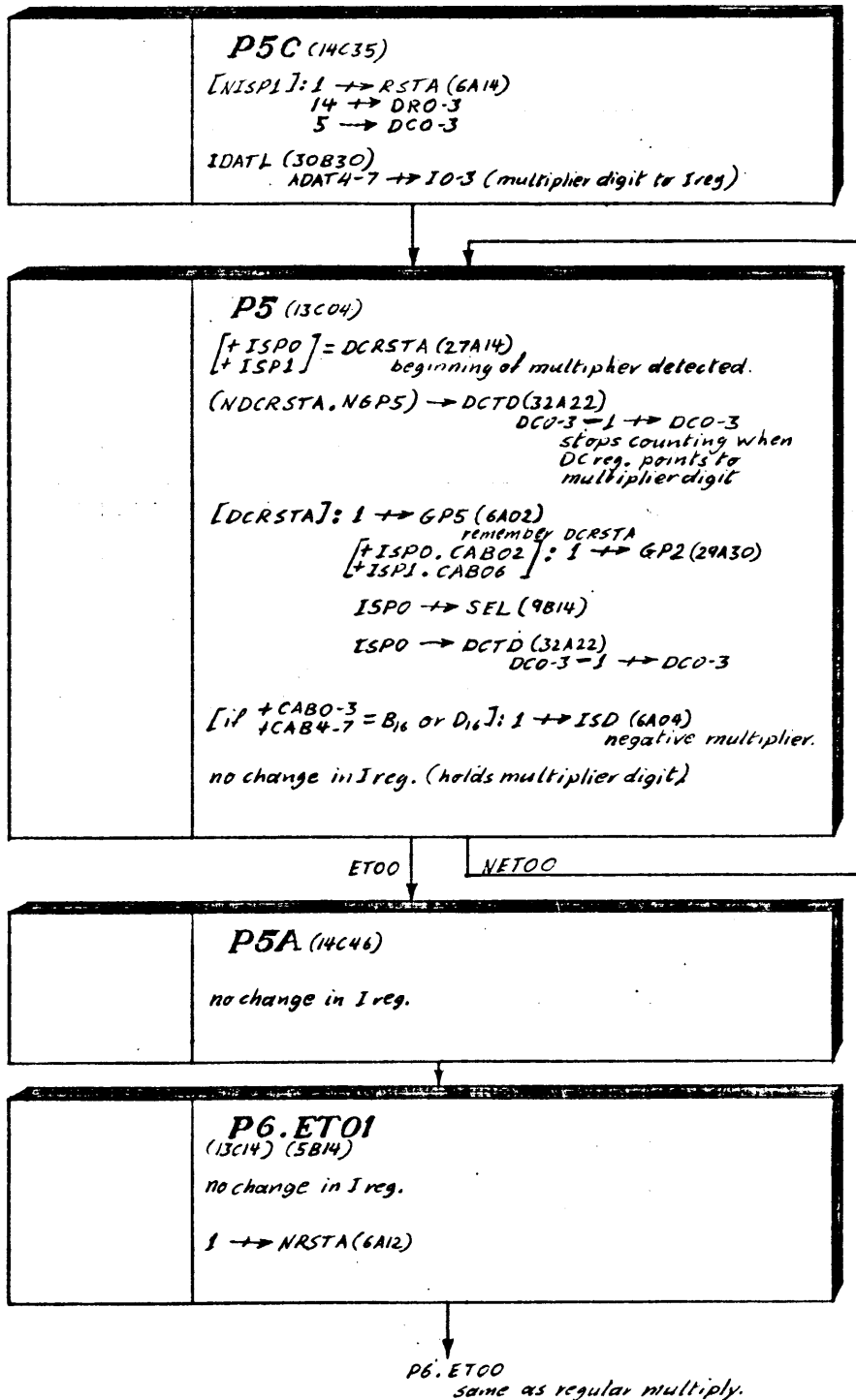
NET15

P7. PHA
 (13C06) (13C27)
 I → NRSTA (6A12)

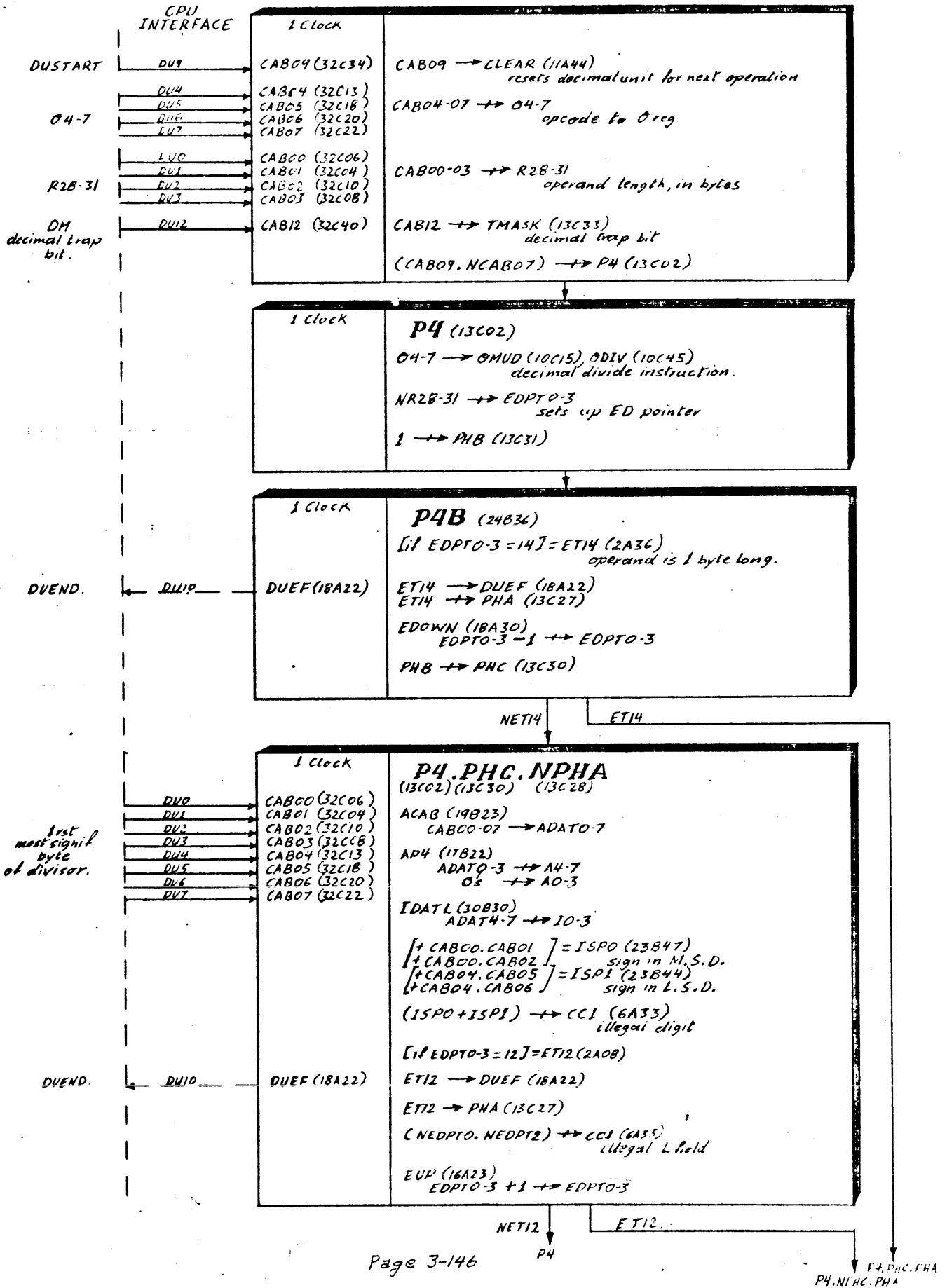
MULTIPLY REENTRY AFTER INTERRUPT

(differences only)

Same as regular multiply until P5C



DECIMAL DIVIDE (7A)



DECIMAL DIVIDE CONTINUED

Divisor.

- DU0
- DU1
- DU2
- DU3
- DU4
- DU5
- DU6
- DU7

P4 (13C02)

AO-7 → SO-7 → EDO-7
divisor to EDreg.

[if SO-7 ≠ 0] = NSZO (23C06)
data not zero

NSZO → CC4 (6A27)

ACAB (19B23)
CAB00-07 → ADAT0-7

IDATL (30B30)
ADAT4-7 → IO-3

AP4 (17B22)
IO-3 → AO-3
ADAT0-3 → A4-7

[+ CAB00.CAB01] = ISPO (23B47)
sign in M.S.D.
[+ CAB00.CAB02] = ISPI (23B44)
sign in L.S.D.
[+ CAB04.CAB05] = ISPI (23B44)
sign in L.S.D.

(ISPO + ISPI) → CCI (6A33)
illegal digit

[if EDPT0-3 = 12] = ET12 (2A08)
sets SW1 in CPU

ET12 → PHA (13C27)

ET12 → DUEF (18A22)

(NEDPT0.NEDPT2) → CCI (6A33)
illegal L field

EUP (16A23)
EDPT0-3 + 1 → EDPT0-3

DUEND

DUI0

DUEF (18A22)

ET12

NET12

least signif. byte of divisor.

- DU0
- DU1
- DU2
- DU3
- DU4
- DU5
- DU6
- DU7

1 Clock

P4.NPHC.PHA
(13C02) (13C39) (13C27)

AO-7 → SO-7 → EDO-7

[if SO-7 ≠ 0] = NSZO (23C06)
data not zero

NSZO → CC4 (6A27)

ACAB (19B23)
CAB00-07 → ADAT0-7

IDATL (30B30)
ADAT4-7 → IO-3

AP4 (17B22)
IO-3 → AO-3
ADAT0-3 → A4-7

[+ CAB00.CAB01] = ISPO (23B47)
sign in M.S.D.
[+ CAB00.CAB02] = ISPI (23B44)
sign in L.S.D.
[+ CAB04.CAB05] = ISPI (23B44)
sign in L.S.D.

(ISPO + NISPI) → CCI (6A33)
illegal digit or sign

[if CAB04 07 = B₁₆ or D₁₆] : 1 → ISE (6A06)
negative sign.

EUP (16A23)
EDPT0-3 + 1 → EDPT0-3

PHA → PHB (13C31)

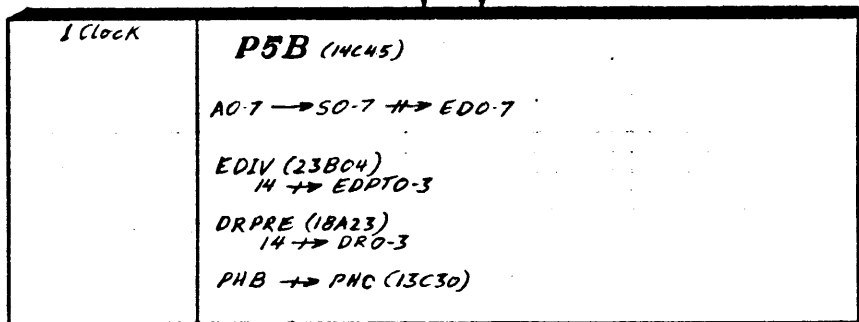
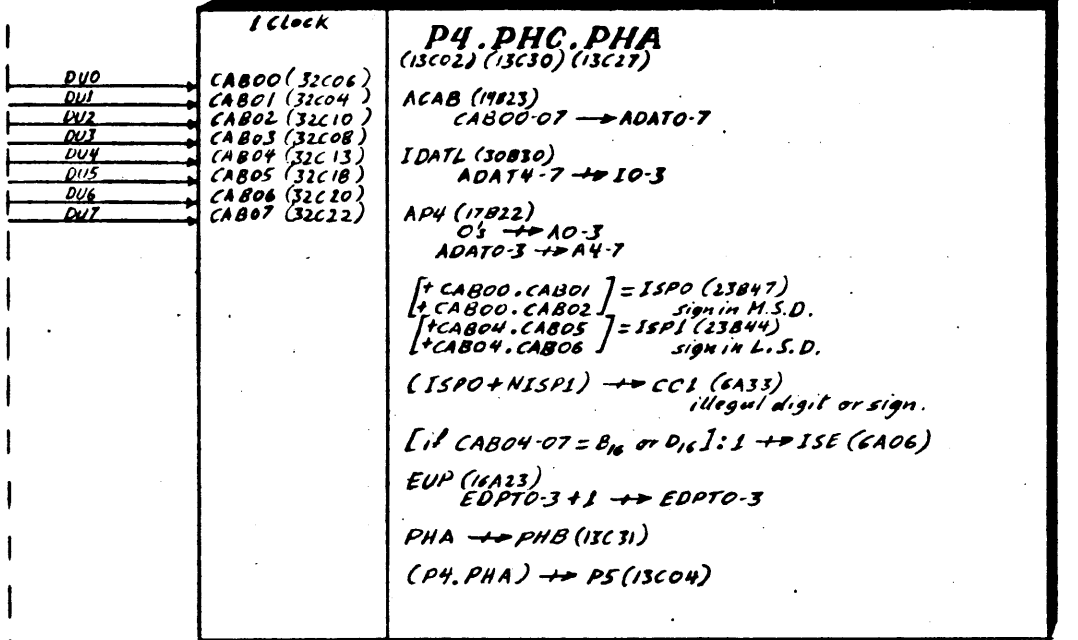
(P4.PHA) → P5 (13C04)

P5B

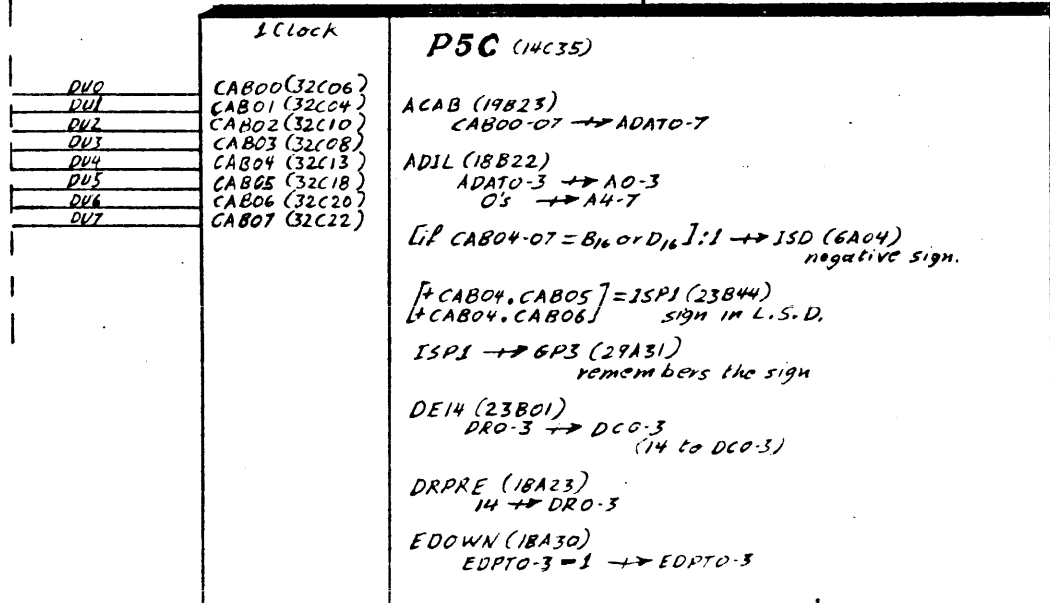
P4.NPHC.PHA

DECIMAL DIVIDE CONTINUED

Single
byte
divisor.



1st
dividend
byte
from R15



P5

DECIMAL DIVIDE CONTINUED

Dividend.

- DU0
- DU1
- DU2
- DU3
- DU4
- DU5
- DU6
- DU7

P5 (13C04)

CAB00 (32C06)
 CAB01 (32C04)
 CAB02 (32C10)
 CAB03 (32C08)
 CAB04 (32C13)
 CAB05 (32C18)
 CAB06 (32C20)
 CAB07 (32C22)

DRO-3 → DAPTO-3 @ DBPTO-3
 points to DA @ DB reg.

A0-7 → S0-7 → H → DAO-7 @ DB0-7

ACAB (19B23)
 CAB00-07 → ADATO-7

ADATA (19B22)
 ADATO-7 → A0-7

[if EDPTO-3 = 0] = ETOO (5B15)

ETOO → PHA (13C27)

EDOWN (18A30)
 EDPTO-3 - 1 → EDPTO-3

DOWN (20A23)
 DRO-3 - 1 → DRO-3

ETOO NETOO

Last most signif digit of dividend.

- DU0
- DU1
- DU2
- DU3
- DU4
- DU5
- DU6
- DU7

P5A (14C46)

CAB00 (32C06)
 CAB01 (32C04)
 CAB02 (32C10)
 CAB03 (32C08)
 CAB04 (32C13)
 CAB05 (32C18)
 CAB06 (32C20)
 CAB07 (32C22)

DRO-3 → DAPTO-3 @ DBPTO-3
 points to DA @ DB reg.

A0-7 → S0-7 → H → DAO-7 @ DB0-7

ACAB (19B23)
 CAB00-07 → ADATO-7

ADATA (19B22)
 ADATO-7 → A0-7

PSA → DUEF (18A22)

EDNO (31C06)
 1 → EDPT1 (10A25)
 1 → EDPT2 (00A19)

EZERO (3A30)
 1 → EDPT3
 sets ED pointer to 7

DOWN (20A23)
 DRO-3 - 1 → DRO-3

1 → GPU (29A27)

PSA → P6 (13C14)

PHA → PHB (13C31)

DUEND ← DU10

P6B (14C36)

DRO-3 → DAPTO-3 @ DBPTO-3
 points to DA @ DB reg.

A0-7 → S0-7 → H → DAO-7 @ DB0-7

[if EDPTO-3 = NR28-31] = EDMA (12A46)

EDMA → GPI (29A33)
 ED pointer points to N.S. Byte of divisor.

CC1 → P6.6ABORT (23A14)

P6.6ABORT

DECIMAL DIVIDE CONTINUED

P6.GP4 Normalization
(13C14) (29A27)

[$(B0-7 \neq 0).GP1.N\&P3$] = BSIGF (11B37)
1st none zero byte in divisor

[BSIGF]: 1 → GP3 (29A31)
stops ED pointer until none zero dividend byte is detected.

[BSIGF] = EDOWN (18A30)
EDPTO-3 - 1 → EDPTO-3
go back to none zero divisor byte.

DOWN (20A25)
DRO-3 - 1 → DRO-3
back up DRO-3 same as ED pointer.

[$(A0-7 \neq 0).N\&P2$] = ASIGF (24B14)
1st none zero byte in dividend

[ASIGF]: 1 → GP2 (29A30)
allows the count down of DRO-3 and EDPTO-3 with GP3 set.

[+ASIGF.NBSIGF.(A0-3 ≠ 3)] = EUP (16A23)
EDPTO-3 + 1 → EDPTO-3

[+ASIGF.NBSIGF.(B0-3 = 0)] : 1 → SEL (9B14)
shifts divisor 1 digit left

ED0-7 → B0-7
divisor to B reg.

ADA (19B30)
DAO-7 → ADAO-7

ADATA (19B22)
ADATO-7 → A0-7
dividend to A reg.

[if EDPTO-3 = NR28-31] = EDMA (12A46)

EDMA → GP1 (29A33)
ED pointer now looking at divisor.

[GP2.N\&P3]: 1 → CC2 (6A30)
overflow, abort the operation.

[+(DRO-3 = 15).GP3] = GP4R (27A30)
normalization finished.

[GP4R]: 1 → N\&P4 (29A28)
1 → N\&P3 (29A26)
1 → N\&P2 (29A29)
EZERO (3A30)
1 → EDPTO-3

[NBSIGF.N\&P3] = EUP (16A23)
EDPTO-3 + 1 → EDPTO-3

[N\&P4R.GP2.GP3] = EUP (16A23)
EDPTO-3 + 1 → EDPTO-3

[N\&P4R]: DRO-3 → DCO-3
keeps track of difference between divisor and dividend for proper subtraction.

[NASIGF.NBSIGF] = DUP (26A22)
DRO-3 + 1 → DRO-3

GP4.NCC2

S/C22

EZERO

P6.GABCKT

DECIMAL DIVIDE CONTINUED

P6.ET01
(13C14) (5814)

P6 → SUB (2836)

A0-7 → B0-7 → S0-7

[DEL]: DWO-3 → DBPT0-3
S0-7 → DB0-7

[NDEL]: DWO-3 → DAPTO-3
S0-7 → DAO-7

DCO-3 → DRO-3

EDOWN (18A30)
EDPT0-3 - 1 → EDPT0-3
go to ET00

} store last byte of new dividend.

P6.ET00
(13C14) (5815)

I3 → GP3 (29A31)
remembers to store quotient digit.

[NI3.NI0.NSCOS]: IO-3 + 2 → IO-3

[IO.NI3.NSCOS]: IO-3 + 1 → IO-3

[SCOS]: IO-3 - 1 → IO-3

(NSCOS.DEL) → NDEL (9807)

(NSCOS.NDEL) → DEL (9806)

} Invert DEL

[NSCOS.(I≠0).(DCO-3=6)]: 1 → CC2 (6A30)
overflow

EDOWN (18A30)
EDPT0-3 - 1 → EDPT0-3

} Update quotient digit held in I reg.

CC2

P6.ET15
(13C14) (2A37)

[IO-3 ≠ 0]: 1 → CC3 (6A71)
quotient not zero.

[GP3]: 1 → GP2 (29A30)
remembers to store quotient digit

NDR0 → DAPTO + DBPT0
DRI-3 → DAPTI-3 + DBPTI-3

[ADA]: DAO-7 → ADAT0-7
[ADB]: DBO-7 → ADA0-7

[GP3.NSEL]: ADIL (18B22)
IO-3 → A4-7

[GP3.SEL]: ADIM (17B23)
IO-3 → A0-3
ADAT4-7 → A4-7

} Put quotient digits in A reg.

[GP3.NSEL]: DCTU (32A30)
DCO-3 + 1 → DCO-3

(GP3.SEL) → NSEL (9812)
(GP3.NSEL) → SEL (9814)

[GP3]: 0's → IO-3

[NGP3] = EDOWN (18A30)
EDPT0-3 - 1 → EDPT0-3

NGP3

P6.ET15.GP2

P6.GABORT

P6.ET01

DECIMAL DIVIDE CONTINUED

P6.ET15.GP2
(13C14) (2A37) (27A30)

DCOM (23A22)
NDKO → DAPTO @ DBPTO
DRI-3 → DAPT1-3 @ DBPT1-3
AO-7 → SO-7 → DAO-7 @ DBO-7

} Store quotient byte in both DA and DB reg.

[GP2]: 2 → IO-3
[SEL.NDT14] = DUP (26A22)
DRO-3+1 → DRO-3
[NDT14] = EDOWN (18A30)
EDPTO-3-1 → EDPTO-3

[if DRO-3 = 14] = DT14 (21A38)
DT14 = ACC (23B45) goto ET14
[CC3.(ISD=ISE)] → A2
[CC3.(ISD≠ISE)] → A3
NCC1 → A6
NCC2 → A7

} END of divide iterations.

[ISD=ISE]: C₁₆ → IO-3
positive sign.
[ISD≠ISE]: D₁₆ → IO-3
negative sign.

EDIV (23B04)
14 → EDPTO-3
DRPRE (18A23)
14 → DRO-3
[DT14]: 1 → PHA (13C27)

DT14

P6.ET14
(13C14) (2A36)

[DEL]: DRO-3 → DAPTO-3
ADA
DAO-7 → ADATO-7

[NDEL]: DRO-3 → DBPTO-3
ADB
DBO-7 → ADATO-7

} Dividend to Areg.

ADATA (19B22)
ADATO-7 → AO-7

EDO-3 → ELO-3

[NSEL]: EDO-7 → ESHO-7
[SEL]: ED4-7 → ESHO-3
ELO-3 → ESH4-7

} Divisor to Breg.

[NI3]: ESHO-7 x2 → BO-7
[I3]: ESHO-7 → BO-7

[if EDPTO-3 = NR28-31] = EDMA (12A46)
[EDMA] = EZERO (3A30)
1 → EDPTO-3
[NEDMA] = EDOWN (18A30)
EDPTO-3-1 → EDPTO-3

DRO-3 → DWO-3
DOWN (20A23)
DRO-3-1 → DRO-3

P6

P6.PHA

P6.GABORT

DECIMAL DIVIDE CONTINUED

P6 (13C14)

P6 → SUB (2836)
 AO-7 = BO-7 → SO-7
 [DEL]: DWO-3 → DBPTO-3
 SO-7 → DBO-7
 [NDEL]: DWO-3 → DAPTO-3
 SO-7 → DAO-7

 [DEL]: DRO-3 → DAPTO-3
 ADA (14830)
 DAO-7 → ADATO-7
 [NDEL]: DRO-3 → DBPTO-3
 ADB (19814)
 DBO-7 → ADATO-7

 EDO-3 ↔ ELO-3
 [NSEL]: EDO-7 → ESHO-7
 [SEL]: ED4-7 → ESHO-3
 ELO-3 → ESH4-7
 [NI3]: ESHO-7 x2 ↔ BO-7
 [I3]: ESHO-7 ↔ BO-7

 [if EDPTO-3 = NR28-31] = EDMA (12A46)
 [EDMA] = EZERO (3A30)
 I ↔ EDPTO-3
 [NEZERO] = EDOWN (18A30)
 EDPTO-3 - 1 ↔ EDPTO-3

 DRO-3 ↔ DWO-3
 DOWN (20A23)
 DRO-3 - 1 ↔ DRO-3

NEZERO

EZERO

P6.6ABORT (13C14) (23A14)

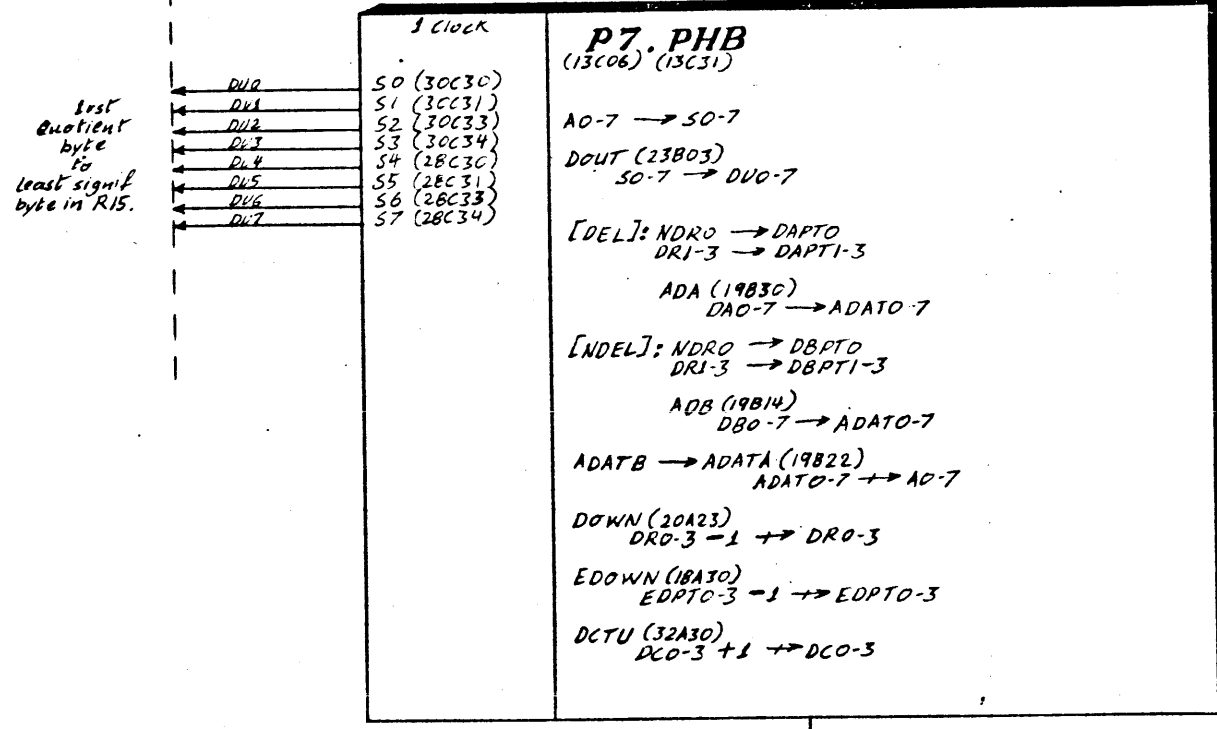
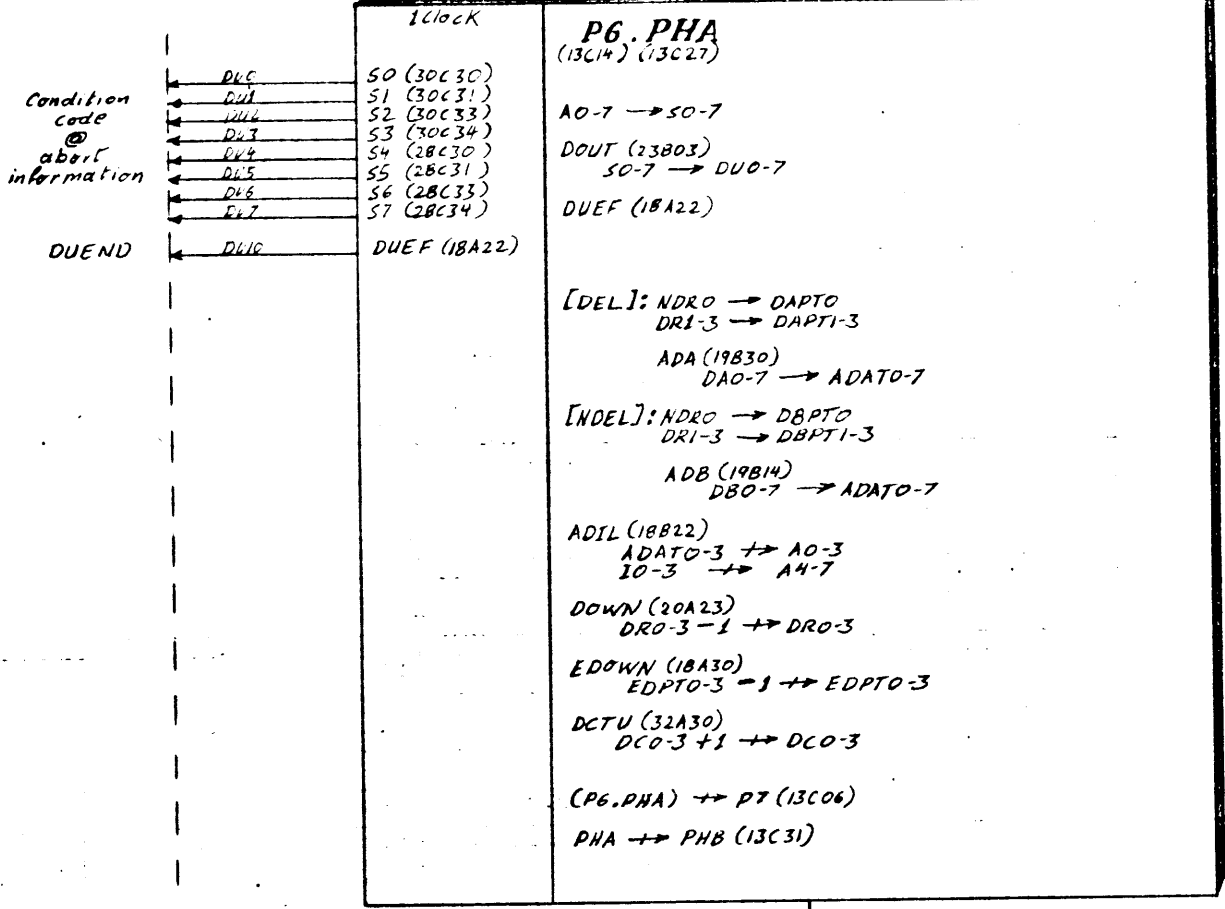
ACC (23B45)
 CC1 ↔ AO (20B27)
 CC2 ↔ AI (20B31)
 [CC3. (ISD=ISE)] ↔ AZ (20B19)
 [CC3. (ISD≠ISE)] ↔ A3 (20B23)
 [CC1. TMASK] ↔ A4 (21B27)
 [CC1. NTMASK] ↔ A5 (21B31)
 NCC1 ↔ A6 (21B19)
 NCC2 ↔ A7 (21B23)

 [ISD=ISE]: C₁₆ ↔ IO-3
 positive sign.
 [ISD≠ISE]: D₁₆ ↔ IO-3
 negative sign.

 EDIV (23B04)
 I4 ↔ EDPTO-3
 DRPRE (18A23)
 H ↔ DRO-3

 I ↔ PHA (13C27)

DECIMAL DIVIDE CONTINUED



P7

DECIMAL DIVIDE CONTINUED.

Quotient @
remainder
to CPU
fast memory.

- DU0 50 (30C30)
- DU1 51 (30C31)
- DU2 52 (30C33)
- DU3 53 (30C34)
- DU4 54 (28C30)
- DU5 55 (28C31)
- DU6 56 (28C33)
- DU7 57 (28C34)

PT (13C06)

A0-7 → S0-7

DOUT (23B03)
S0-7 → DU0-7

[DEL]: DRO → DAPTO
DRJ-3 → DAPT1-3

ADA (19B30)
DA0-7 → ADATO-7

[NDEL]: NDRO → DAPTO
DRJ-3 → DGPT1-3

ADB (19B14)
DB0-7 → ADATO-7

[ISD]: D₁₆ → IO-3
negative sign for remainder

[NISD]: C₁₆ → IO-3
positive sign for remainder.

[if DCO-3 = 6] = DCT6 (21A36)

[NDCT6] = ADATB → ADATA (19B22)
ADATO-7 → A0-7

[DCT6] = ADJL (18B22)
ADATO-3 → A0-3
IO-3 → A4-7

[if EDPT0-3 = 15] = ET15 (2A37)

[ET15]: 1 → PHA (13C27)

DOWN (20A23)
DRO-3 - 1 → DRO-3

EDOWN (18A30)
EDPT0-3 - 1 → EDPT0-3

DCTU (32A30)
DCO-3 + 1 → DCO-3.

ET15

NET15

Last
most signif.
byte
of remainder.

- DU0 50 (30C30)
- DU1 51 (30C31)
- DU2 52 (30C33)
- DU3 53 (30C34)
- DU4 54 (28C30)
- DU5 55 (28C31)
- DU6 56 (28C33)
- DU7 57 (28C34)
- DU10 DUEF (18A22)

DUEND

↓ Clock

PT, PHA
(13C06) (13C27)

A0-7 → S0-7

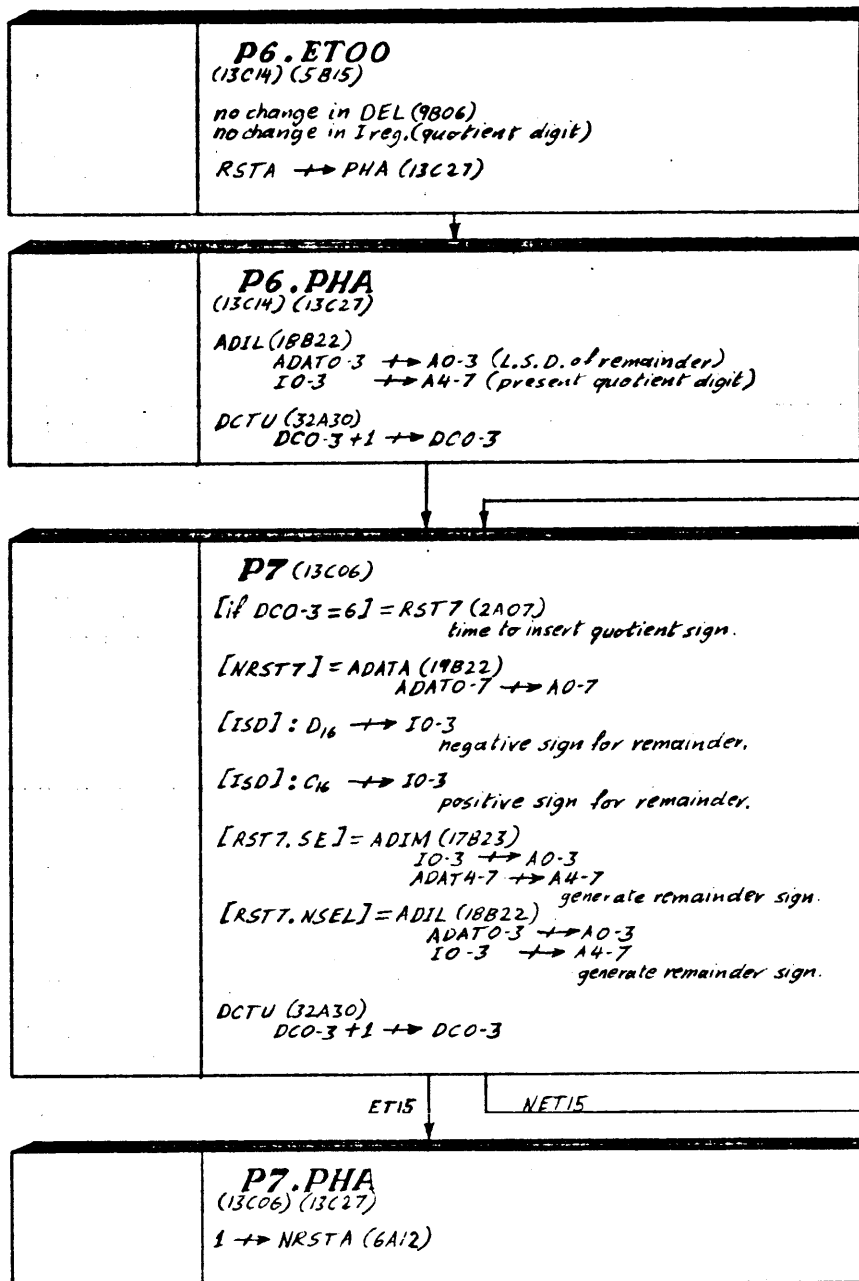
DOUT (23B03)
S0-7 → DU0-7

DUEF (18A22)

DECIMAL DIVIDE INTERRUPTED

(differences only)

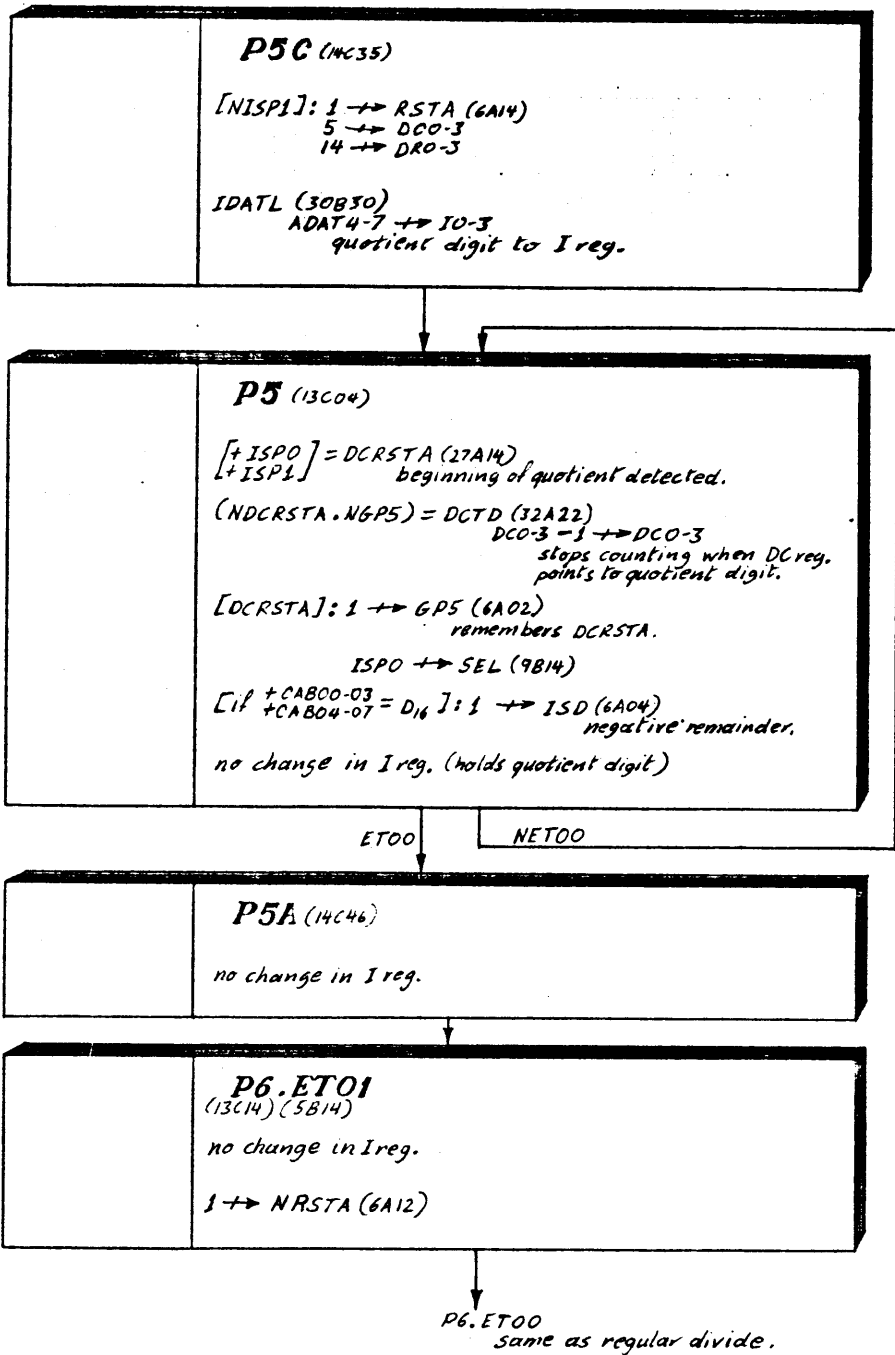
INT → DUI2 → CAB12 (32C40)
 (CAB12.P6.ET00) → RSTA (6A14)
 wait for next ET00



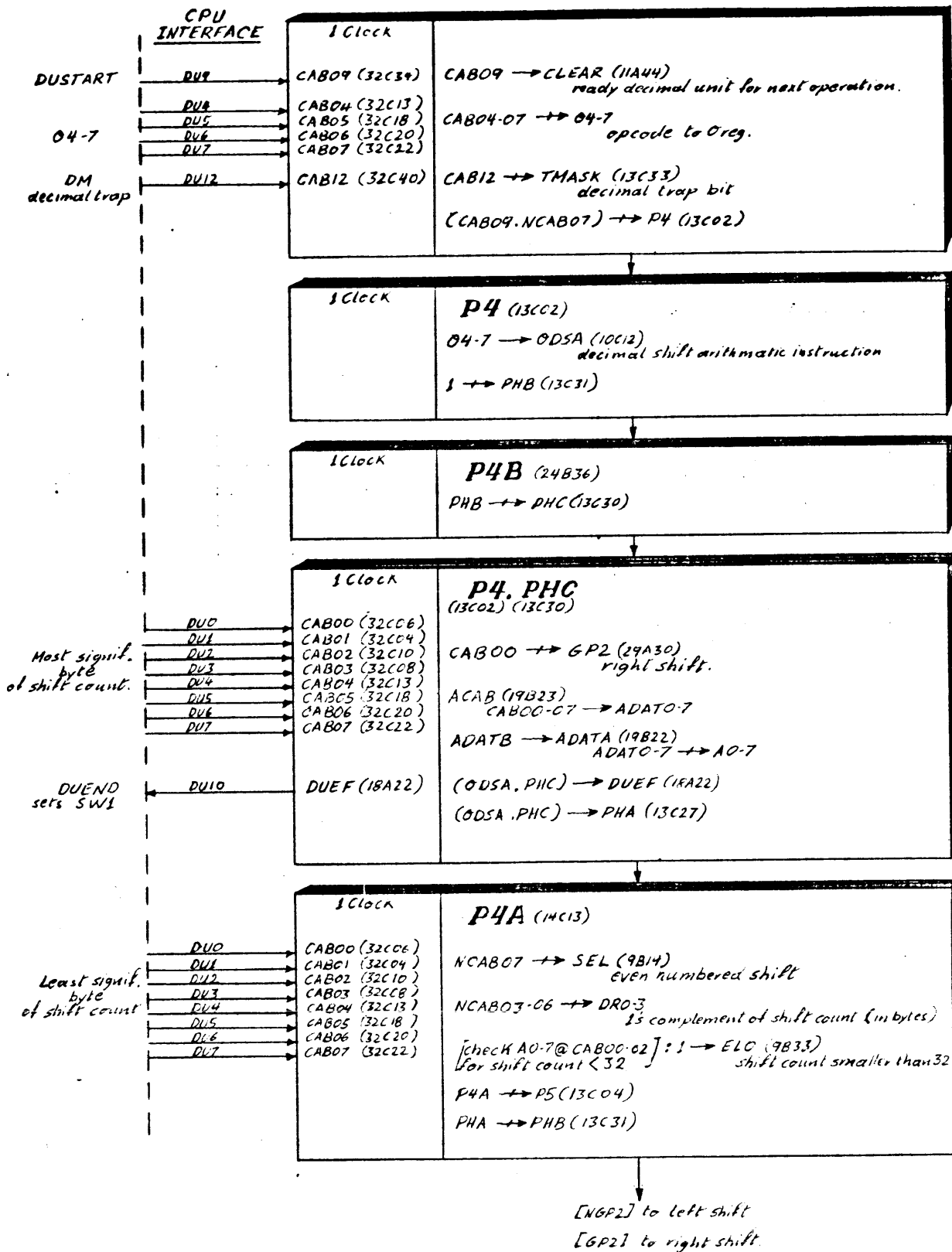
DIVIDE REENTRY AFTER INTERRUPT

(differences only)

Same as regular divide until P5C



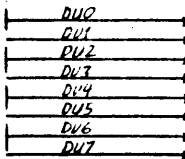
DECIMAL SHIFT ARITHMETIC (7C)



LEFT SHIFT (NGP2)

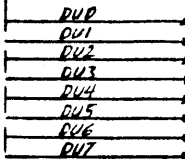
1 Clock	<p>P5B (14C45)</p> <p>EDIV (23B04) 14 → EDPTO-3</p> <p>O's → IO-3</p> <p>PHB → PHC (13C30)</p>
---------	---

Least signif.
byte
from CPU
fast memory.



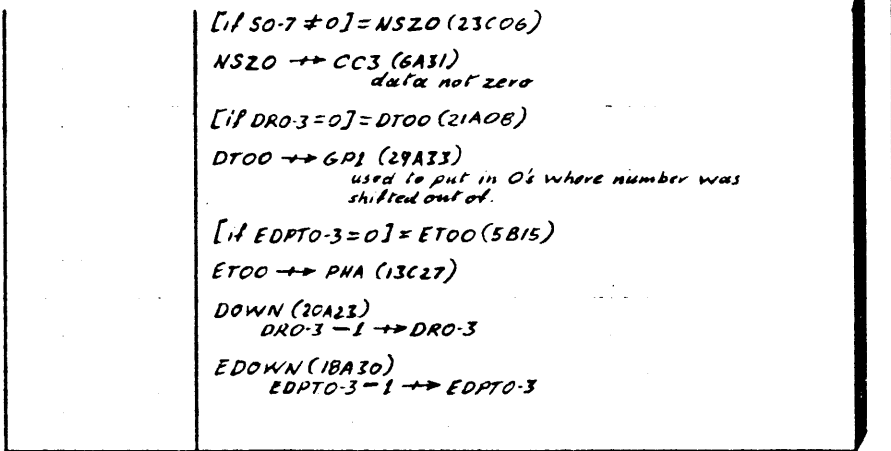
1 Clock	<p>P5C (14C35)</p> <p>[ELO] = ACAB (19823) CAB00-07 → ADATO-7</p> <p>[NELO]: O's → ADATO-7</p> <p>[SEL] = ADIL (18822) ADATO-3 → AO-3 IO-3 → A4-7</p> <p>[NSEL] = IDATM (31823) ADATO-3 → IO-3</p> <p>[if CAB04-07 = B₁₀ or D₁₆]: 1 → ISD (6A04) negative sign</p> <p>[+CAB00.CAB01] = ISPO (23B47) sign in M.S.D. [+CAB00.CAB02] = ISPI (23B44) sign in L.S.D. [+CAB04.CAB05] [+CAB04.CAB06]</p> <p>ISPO → CC1 (6A33) illegal digit</p> <p>ISPI → GP3 (29A31) remembers the sign.</p> <p>[if DRO-3 = 0] = DTOO (21A08)</p> <p>DT00 → GP1 (29A33) used to put in O's where number was shifted out of</p> <p>DOWN (20A23) DRO-3 - 1 → DRO-3</p> <p>EDOWN (18A30) EDPTO-3 - 1 → EDPTO-3</p>
---------	--

Data
from CPU
fast memory



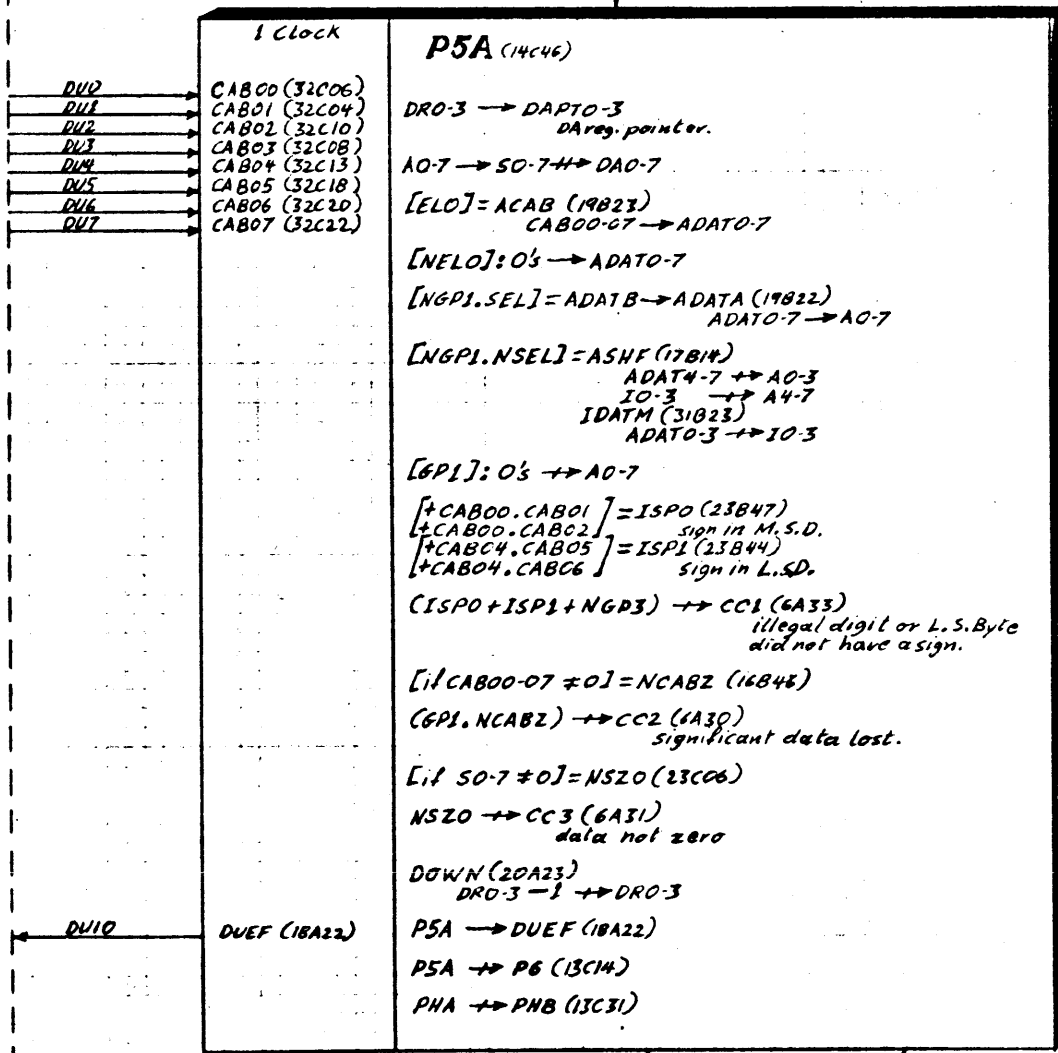
1 Clock	<p>P5 (13C04)</p> <p>DRO-3 → DAPTO-3 DA reg. pointer</p> <p>AO-7 → SO-7 → DA0-7</p> <p>[ELO] = ACAB (19823) CAB00-07 → ADATO-7</p> <p>[NELO]: O's → ADATO-7</p> <p>[NGP1.SEL] = ADATB → ADATA (19822) ADATO-7 → AO-7</p> <p>[NGP1.NSEL] = ASHF (17B14) ADAT4-7 → AO-3 IO-3 → A4-7 IDATM (31823) ADATO-3 → IO-3</p> <p>[GPI]: O's → AO-7</p> <p>[+CAB00.CAB01] = ISPO (23B47) sign in M.S.D. [+CAB00.CAB02] = ISPI (23B44) sign in L.S.D. [+CAB04.CAB05] [+CAB04.CAB06]</p> <p>(ISPO + ISPI) → CC1 (6A33) illegal digit</p> <p>[if CAB00-07 ≠ 0] = NCABZ (4846)</p> <p>(GPI.NCABZ) → CC2 (6A3R) significant data lost.</p>
---------	--

LEFT SHIFT (NGP2)



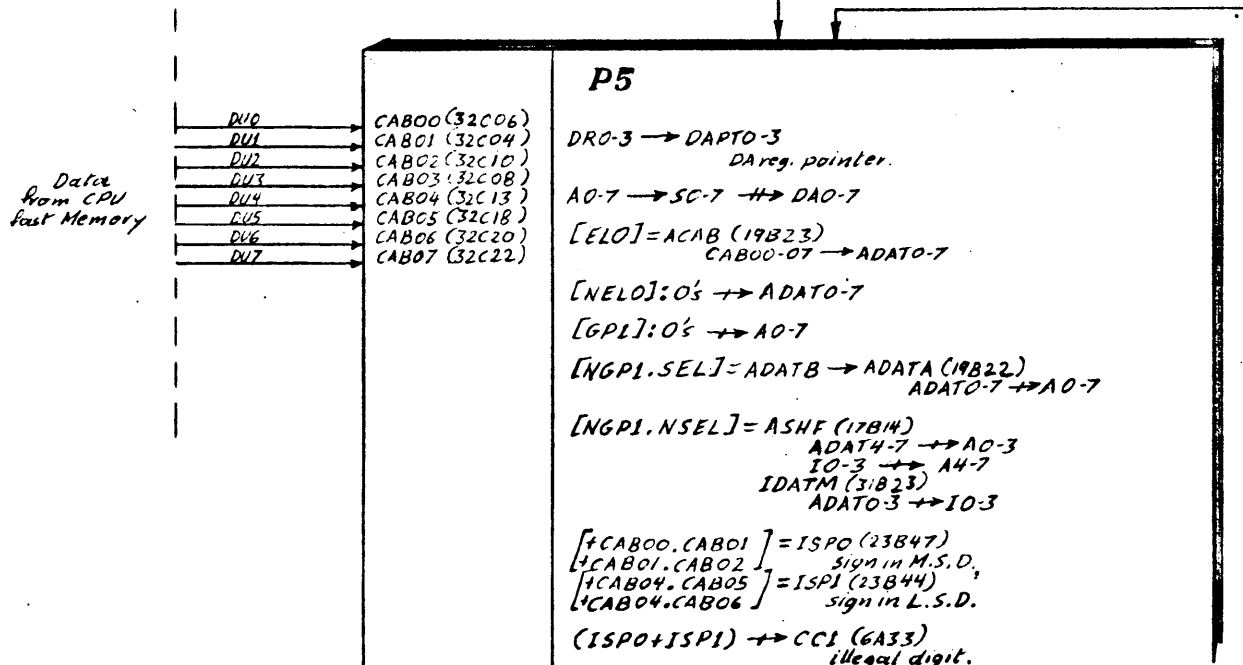
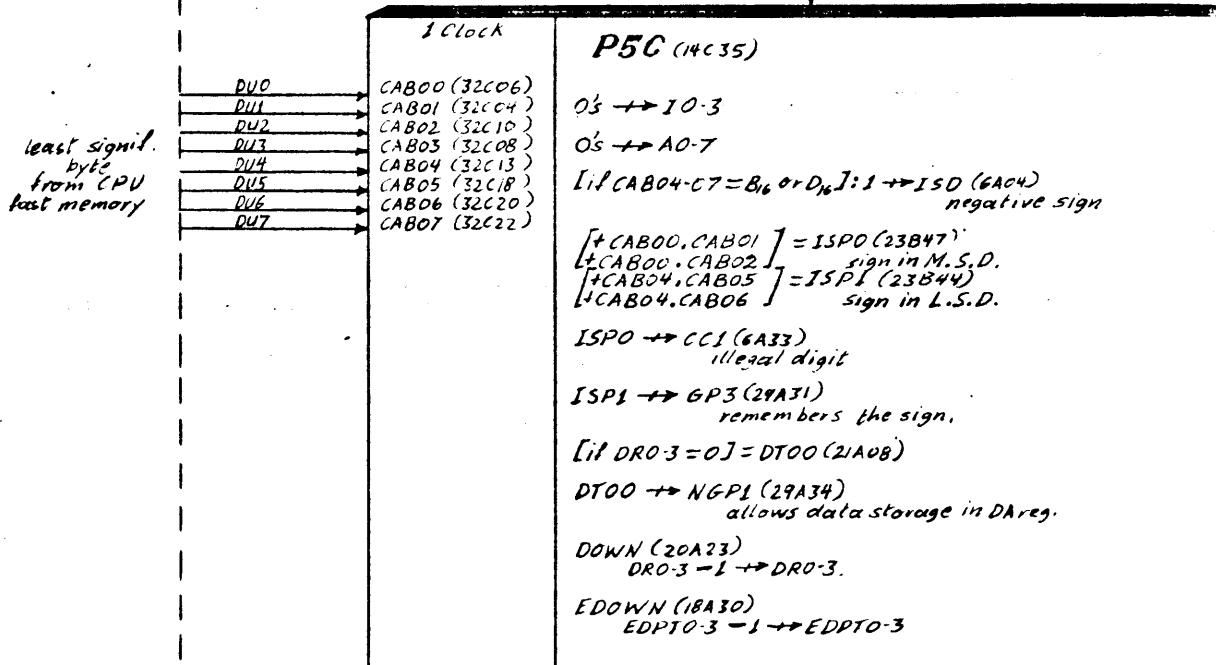
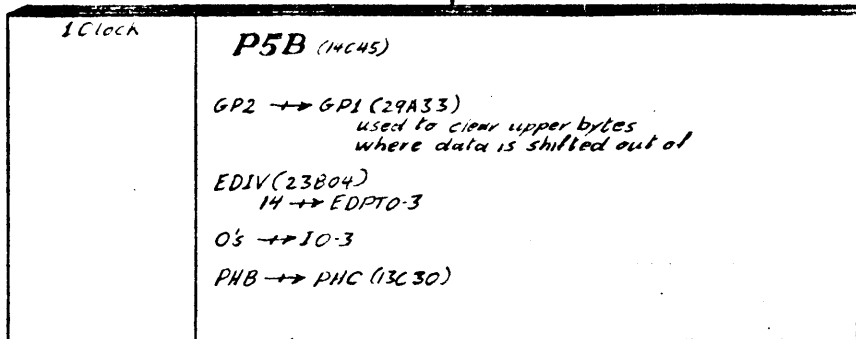
ETOO NETOO

last most signif byte from memory.



P6B

RIGHT SHIFT (GP2)



RIGHT SHIFT

[if SO-7 ≠ 0] = NSZO (23C06)
 NSZO → CC3 (6A31)
 data not zero.

[if DR0-3 = 0] = DT00 (21A06)
 DT00 → NGP1 (29A34)
 allows data storage in DA reg.

[if EDPT0-3 = 0] = ET00 (5B15)
 ET00 → PHA (13C27)

DOWN (20A23)
 DR0-3 - 1 → DR0-3

EDOWN (18A30)
 EDPT0-3 - 1 → EDPT0-3

ET00

NET0C

Last
 most signif
 data byte
 from CPU
 fast Memory.

1 Clock

D10 → CAB00 (32C06)
 D11 → CAB01 (32C04)
 D12 → CAB02 (32C10)
 D13 → CAB03 (32C08)
 D14 → CAB04 (32C13)
 D15 → CAB05 (32C18)
 D16 → CAB06 (32C20)
 D17 → CAB07 (32C22)

P5A (14C46)

DR0-3 → DAPTO-3
 DA reg. pointer

A0-7 → SO-7 → DAO-7

[ELO] = ACAB (19B33)
 CAB00-07 → ADATO-7

[NELO] = 0's → ADATO-7

[GP1] : 0's → A0-7

[NGP1.SEL] = ADATB → ADATA (19B22)
 ADATO-7 → A0-7

[NGP1.NSEL] = ASHF (17B14)
 ADAT4-7 → A0-3
 IO-3 → A4-7
 IDATM (31B23)
 ADAT0-3 → IO-3

[+CAB00.CAB01] = ISPO (23B47)
 sign in M.S.D.
 [+CAB04.CAB05] = ISPI (23B44)
 sign in L.S.D.

(ISPO+ISPI) → CC1 (6A33)
 illegal digit.

[if SO-7 ≠ 0] : 1 → CC3 (6A31)
 data not zero.

DOWN (20A23)
 DR0-3 - 1 → DR0-3

P5A → DUEF (18A22)

P5A → P6 (13C14)

PHA → PHB (13C31)

P6B

DECIMAL SHIFT CONTINUED

1 Clock

P6B (14C36)

DRO-3 → ADPTO-3
DA reg. pointer.

A0-7 → SO-7 → DAO-7

[if SO-7 ≠ 0] = NSZO (23C06)

NSZO → CC3 (6A31)
data not zero

Right shift only: [if IO-3 ≠ 0] = NIZERO (25B46)
(GP2, NIZERO) → CC3 (6A31)
data not zero.

IO-3 → A4-7

CC1 → NCC2 (6A29)

DOWN (20A23)
DRO-3 - 1 → DRO-3

PHB → PHC (13C30)

1 Clock

P6C (14C01)

Right shift only: [GP2]: DRO-3 → ADPTO-3
DA reg. pointer.

A0-7 → SO-7 → DAO-7

ACC (23B45)

CC1 → A0 (20B27)

CC2 → A1 (20B31)

(CC3, NISD) → A2 (20B19)

(CC3, ISD) → A3 (20B23)

(CC1, TMASK) → A4 (21B27)

(CC1, NTMASK) → A5 (21B31)

NCC1 → A6 (21B19)

NCC2 → A7 (21B23)

[NISD]: C₁₆ → IO-3

[ISD]: D₁₆ → IO-3

DRPRE (18A23)
14 → DRO-3

EDIV (23B04)
14 → EDPTO-3

P6C → PHA (13C27)

1 Clock

P6. PHA
(13C14) (13C27)

A0-7 → SO-7

DOUT (23B03)
SO-7 → DUO-7

DUEF (18A22)

ADIL (18B22)
IO-3 → A4-7
sign.

ADA (19B30)
DAO-7 → ADATO-7

ADATC → ADATA (19B22)
ADATO-3 → AO-3

DOWN (20A23)
DRO-3 - 1 → DRO-3

EDOWN (18A30)
EDPTO-3 - 1 → EDPTO-3

(P6. PHA) → PT (13C06)

Condition Code @ abort info.

DU0 → 50 (30C30)

DUI → 51 (30C31)

DUI → 52 (30C33)

DUI → 53 (30C34)

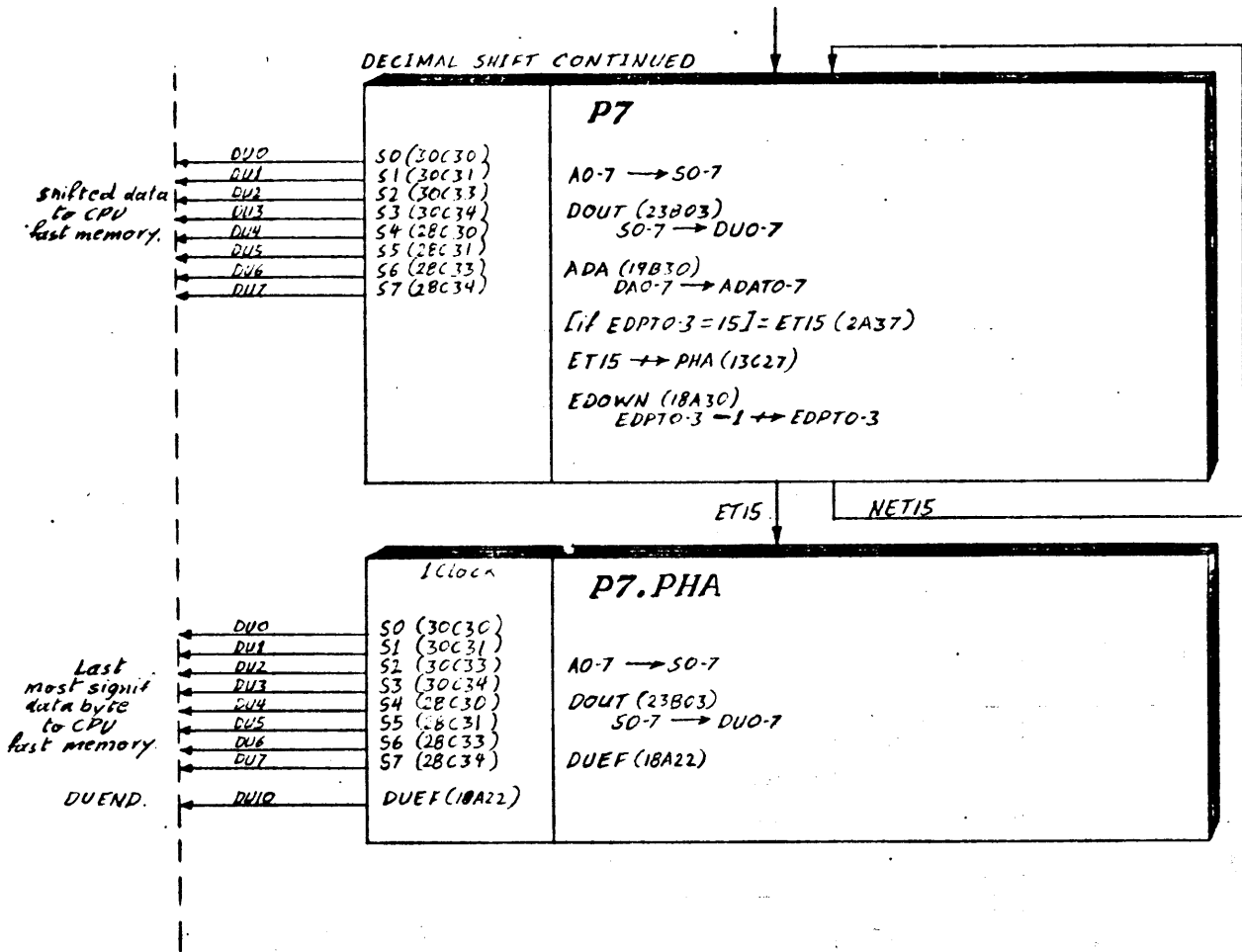
DUI → 54 (28C30)

DUI → 55 (28C31)

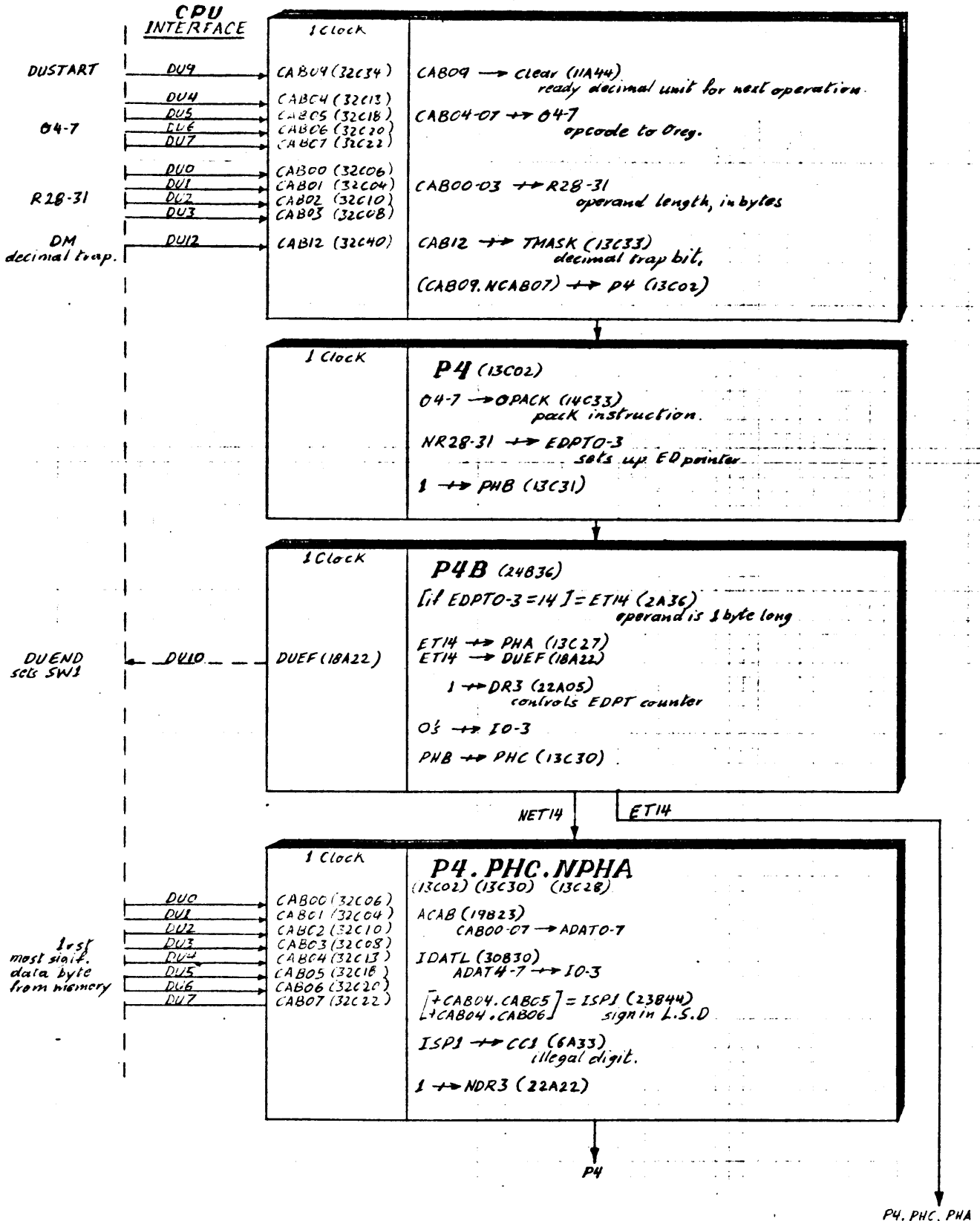
DUI → 56 (28C33)

DUI → 57 (28C34)

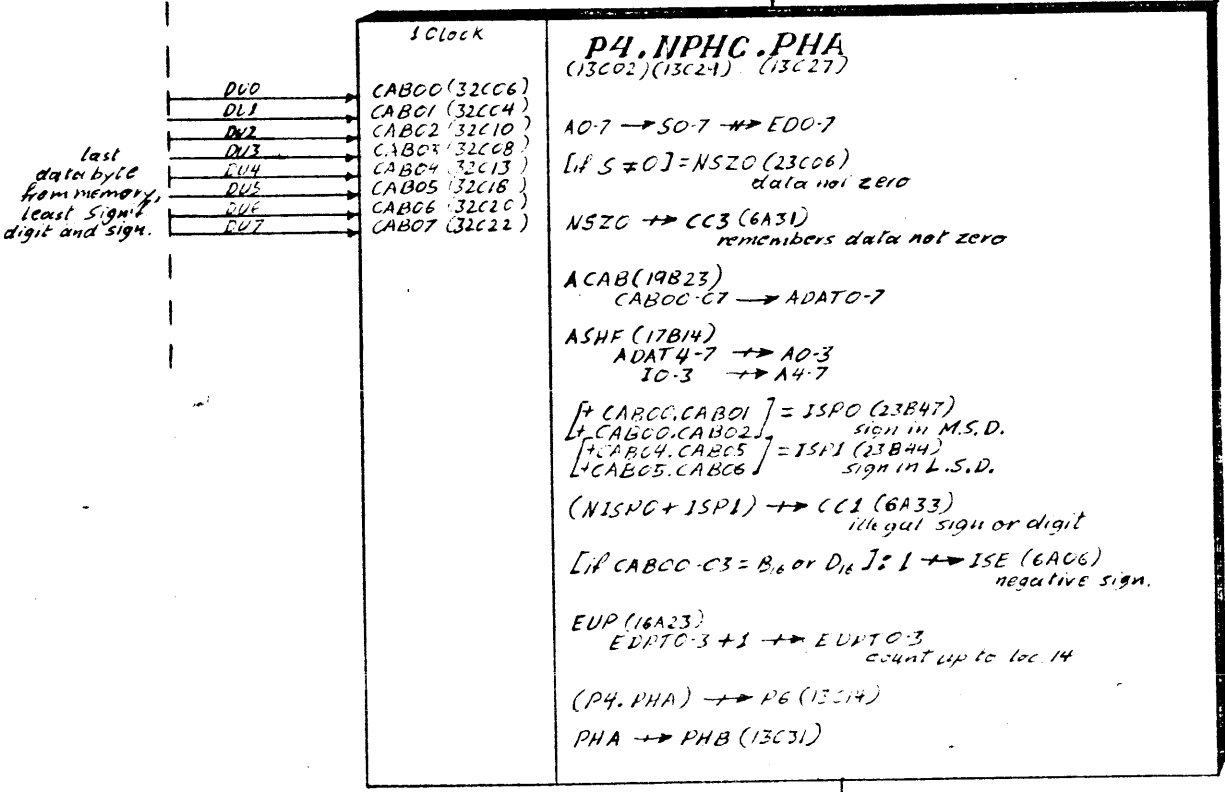
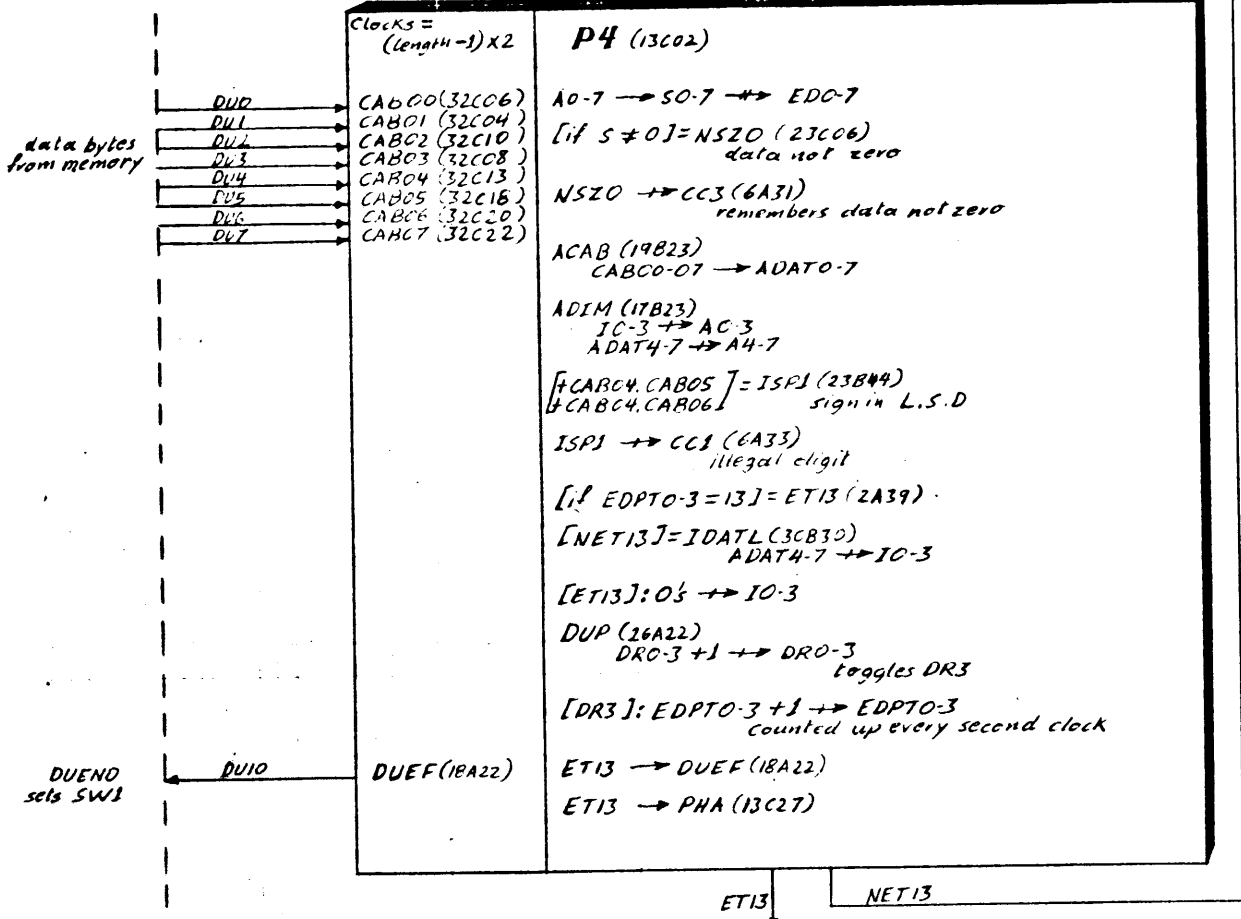
DUEND → DU10 → DUEF (18A22)



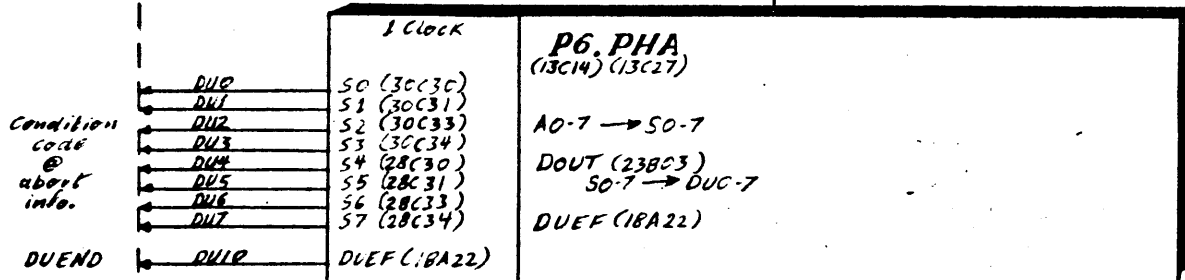
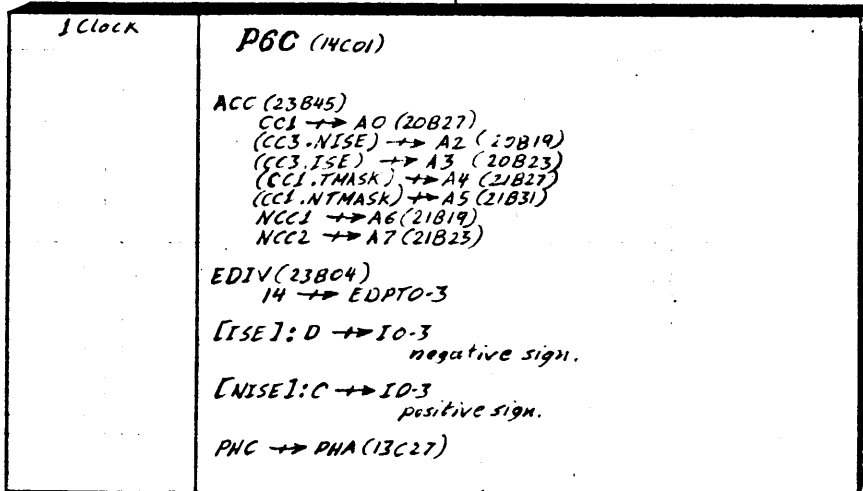
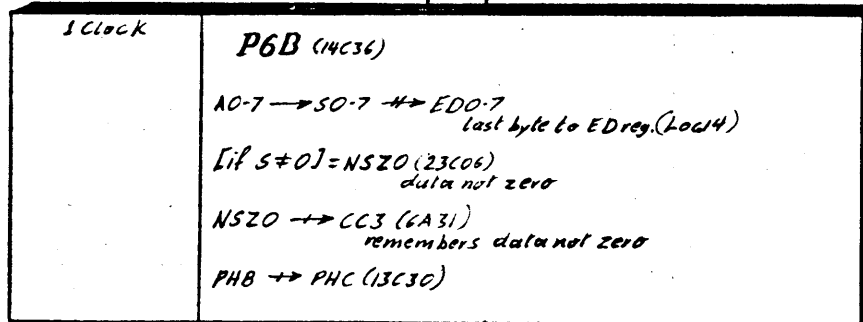
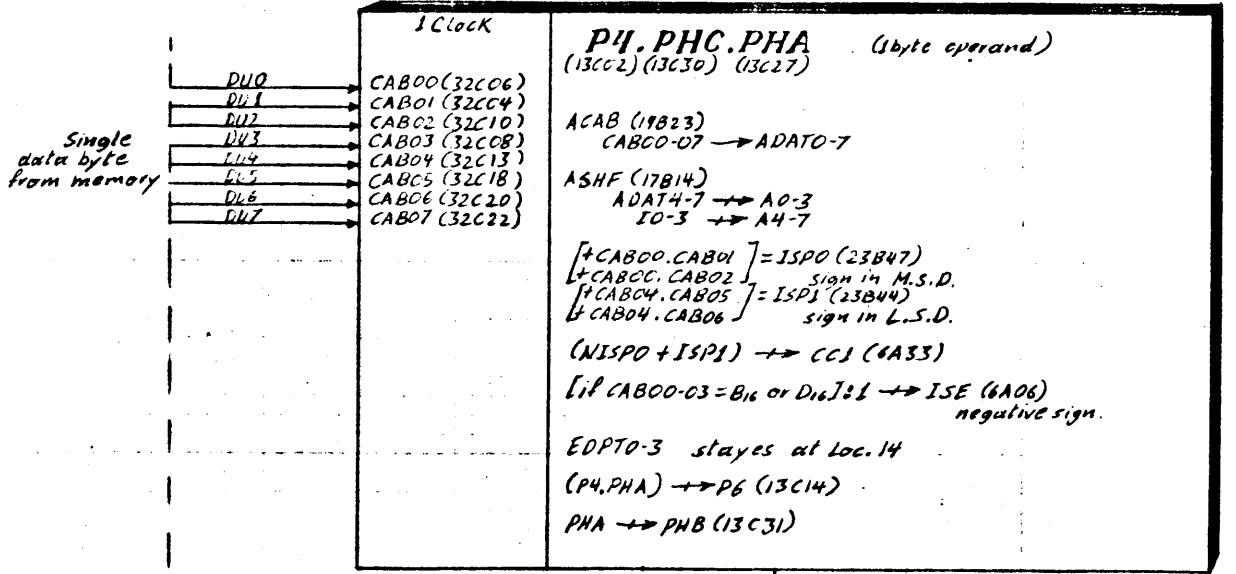
PACK DECIMAL DIGITS (76)



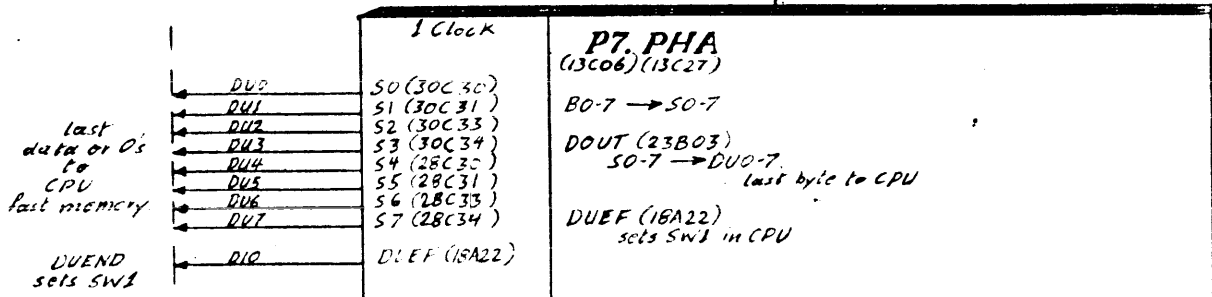
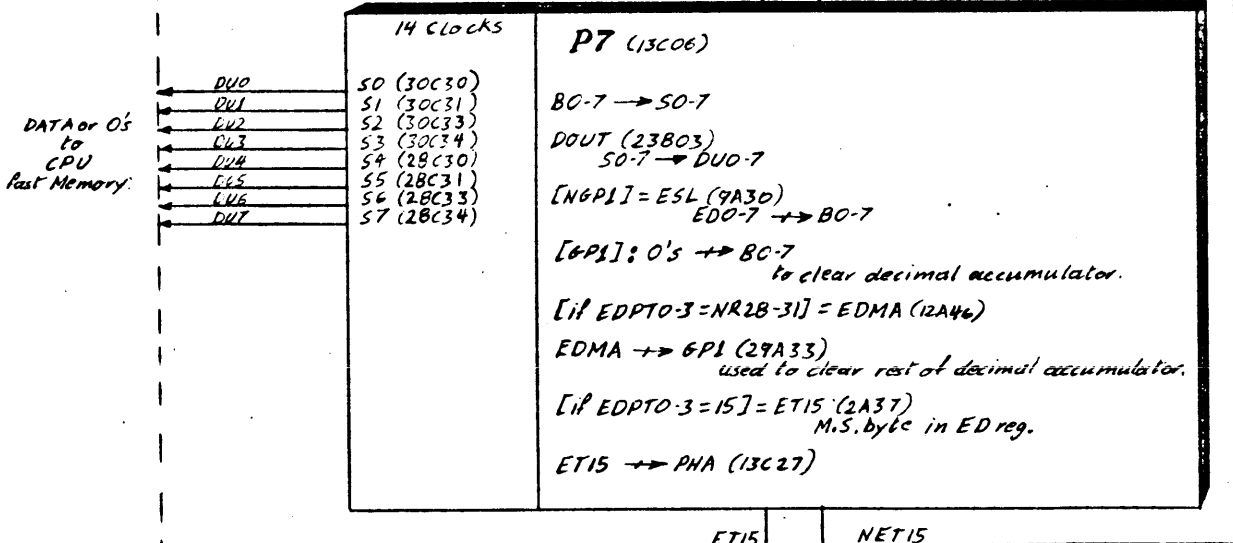
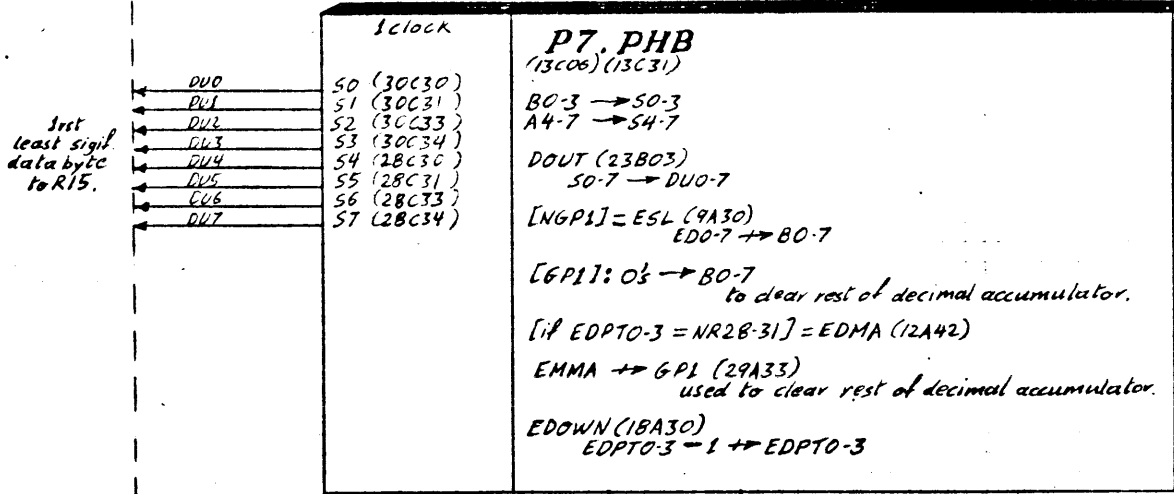
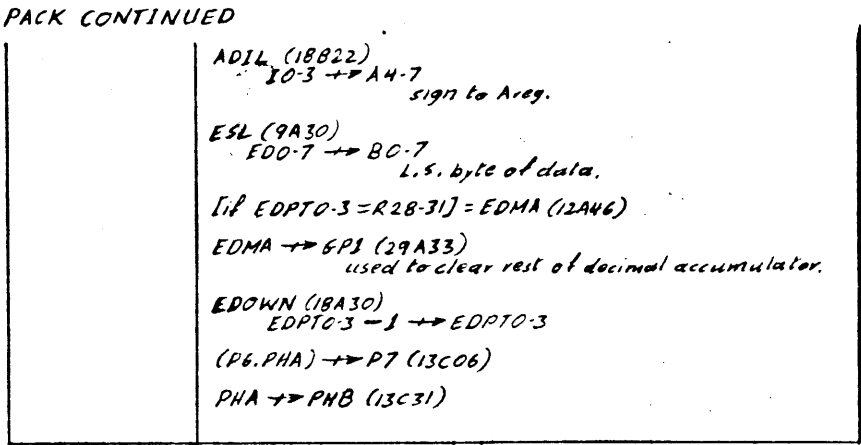
PACK CONTINUED



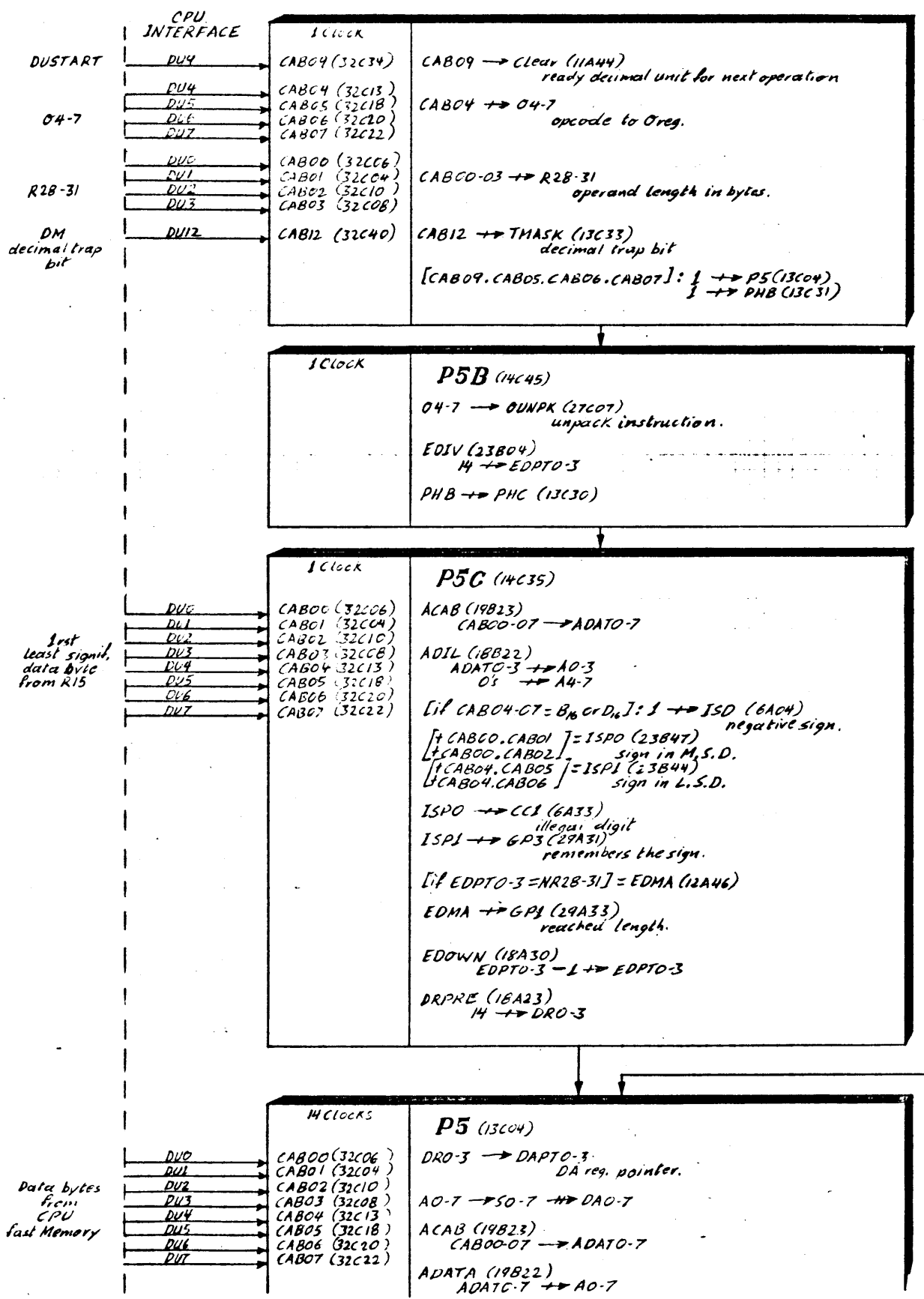
PACK CONTINUED



PACK CONTINUED



UNPACK DECIMAL DIGITS (77)



UNPACK CONTINUED

$[+CAB00.CAB01] = ISPO (23B47)$
 $[+CAB00.CAB02] = ISPI (23B44)$ sign in M.S.D
 $[+CAB04.CAB05] = ISPI (23B44)$ sign in L.S.D
 $[+CAB04.CAB06] = ISPI (23B44)$ sign in L.S.D
 $(ISPO + ISPI) \rightarrow CC1 (6A33)$ illegal digit
 $[if CAB00-07 \neq 0] = NCABZ (16B46)$ data not zero
 $(NCABZ . 6PI) \rightarrow CC2 (6A30)$ significant data lost
 $[if EDPT0-3 = NR2E-3I] = EDMA (12A46)$
 $EDMA \rightarrow GPI (29A33)$
 $[if EDPT0-3 = 0] = ETCO (5B15)$
 $ETCO \rightarrow PHA (13C27)$
 $EDOWN (18A30)$
 $EDPT0-3 - 1 \rightarrow EDPT0-3$
 $DOWN (20A23)$
 $DRO-3 - 1 \rightarrow DRO-3$

ETCO NETOO

last data byte from CPU fast Memory

D10 → CAB00 (32C06)
 D11 → CAB01 (32C04)
 D12 → CAB02 (32C10)
 D13 → CAB03 (32C08)
 D14 → CAB04 (32C13)
 D15 → CAB05 (32C18)
 D16 → CAB06 (32C20)
 D17 → CAB07 (32C22)

1 CLOCK

P5A (14C46)

$DRO-3 \rightarrow DAPTO-3$ DA reg. pointer
 $AO-7 \rightarrow SO-7 \rightarrow DA0-7$
 $ACAB (19B23)$
 $CAB00-07 \rightarrow ADATO-7$
 $ADATA (19B22)$
 $ADATO-7 \rightarrow AO-7$
 $[+CAB00.CAB01] = ISPO (23B47)$
 $[+CAB00.CAB02] = ISPI (23B44)$ sign in M.S.D
 $[+CAB04.CAB05] = ISPI (23B44)$ sign in L.S.D
 $[+CAB04.CAB06] = ISPI (23B44)$ sign in L.S.D
 $(ISPO + ISPI) \rightarrow CC1 (6A33)$ illegal digit
 $[NEP3]: 1 \rightarrow CC1 (6A33)$ illegal sign
 $[if CAB00-07 \neq 0] = NCABZ (16B46)$
 $(NCABZ . 6PI) \rightarrow CC2 (6A30)$ significant data lost
 $DOWN (20A23)$
 $DRO-3 - 1 \rightarrow DRO-3$
 $P5A \rightarrow DUEF (18A22)$ sets SW1 in CPU
 $P5A \rightarrow PE (13C14)$
 $PHA \rightarrow PHB (13C31)$

DUEF (16A22)

DUEND sets SW1

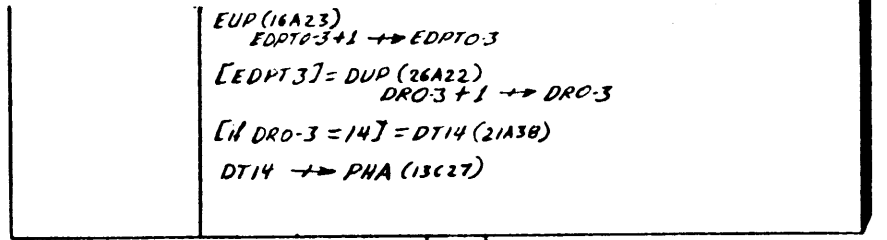
DUEF ← D10

1 CLOCK

P6B (14C36)

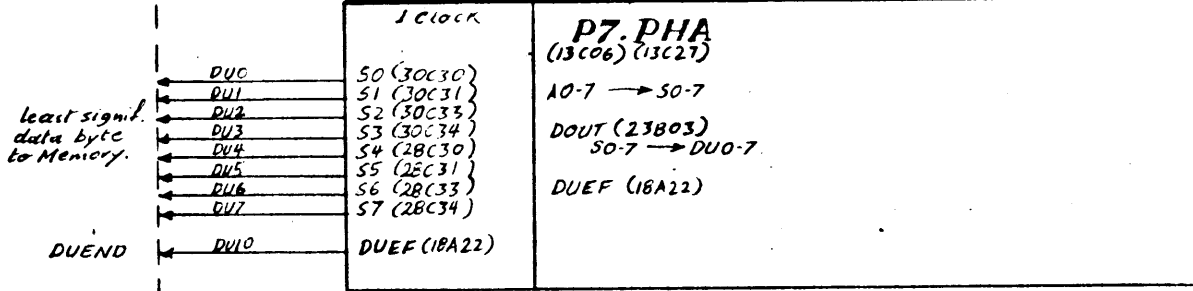
$DRO-3 \rightarrow DAPTO-3$ DA reg. pointer
 $AO-7 \rightarrow SO-7 \rightarrow DA0-7$
 $[CC1]: 1 \rightarrow NCC2 (6A29)$
 $DRX (24B45)$
 $NR2B-3I \rightarrow DRO-3$
 $O's \rightarrow EDPT0-3$
 $FHS \rightarrow PHC (13C30)$

UNPACK CONTINUED



DT14

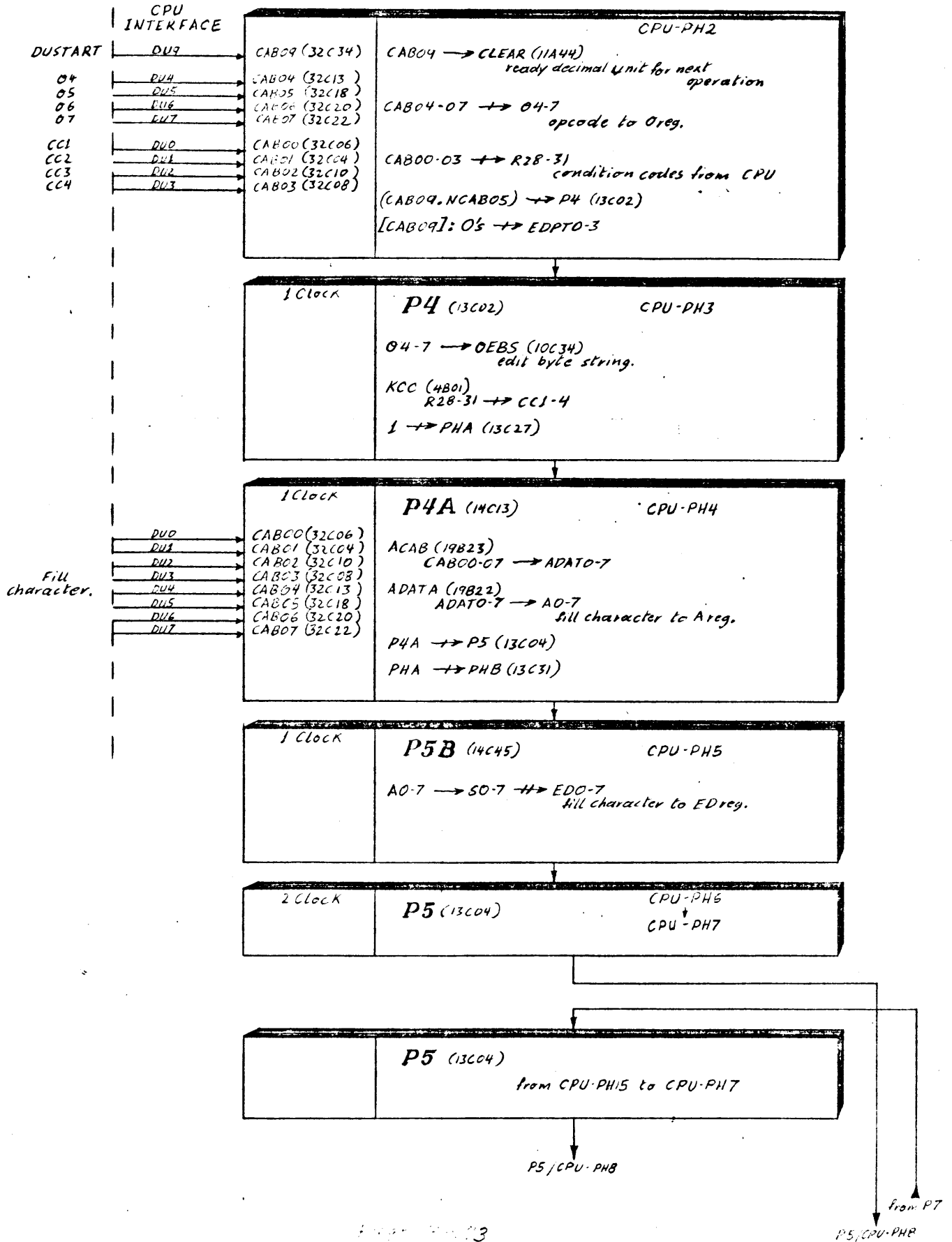
NDT14



least signif.
data byte
to Memory.

DUEND

EDIT BYTE STRING (63)

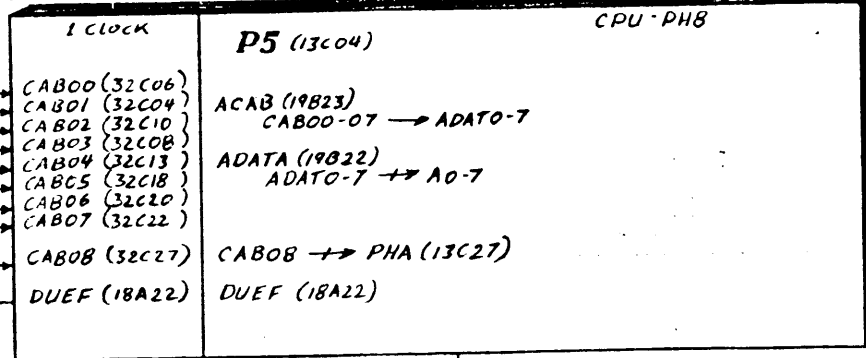


EDIT BYTE STRING CONTINUED

CPU-PH8

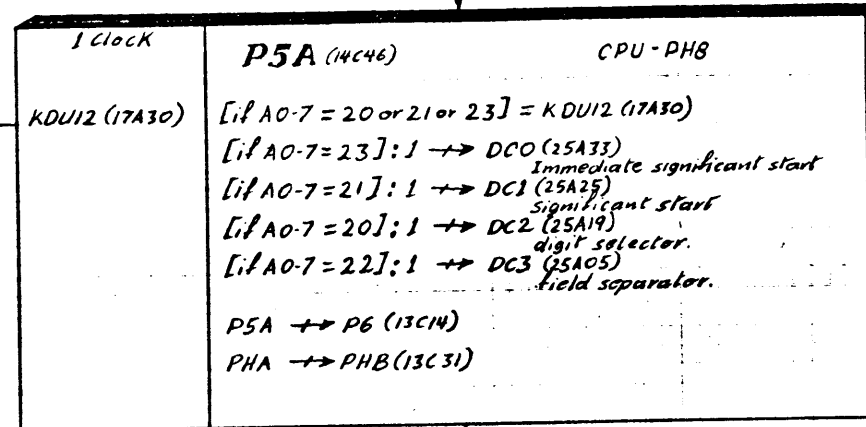
Editing Pattern

DUCLOCK
DUEND sets DRQ



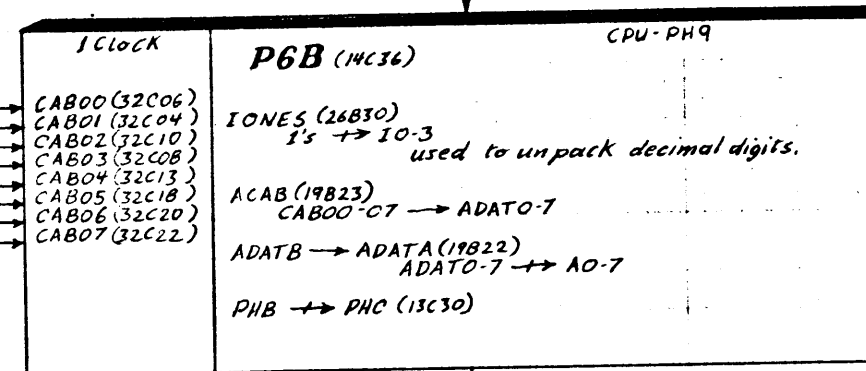
CPU-PH8

sets SW4

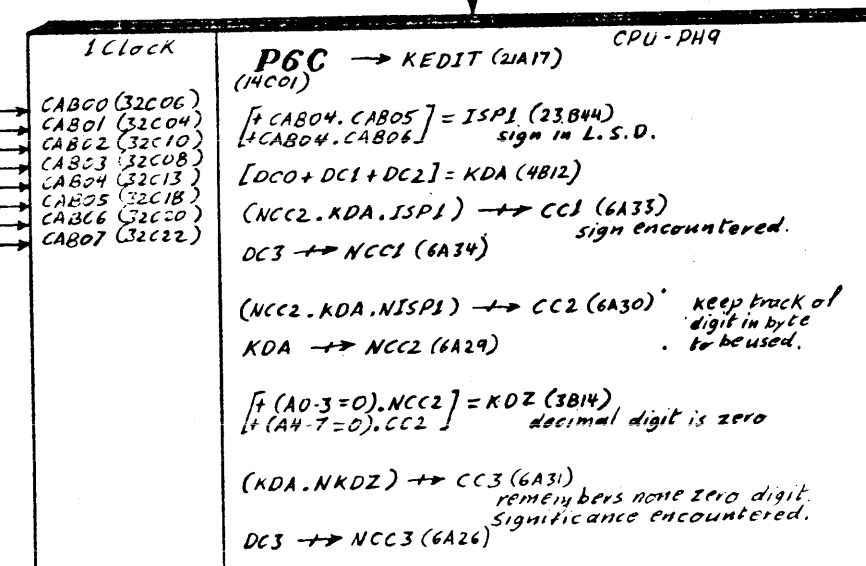


CPU-PH9

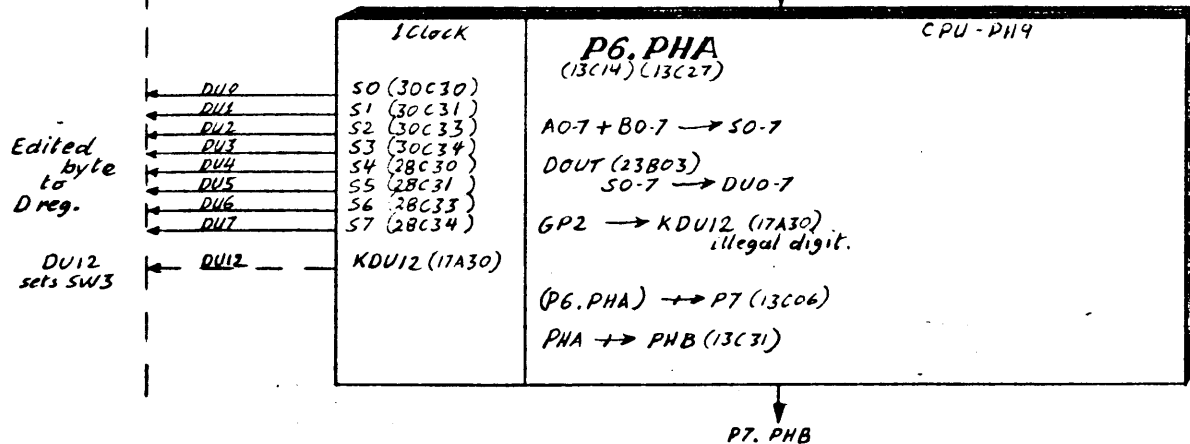
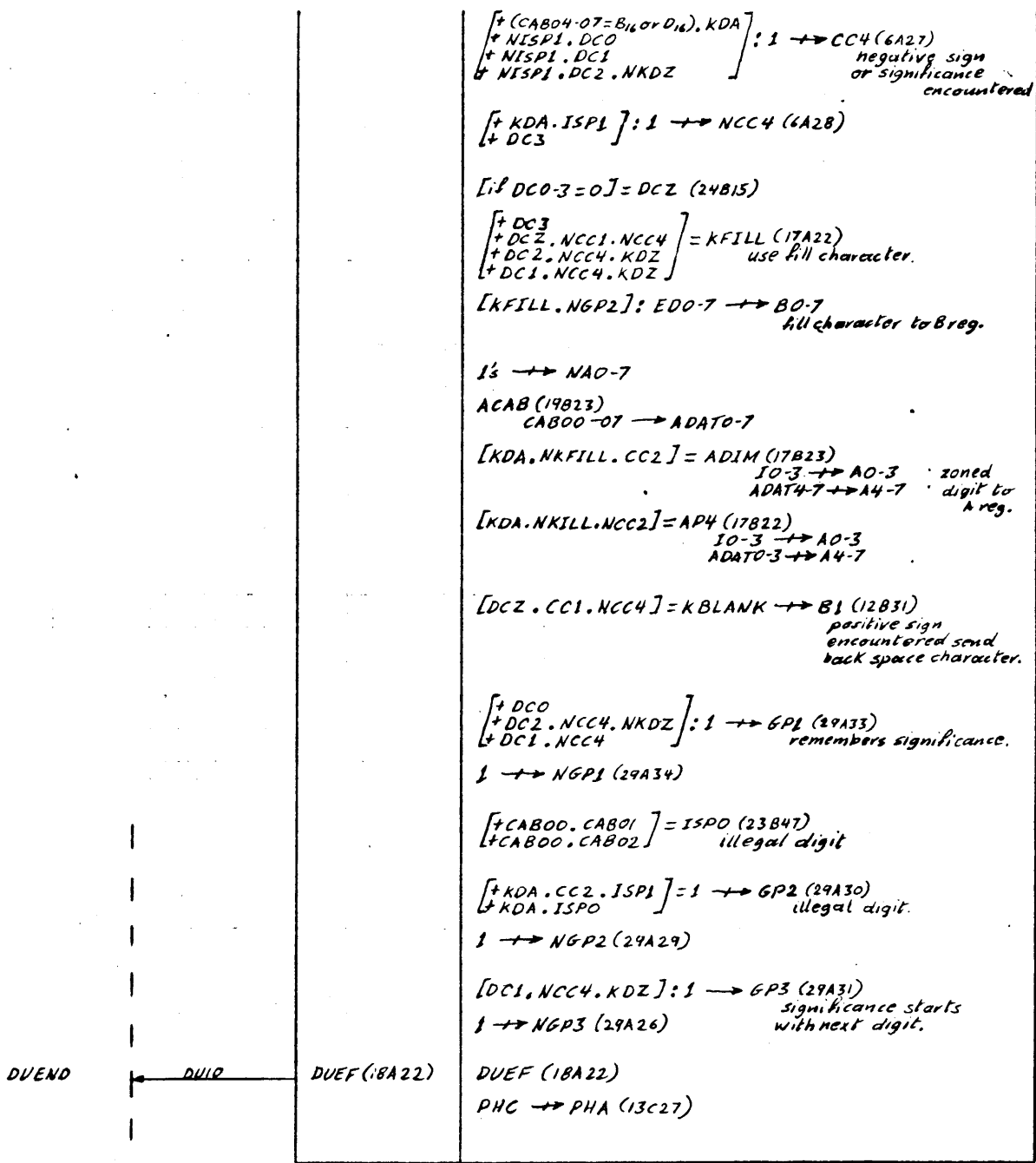
Packed decimal digit.



CPU-PH9

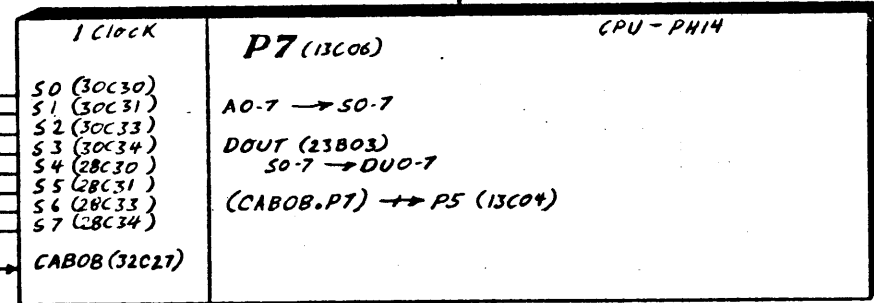
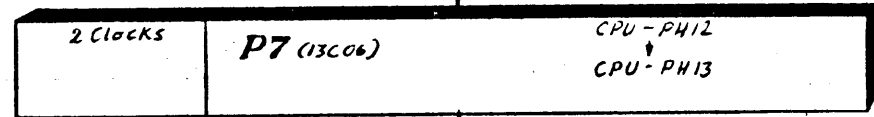
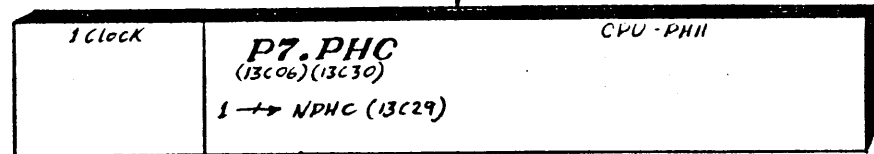
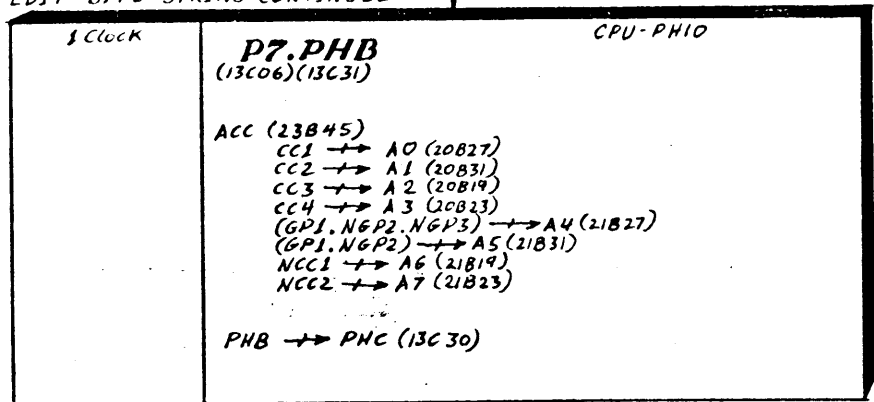


EDIT BYTE STRING CONTINUED



EDIT BYTE STRING CONTINUED

P5



Conditions
 @
 condition
 code
 information

DUCLOCK

DU0
 DU1
 DU2
 DU3
 DU4
 DU5
 DU6
 DU7
 DUB

MODULE CONNECTION CHART (SIOP)

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	DT14	HT15	BT22	FT24	IT26	LT13	XT10	BT10	XT10	AT24	FT37	IT13	BT16	FT38	FT38	FT38	FT39	AT16	BT10	LT20	IT16	AT11	IT25	LT21	XT10	XT10	LT13	LT13	FT37	BT18	FT15	IT15
B	AT16	IT25	IT24	BT22	IT25	LT21	FT26	BT16	IT16	FT39	FT39	FT27	FT39	FT26	FT39	XT10	LT13	IT16	IT15	IT11	IT11	IT11	BT18	FT37	XT10	XT10	IT15	FT37	IT16	FT37	LT13	IT25
C	FT18	FT18	LT13	FT27	XT10		IT15	IT25	BT25	XT10	FT26	BT10	BT25	IT16	IT25	FT26	BT10	BT10	LT21	BT15	FT26	BT18	IT18	LT13	XT10		LT29	DT14	HT15	BT16		BT22
D	BT11	FT18	FT18	FT18	FT18		FT38	FT38	FT38	FT38	FT26	FT38	AT11	FT38	AT11	FT26	FT38	AT11	FT38	AT11	FT26	AT12	FT37	FT37	LT21	BT22	XT10	DT11	HT15	BT15	AT75	BT22
E	GT11	FT18	FT18	BT11	FT18	FT18	FT18	FT18	FT18	XT10	FT38	AT11	FT37	AT11	FT37	AT11	BT16	XT10	AT10	BT18	BT25	AT12	LT21	AT11	LT21	XT10		FT24	FT37	LT20	BT10	LT2
F		BT18	BT22	BT16	XT10	BT11	BT15	FT18	FT18	GT11	BT22	BT10	FT22	BT24	IT16	LT65	IT15	IT25	BT18	IT16	IT25	BT16	AT13	LT64	LT26	XT10	IT16	IT25	IT11	FT66		
SIOP																																
A	AT56	DT26	AT60	LT89	AT57	LT90	AT83			LT94	LT95	LT26	BT16	AT60	LT71	AT60	FT82	AT11	FT79	AT11	FT79	AT11	FT79	FT79	IT31	BT12	BT31	BT31	BT10	FT66	FT66	FT43
MS																																

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SIOP SWITCHES (LT26 Loc. 8F)

ADDRESS

- S1-1 = Bit 21 = IOPAO
- S2-1 = Bit 22 = IOPAI
- S3-1 = Bit 23 = IOPAZ

AIOP = S1-2 up

Buss Shared = S2-2 up

LASTONE = S4-1 up.

MS SWITCHES

ADDRESS (LT26 Loc. 21A)

- S1-1 = Bit 26 → A10
- S2-1 = Bit 25 → A09
- S3-1 = Bit 24 → A08
- S4-1 = Bit 23 → A07
- S1-2 = Bit 22 → A06
- S2-2 = Bit 21 → A05
- S3-2 = Bit 20 → A04
- S4-2 = Bit 19 → A03

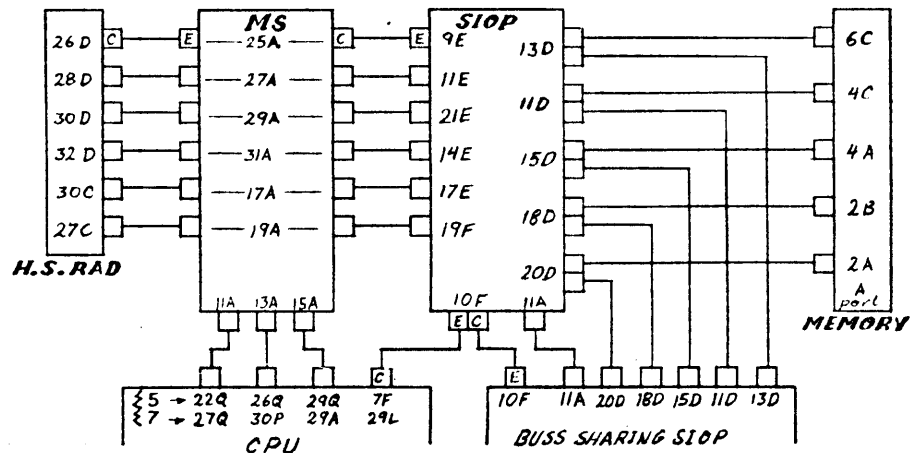
ON/OFF LINE (LT94 Loc. 23A)

- S1 up = On Line
- S1 down = Off Line

Note: S1 Loc. 22A must be up.

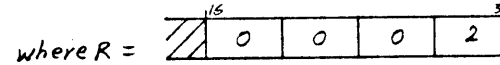
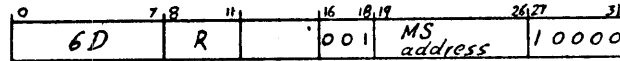
OPTION

- BS = Buss Sharing.
- ABS = Buss Sharing AIOP only.

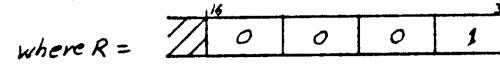
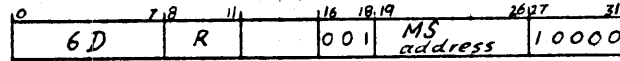


Single Phasing The SIOP

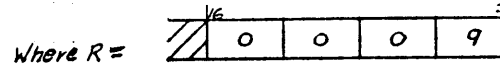
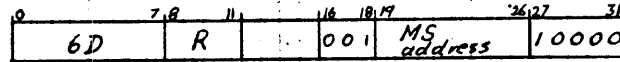
Set SIOP to single phase mode



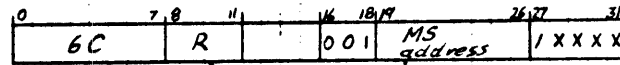
Run TI delay line once



Run TM delay line twice (1 TM phase)



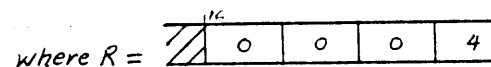
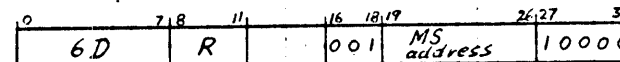
Read SIOP signals



Group 16 -> A16

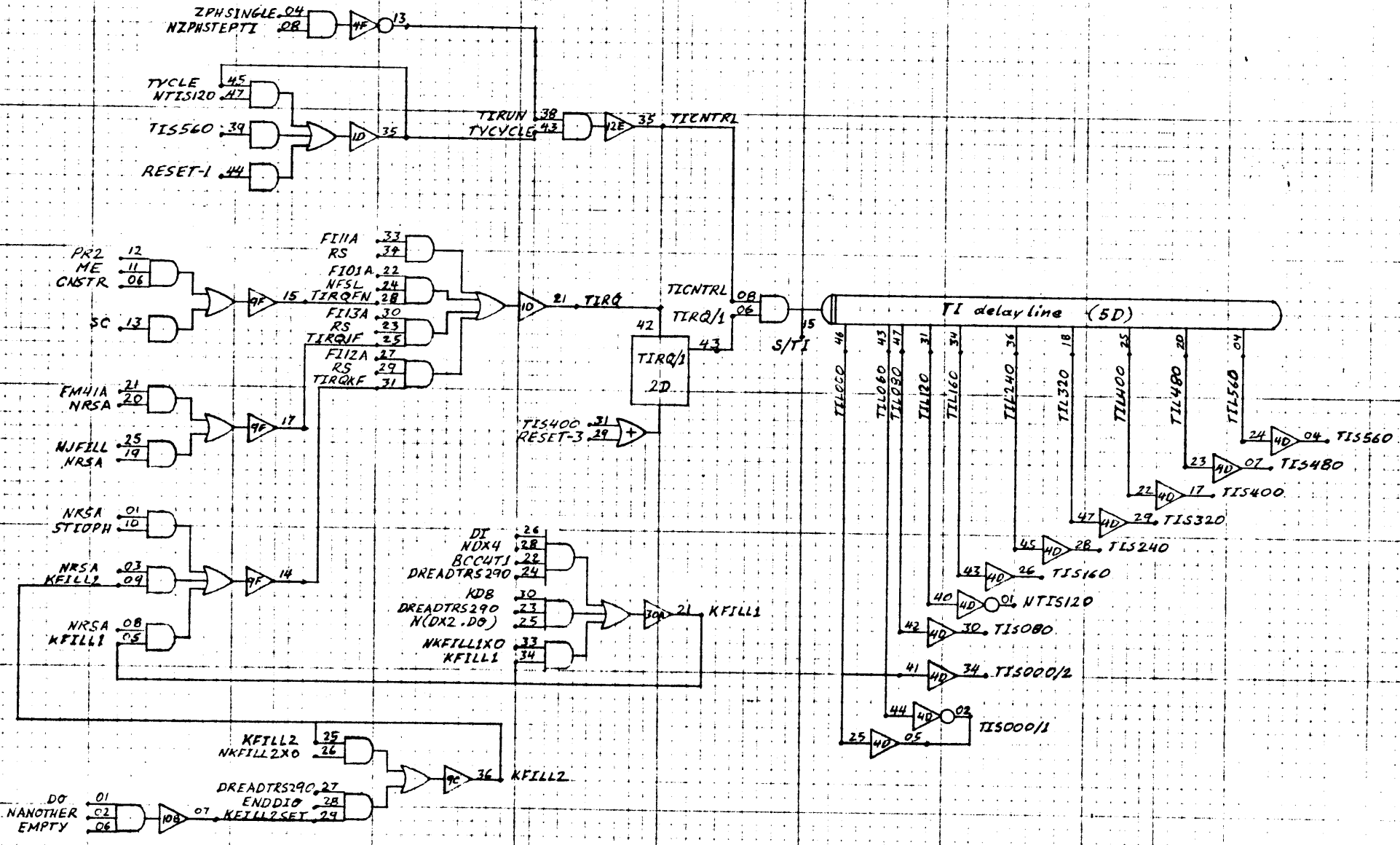
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Group 1	F101A	F101B	F101A	F101B	F111A	F111B	F112A	F112B	F113A	F113B	F114A	F114B	LAST	MATCH	ZBC1	ZBC2
Group 2	F11A	F11B	F112A	F112B	F113A	F113B	F121A	F121B	F122A	F122B	F124A	F124B	END1	NSERVICE1	CRD	CUT
Group 3	F131A	F131B	F132A	F132B	F133A	F133B	F134A	F134B	F141A	F141B	MWA	MWB	MWC	MWD		S31
Group 4	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30
Group 5	BC00	BC01	BC02	BC03	BC04	BC05	BC06	BC07	BC08	BC09	BC10	BC11	BC12	BC13	BC14	BC15
Group 6	CNSTR	PK1	FS	FSL	AVO	RS	RSA	SC	IC	IR	FNCF	MPE	MPR	MRQ	MRQ1	MRQ2
Group 7	STIL	STDE	STME	STMAE	STIOPME	STIOPCE	STIOPH	STIOPB1	STCE1	STLC1	STZBC1	END1	END2	END3	END10	FECLEAR
Group 8	RK0	RK1	RK2	RK3	IA1	IA2	IA3	OA1	OA2	OA3	LR1	LR2	LR3	SWRITE	SREAD	DREAD
Group 9	RAB	RBB	KCB	RDB	KAA	KAB	KAC	KAD	SAA	SAB	SAC	SAD	KAB	KBB	KCB	KDB
Group A	WBA	WBB	WBC	WBD	JAB	JBB	JCB	JDB	NANOTHER			AIOP	PRQA	PRQB	MEMCYCA/1	MEMCYCB/1
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Return SIOP to normal mode (RESET)

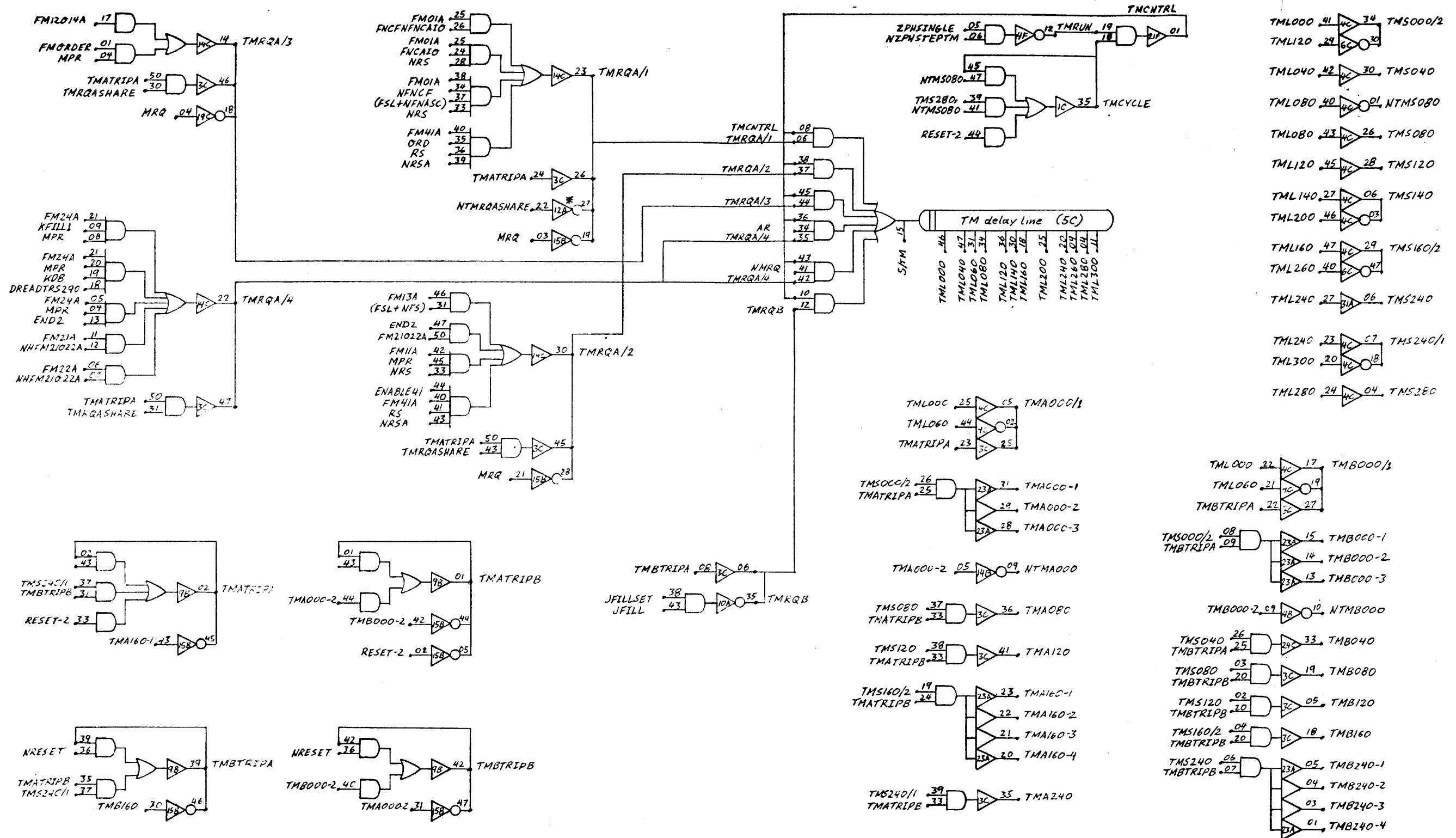


TI Delay line (SIOP)

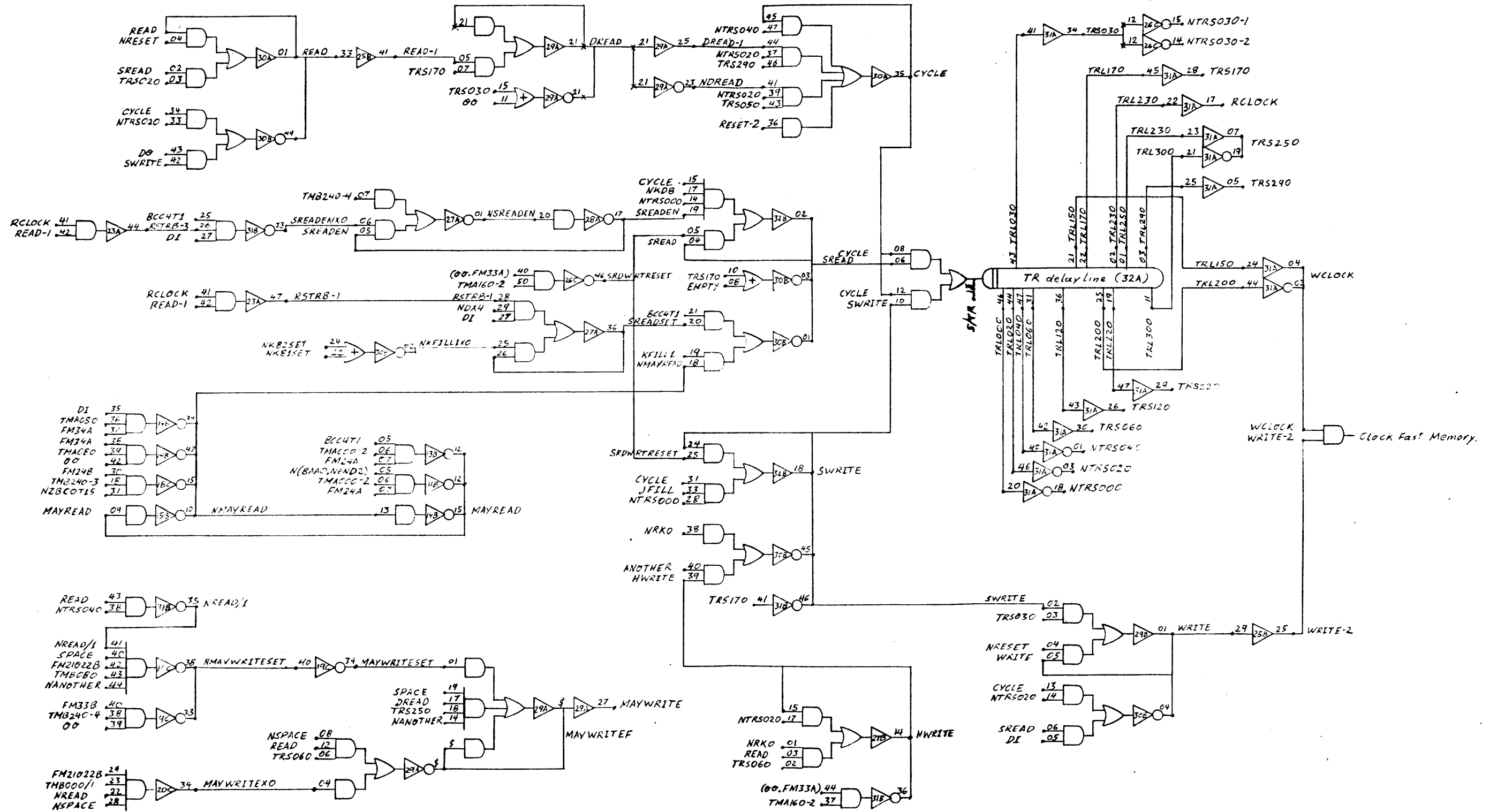
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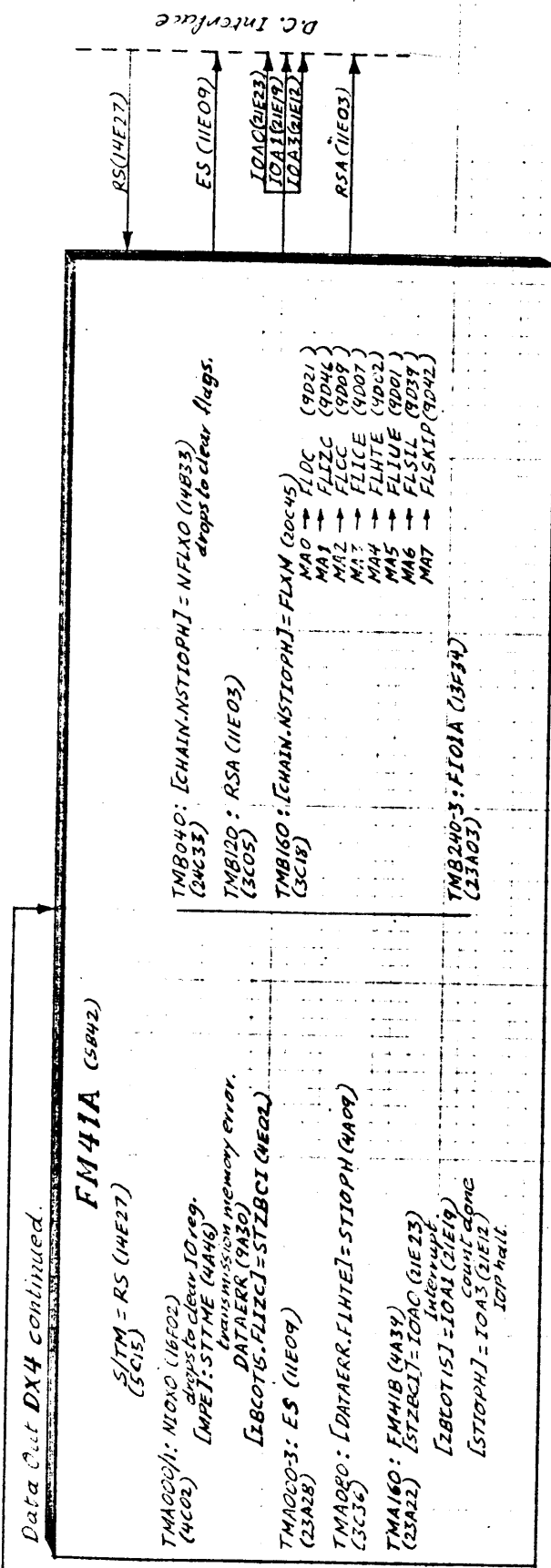


TM Delay Line (STOP)



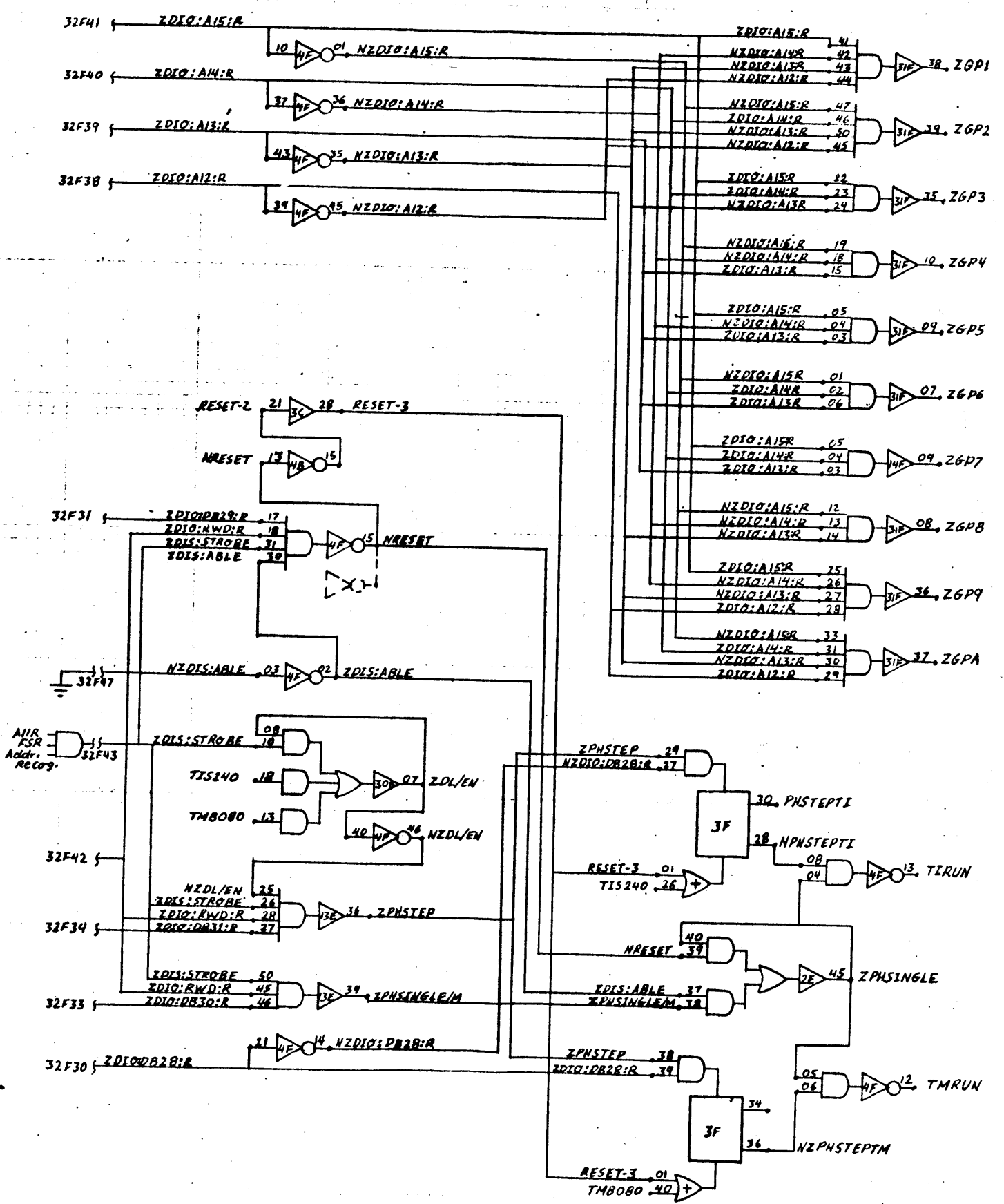
Fast Memory (TR) Delay Line. (SIOP)



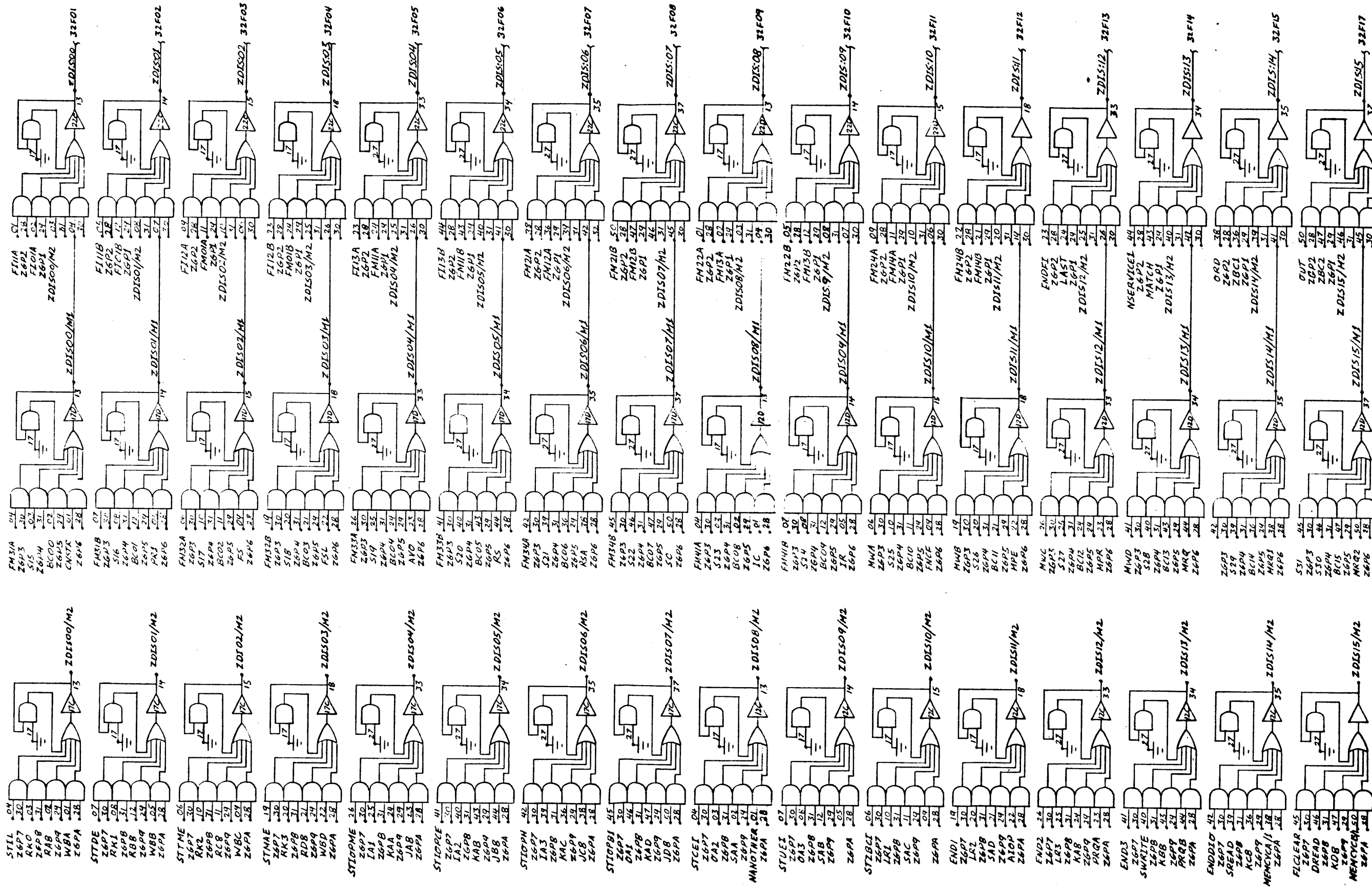


Data Out DX4 continued.

Display Control Logic (SIOP)

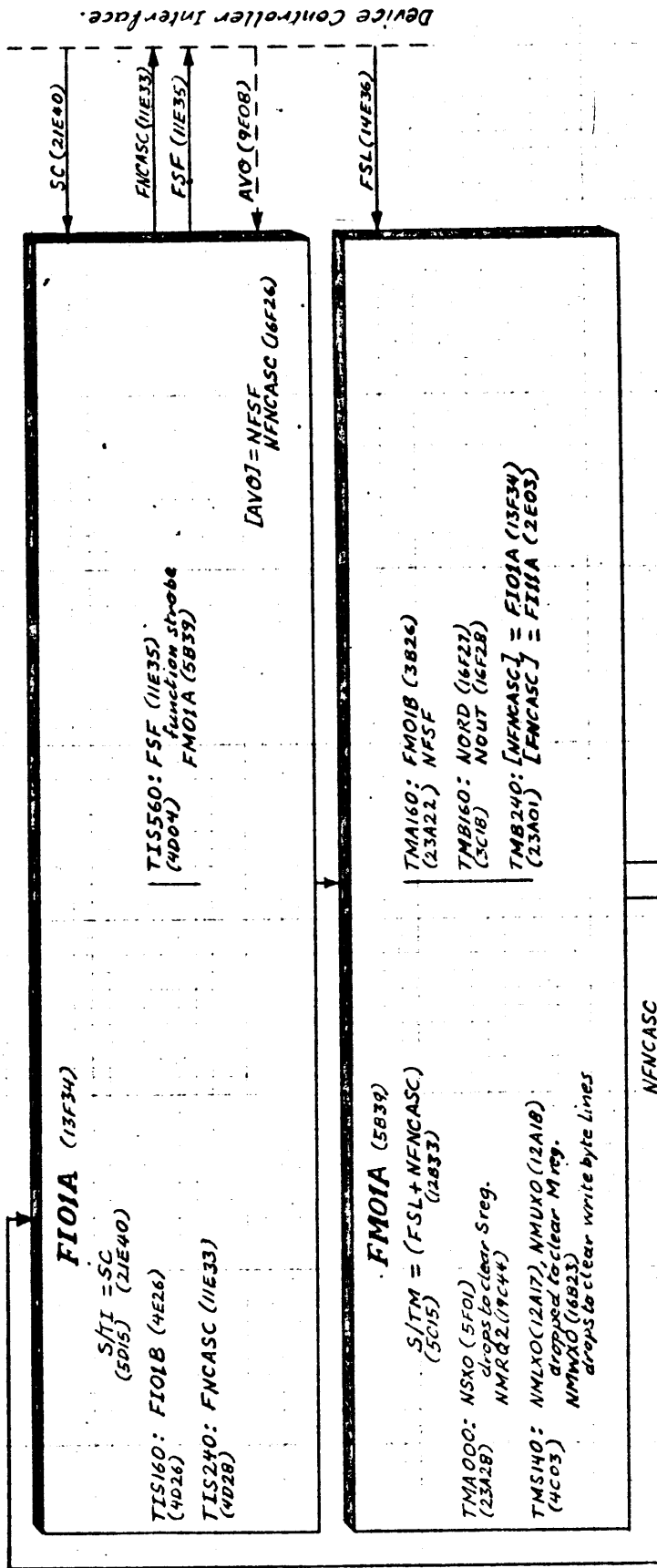


Display Logic (STOP)



SERVICE CALL

Service Connection (SIOP)



ORDER IN (SIOP)

FIOIA (13F34)
FMOIA (5839) } SEE SERVICE CONNECTION

FIJIA (2E03)

S/TI = RS (14E27)
 (5D15)

TIS000/1: NIOXO (16F02)
 (4D02) drops to clear IO reg.
 [IX.F6A10+F6H10.MYNUM]=ED (21E33)

TIS160: FI11B (4E27)
 (4D26) SERVICEI (13F27)
 NFGASC (16F26)
 [ED]=ED (21E33)
 [DOR]=ORD (9F36)
 [LORD,NGOUT]=OI (4E46)
 NUXO (9C01)
 drops to clear J reg.
 IOXD (18F46)
 DAOR-4K to IOAO-4

FM4IA (5842)

S/JM = RS (14E27)
 (3C15)

TMA000/1: NIOXO (16F02)
 (4C02) drops to clear IO reg.

TMA000/3: ES (11E09)
 (23A28)

TMA080: [DATAERR.FLHTE]=STIOPH (4A09)
 (3C35)

TIS240: JAXIO (9C34)
 (4D28) IOAO-4 to JO-4

TIS320: [IOAO]=STIDE (4A27)
 (4D29) DATAERR (9A30)
 [IOA1]=STIL (4A26)

TIS400: [IOA2]=CM (16C47)
 (4D17)

TIS480: [ED]=RSA (11E03)
 (4D07) NSERVICEI (9F32)

TIS560: [STIL.NFLSIL.FLHTE]=STIOPH (4A09)
 (4D04) FM4IA (5842)

TMA160: [FLICE-JA3]=IOAO (21E23)
 (23A20) STCEI (4A01)
 [FLICE.(J4+STIOPH)]=IOAO (21E23)
 [FLCC]=IOA2 (21E15) STUEI (20A47)
 [STIOPH]=IOA3 (21E12)

TMA240: [F-JA3.NFLCC]
 (3C35) [F-STIOPH] = NSTIOPBI (13F35)
 [F-J4] not IOP busy.

TMB120: RSA (11E03)
 (3C05)

TMB240: FIOIA (13F34)
 (23A0U)

Order:

DAOR = data transition error
 DA1R = incorrect length
 DA2R = chaining modifier bit
 DA3R = channel end
 DA4R = unusual end

Terminal Order:

IOAO = interrupt
 IOA2 = command chain
 IOA3 = IOP error

Device Controller Interface

RS (14E27)

EDI (21E34)

DOR (21E38)

NIOR

DAOR (21E27)

DA1R (21E20)

DA2R (21E18)

DA3R (21E13)

DA4R (21E08)

ED (21E33)

RSA (11E03)

RS (14E27)

ES (11E09)

IOAO (21E23)

IOA2 (21E15)

IOA3 (21E12)

RSA (11E03)

ORDER OUT (STOP)

FIOIA (13F34) } SEE SERVICE CONNECTION
FMOIA (5B39)

FIIIA (2E03)

S/TI = RS (14E27)
 (5D15)
 TIS000 : [IR.FGAIO+FGHIO.MYNUM]=ED (21E33)
 (4D02) MPR (16C01)

TIS160 : F111B (4E27)
 (4D26) NFKASC (16F26)
 [DOR] = ORD (9F36)
 [IOR] = OUT (9F39)
 [ORD. OUT] = O (4E21)
 [EDJ] = ED (21E33)
 SERVICEI (13F27)

TIS320 : FM31A (15B12)
 (4D29)

RS (14E27)
 IOR (14E34)
 DOR (21E38)
 EDI (21E34)
 ED (21E33)

FM31A (5B12)

S/TM = MPR (16C01)
 (5C15)

TMA000/1: NSXO (5F01)
 (4C02) drops to clear Stg.
 TMA000: SXCA (3D26)
 (23A28) CA reg. to S reg.
 TMS140: NMLXO (12A17), NMUXO (12A18)
 (4C03) drops to clear M reg.
 NMWXO (16B23)
 [NCM] = MRC (13D01)
 CA reg. +1 memory request.

[POK] = MPR (16C01)
 [DG] = MXM (16E46)
 [PE] = MPE (16C02)

TMA160 : FM31B (3B02)
 (23A20) CHAIN (16C96)
 [NCM] = MRQ2 (15C47)
 NMPE (23A14)
 TMB000-2: NCM (4B11)
 (3C19)
 TMB080 : [MKG.NMH] = STMAE (4A07)
 (3C19) STIOPH (4A09)
 TMB240 : [INSTMAE.NMRQ2]=FM31A (5B12)
 (23A01) [INSTMAE.NMRQ2]=FM32A (5B07)
 [STMAE]=FM33A (5B02)

Chaining Modifier was true
 Memory address error.

FM32A (5B07)

S/TM = MPR (16C01)
 (5C15)

TMA000/1: NIOXO-A (16F01)
 (4C02) drops to clear IO reg.
 [MHA,NHA5,NHA6,NHA7]=TRA (12E15)
 transfer in channel.
 TMA000: IOXM (1D01)
 (23A28) Order to IOAO-7
 [MPE] = STIOPME (4A21)
 TMS140 : [TRA.NMPE] = CAXM (21F01)
 (4C03) MCO-7@MDO-7 to CA reg.

Transfer in channel.

TMA160 : FM32B (3B01)
 (23A20) [TRA.TRAJ] = STIOPCE (4A12)
 [M IOA+7=C₁₆] = BKWD (2E47)
 read backwards.
 TMB000 : [STIOPME+STIOPCE] = STIOPH (4A09)
 (23A14)
 TMB080 : [TRA] = TRAJ (16C44)
 (3C19) remembers TRA
 TMS140 : [NWKWD] = BAXM (3D34)
 (4C03) MHS-7@MCO-7@MDO-7 to BA00-7B
 [BKWD] = BAXM (3D34)
 MBS-7@MCO-7@MDO-5 to BA00-16
 MDO-6 to BA17, MWD-7 to BA18
 TMB240 : [TRA.NSTIOPH] = FM31A (5B12)
 (23A01) [TRA.NSTIOPH] = FM33A (5B02)

Get and dispose of Ind. Word

FM33A (5B02)

S/TM = FM33A (5B02)
 (5C15)

TMA000-3: S31 (8D30)
 (23A28) for odd loc. access
 TMS140 : NMLXO (12A7), NMUXO (12A18)
 (4C03) drops to clear M reg.
 [NSTIOPH] = MRQ (13D01)
 memory request
 [POK] = MPR (16C01)
 [DG] = MXM (16E46)
 [PE] = MPE (16C02)

Transfer in channel.

TMA160 : FM33B (3B39)
 (23A20) IAPAXO (24C46)
 set IA reg. to 0
 set OA reg. to 0
 set RA reg. to 15
 TMB000-3: RSA (11E03)
 (23A13) [RSA.ED]=NSERVICEI (9F18)
 TMB240-4: FM34A (5B01)
 (23A01)

RSA (11E03)

FM34A (5B01)

S/TM = MPR (16C01)
 (5C15)

TMA000-2: FLCLEAR (19C18)
 (23A29)
 TMA080 : [MPE] = STIOPME (4A21)
 (3C36)
 TMS140 : [NSTIOPH] = BCXM (14F37)
 (4C03) MCO-7@MDO-7 to BC reg.
 TMA160 : FM34B (3B42)
 (23A20) P.ORD
 + STIOPH
 + DO.NFAST.FLIZC] = NFLCLEAR
 [DI.ED.FLIZC] (29C02)
 NMPE

TMB080 : [FLCLEAR] = NFLXO (14B33)
 (24C33) drops to clear flags.
 TMB160 : [FLCLEAR] = FLXM (20C45)
 (3C18) MA0 → FLDC (9D21)
 MA1 → FLIZC (9D46)
 MA2 → FLCC (9D09)
 MA3 → FLICE (9D07)
 MA4 → FLITE (9D02)
 MA5 → FLIUE (9D01)
 MA6 → FLISL (9D39)
 MA7 → FLSKIP (9D42)
 TMB240 : [DO.FLCLEAR] = FM21A (5B26)
 (23A01) [DI.FLCLEAR] = FM24A (5B27)
 [NFLCLEAR] = FM41A (5B42)

FM41A (5B42)

S/TM = RS (14E27)
 (5C15)

TMA000/1: NIOXO (16F02)
 (4C02) drops to clear IO reg.
 TMA000-3: ES (11E09)
 (23A28)
 TMA160 : FM41B (4A39)
 (23A20) [STIOPH] = IOA3 (21E12)
 TMB040 : [NSTIOPH] = NFLXO (14B33)
 (24C33) drops to clear flags.

RS (14E27)
 ES (11E09)
 IOA3 (21E12)
 RSA (11E03)

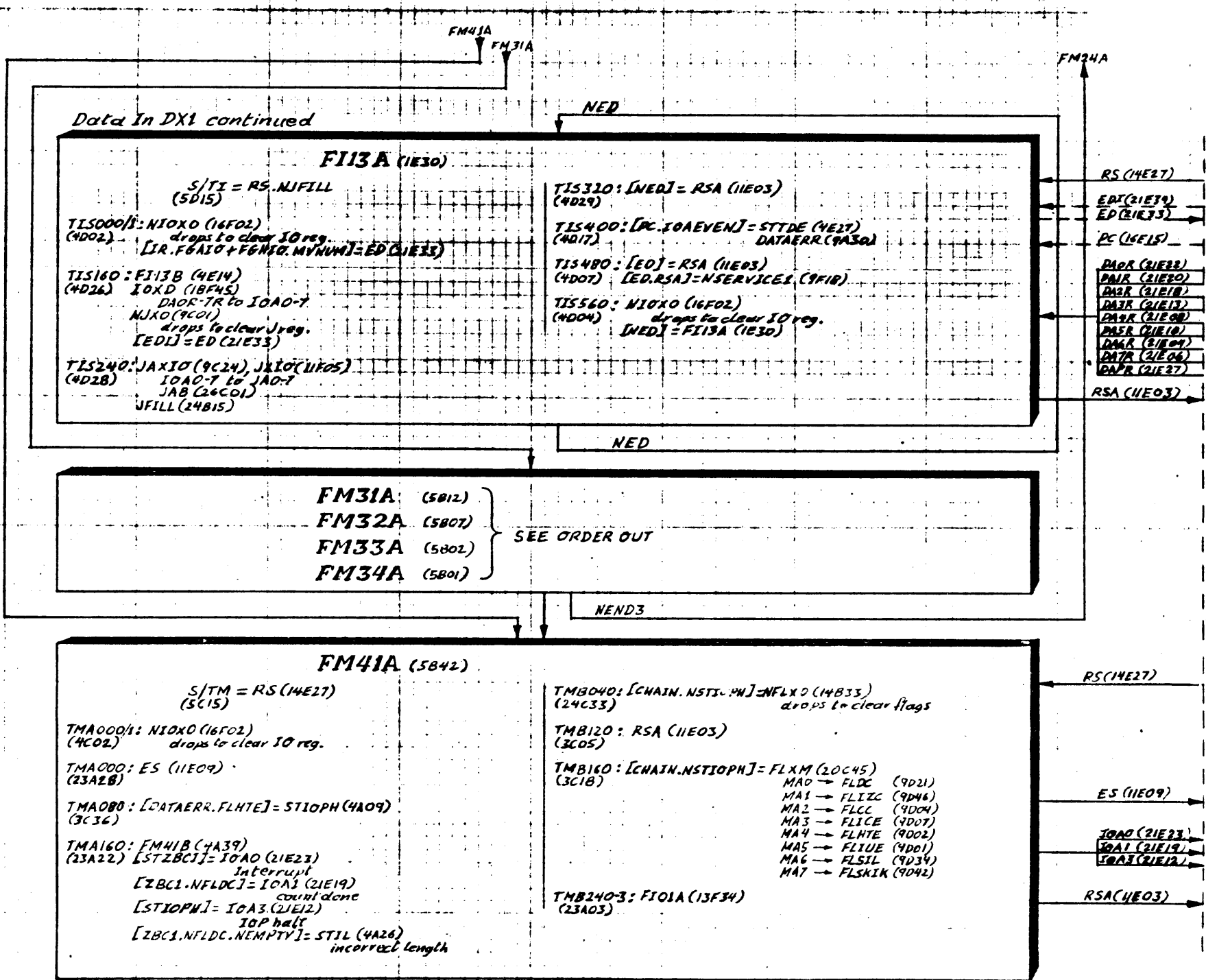
TMB120 : RSA (11E03)
 (3C05)
 TMB160 : [NSTIOPH] = FLXM (20C45)
 (3C18) MA0 → FLDC (9D21)
 MA1 → FLICE (9D46)
 MA2 → FLCC (9D09)
 MA3 → FLICE (9D07)
 MA4 → FLITE (9D02)
 MA5 → FLIUE (9D01)
 MA6 → FLSIL (9D39)
 MA7 → FLSKIP (9D42)
 TMB240 : FIOIA (13F34)
 (23A01)

Memory Interface

IOA0 (21E13)
 IOA1 (21E19)
 IOA2 (21E15)
 IOA3 (21E12)
 IOA4 (21E10)
 IOA5 (21E09)
 IOA6 (21E01)
 IOA7 (21E02)

Device Controller Interface.

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Data In DX4 continued.

FM31A (1E30)

S/IR = RS-NUFILL
 TR5000: [NKOXO] = NKOXO (1E021) drops to clear J reg. [IR.FGATC+FGIC.MYNUM]= ED (2IE33)
 TR5160: FM31B (4E14) Data (lines to J reg. NUXO (1E021) drops to clear J reg. [EDI]= ED (2IE33)

TR5240: JAXIC (4E14), JXIC (1E05) J reg. to J reg. JAR (2E02), JBR (2E02), JCR (2E02), JDB (2E02), JFILL (24B15)
 TR5320: [NED]= RSA (1E03) (4D29)
 TR5440: [ED]= RSA (1E03) (4D07) [EDUNA]= NSERVICEJ (4F1B) (4D04)
 TR5560: NIOXG (1E02) drops to clear J reg. [NEL]= FM31A (1E30)

WRITE into Fast Memory

JAO-8 to W/RBO-8
 SWRITE = JFILL, (32B18) (24B15)
 S/TR = SWRITE CYCLE (32A15) (30A35)
 TR5030: WRITE (25B26) (31A34)
 TR5060: J reg to LR reg. (31A30) NUFILL (29A22)

TR120: JAREG+1 (31A26) RAREG-1
 NEMPTU (18C34)
 TR1150: W/RBO-8 to KAO-8
 W/RBO-8 to RBO-8
 JCO-8 to KCO-8
 JDO-8 to RDO-8
 TR5250: [ED]= ENDI (4F2E) RENAME: ED (31A07)

READ from Fast Memory 2nd through n's time

[RAB]= SAA(5B45)
 S/READ = NKDB.NEMPTU.SREADEN (32B02) .N(KFILLI.NMAYREAD)
 S/IR = S/READ.CYCLE (32A15) (30A35)
 TR5030: READ (30A01) (31A34)
 TR5060: CA reg to LR reg. (31A30)
 TR5120: [NKAB]= KAA (25A46) (31A26) [SAA.KAA]= PATH2 (2E813) CA reg+1 RAREG+1
 TR1230: [PATH6]= MODE6 (13C0) RBO-7 to KAO-7 KCO-7 to KCO-7 RDO-7 to KDO-7
 KAO (24B10) KCB (24B11) KDB (24B25)
 TR5240: [ANOTHER]= NRAM (31A05) NRCM
 [EMPTY.ENDI]= ENDI (4B27)

[NRAB.NKBB.NKCB.RDA]= SAD (25B47) [NKAB.NKBB.RC.R]= SAC (25B46)
 S/READ = NKDB.NEMPTU.SREADEN (32B02) .N(KFILLI.NMAYREAD)
 S/IR = S/READ.CYCLE (32A15) (30A35)
 TR5030: READ (30A01) (31A34)
 TR5060: CA reg to LR reg. (31A30)
 TR5120: [NKAB]= KAA (25A46) (31A26) [SAA.KAA]= PATH2 (2E813) CA reg+1 RAREG+1
 TR5220: NANOTHER (25A02) (31A29)
 TR1230: [PATH4]= MODE4 (20A28) RCO-7 to KAO-7 KCO-7 to KCO-7 RDO-7 to KDO-7
 KAO (24B10) KCB (24B11) KDB (24B25)
 TR5240: [ANOTHER]= NRAM (31A05) NRCM
 [EMPTY.ENDI]= ENDI (4B27)

[NRAB.NKBB.NKCB.RC.R]= SAC (25B46)
 S/READ = NKDB.NEMPTU.SREADEN (32B02) .N(KFILLI.NMAYREAD)
 S/IR = S/READ.CYCLE (32A15) (30A35)
 TR5030: READ (30A01) (31A34)
 TR5060: CA reg to LR reg. (31A30)
 TR5120: [NKAB]= KAA (25A46) (31A26) [SAA.KAA]= PATH4 (2E816) CA reg+1 RAREG+1
 TR5220: NANOTHER (25A02) (31A29)
 TR1230: [PATH4]= MODE4 (20A28) RCO-7 to KAO-7 KCO-7 to KCO-7 RDO-7 to KDO-7
 KAO (24B10) KCB (24B11) KDB (24B25)
 TR5240: [ANOTHER]= NRAM (31A05) NRCM
 [EMPTY.ENDI]= ENDI (4B27)

[NRAB.RBB]= SAB (25B44)
 S/READ = NKDB.NEMPTU.SREADEN (32B02) .N(KFILLI.NMAYREAD)
 S/IR = S/READ.CYCLE (32A15) (30A35)
 TR5030: READ (30A01) (31A34)
 TR5060: CA reg to LR reg. (31A30)
 TR5120: [NKAB]= KAA (25A46) (31A26) [SAB.KAA]= PATH6 (2E814) CA reg+1 RAREG+1
 TR5220: NANOTHER (25A02) (31A29)
 TR1230: [PATH6]= MODE6 (13C0) RBO-7 to KAO-7 KCO-7 to KCO-7 RDO-7 to KDO-7
 KAO (24B10) KCB (24B11) KDB (24B25)
 TR5240: [ANOTHER]= NRAM (31A05) [BCCI+BCC2+BCC3]= KDB (24B25)

TR5240: K FILLI (30A21) (31A05)

[KDB]= K FILLI (30A21) (31A05)
 [NKDB.NEMPTU.SREADEN]= S/READ (32B02)
 S/IR = S/READ.CYCLE (32A15) (30A35)
 TR5030: READ (30A01) (31A34)
 TR5060: CA reg to LR reg. (31A30) [RAB]= SAA (25B45)
 TR5120: [RAB.NKBB]= KAB (25A47) (31A26) [SAA.KAA]= PATH3 (2E813) CA reg+1 RAREG+1
 [KAB.KCB]= ANOTHER (26C33)
 TR1230: [PATH3]= MODE3 (13C3) RAO-7 to KAO-7 KCO-7 to KCO-7 RDO-7 to KDO-7
 KBB (24B27) KCB (24B11) KDB (24B25)

[KDB]= K FILLI (30A21) (31A05)
 [NKDB.NEMPTU.SREADEN]= S/READ (32B02)
 S/IR = S/READ.CYCLE (32A15) (30A35)
 TR5030: READ (30A01) (31A34)
 TR5060: CA reg to LR reg. (31A30) [RAB]= SAA (25B45)
 TR5120: [RAB.NKBB.NKCB]= KAC (25A44) (31A26) [SAA.KAA]= PATH3 (2E813) CA reg+1 RAREG+1
 [KAC.KCB]= ANOTHER (26C33)
 TR1230: [PATH3]= MODE3 (13C3) RAO-7 to KAO-7 KCO-7 to KCO-7 RDO-7 to KDO-7
 KCB (24B11) KDB (24B25)

[KDB]= K FILLI (30A21) (31A05)
 [NKDB.NEMPTU.SREADEN]= S/READ (32B02)
 S/IR = S/READ.CYCLE (32A15) (30A35)
 TR5030: READ (30A01) (31A34)
 TR5060: CA reg to LR reg. (31A30) [RAB]= SAA (25B45)
 TR5120: [RAB.NKBB.KCB]= KAD (25A45) (31A26) [SAA.KAD]= PATH5 (2E834) CA reg+1 RAREG+1
 [KAD.KCB]= ANOTHER (26C33)
 TR1230: [PATH5]= MODE5 (20B25) RAO-7 to KAO-7 KCO-7 to KCO-7 RDO-7 to KDO-7
 TR5240: [KDB]= K FILLI (30A21) (31A05) [ANOTHER]= CA reg-1 RAREG-1 RAM (22A21) grounds: RAB

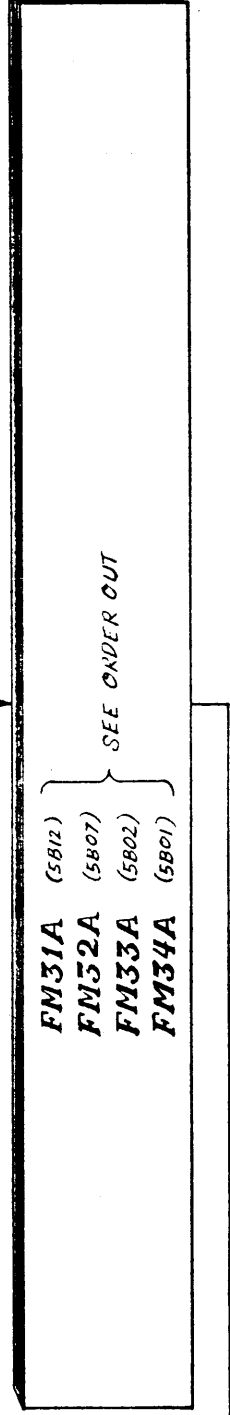
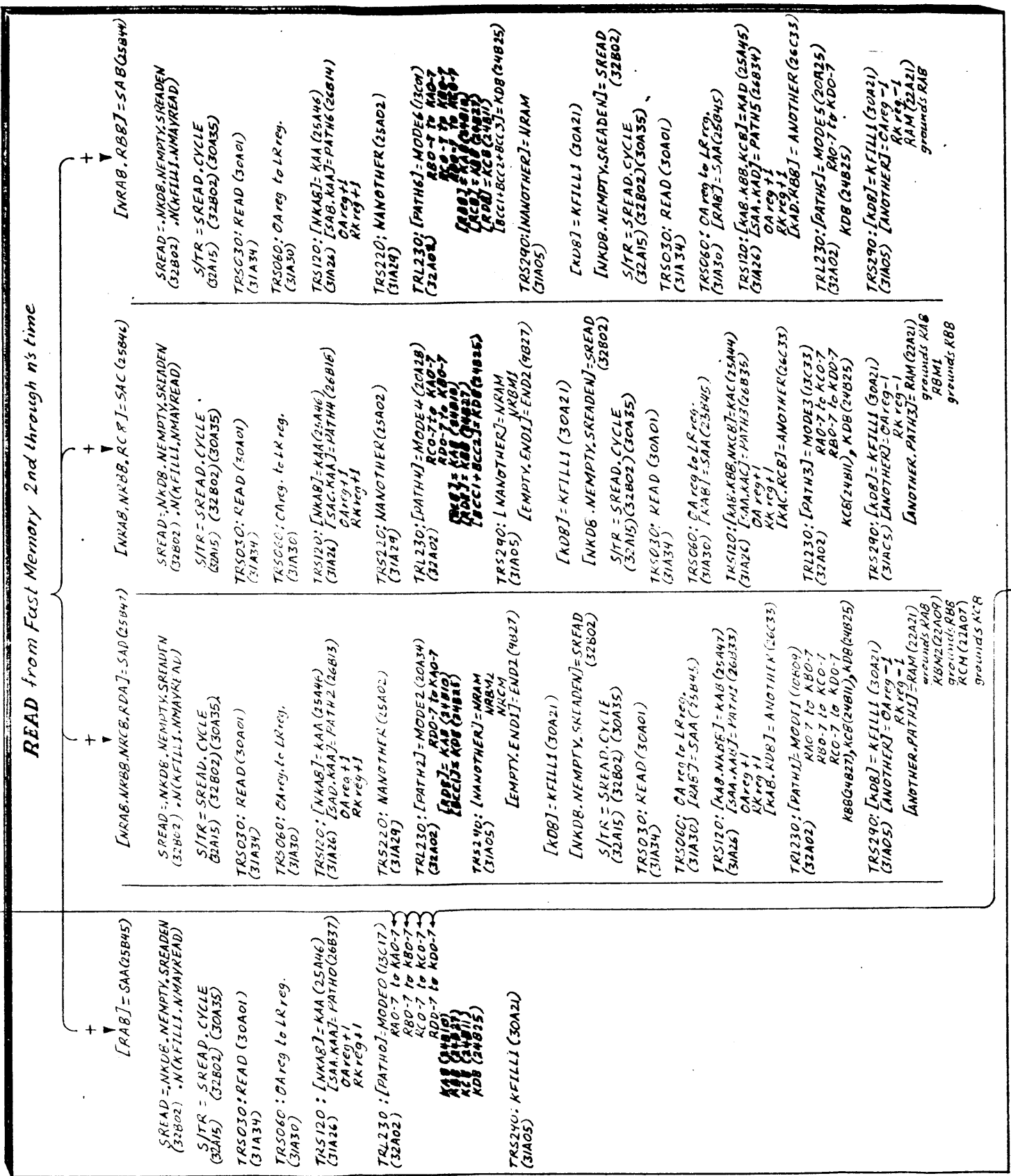
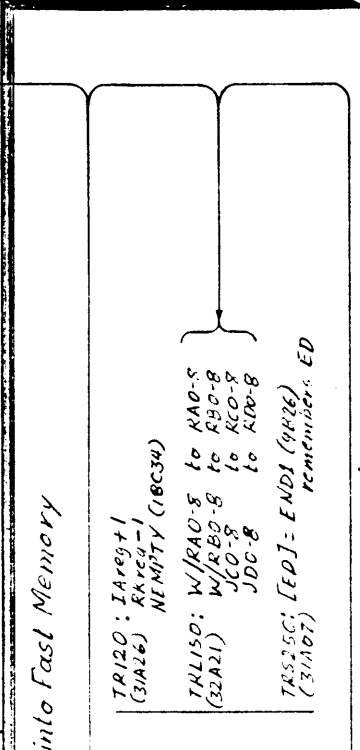
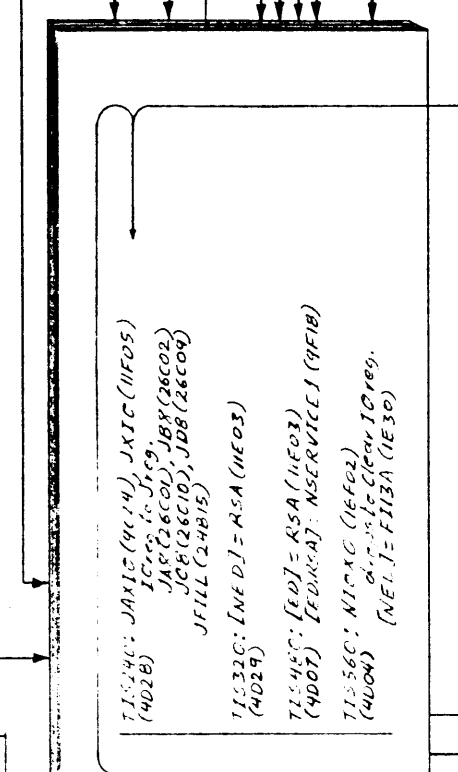
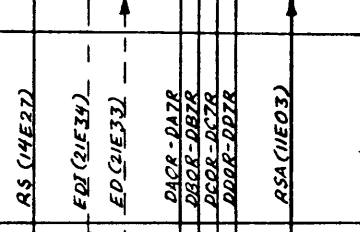
To FM24A

- FM31A (5B12)
- FM32A (5B07)
- FM33A (5B02)
- FM34A (5B01)

SEE ORDER OUT

2nd to's Data Flow

Device Controller Interface



FM41A

Data In DX4 continued

FMHIA (5842)

S/IM = RS (14E27)

(5C15)

TMA000A: NIOXO (1EFO2)

(4C02) drops to clear IOreq

TMA000C: ES (11E04)

(23A28)

TMA160: FM41B (4A39)

(3A22) [STZBCI] = IOAO (21E23)

[ZBCL.NFLDCJ] = IOA (21E19)

[STIOPH] = IA03 (21E12)

POP, HALC

[ZBCL.NFLDC.NEMPTYJ] = STIL (4A26)

incorrect length

TMB000: [CHAIN.NSTIOPH] = NFLXO (MB33)

(24C33)

TMB120: RSA (11E03)

(3C05)

TMB160: [CHAIN.NSTIOPH] = FLXM (20C45)

(3C18) MA0 → FLDC (9D21)

MA1 → FLDC (9D4E)

MA2 → FLCC (9D0F)

MA3 → FLCC (9D07)

MA4 → FLHE (9D02)

MA5 → FLHE (9D01)

MA6 → FLSL (9D39)

MA7 → FLSKIP (9D42)

TMB240-3: FLOIA (31F34)

(23A03)

RS (14E27)

ES (11E03)

IOAO (21E19)

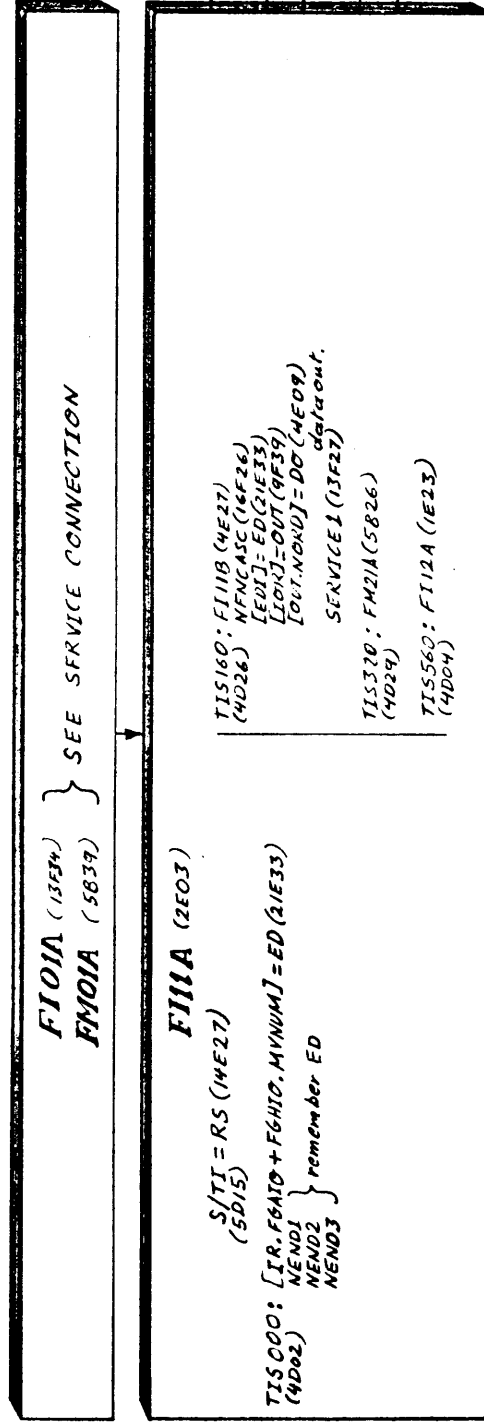
IOA (21E19)

IOA (21E12)

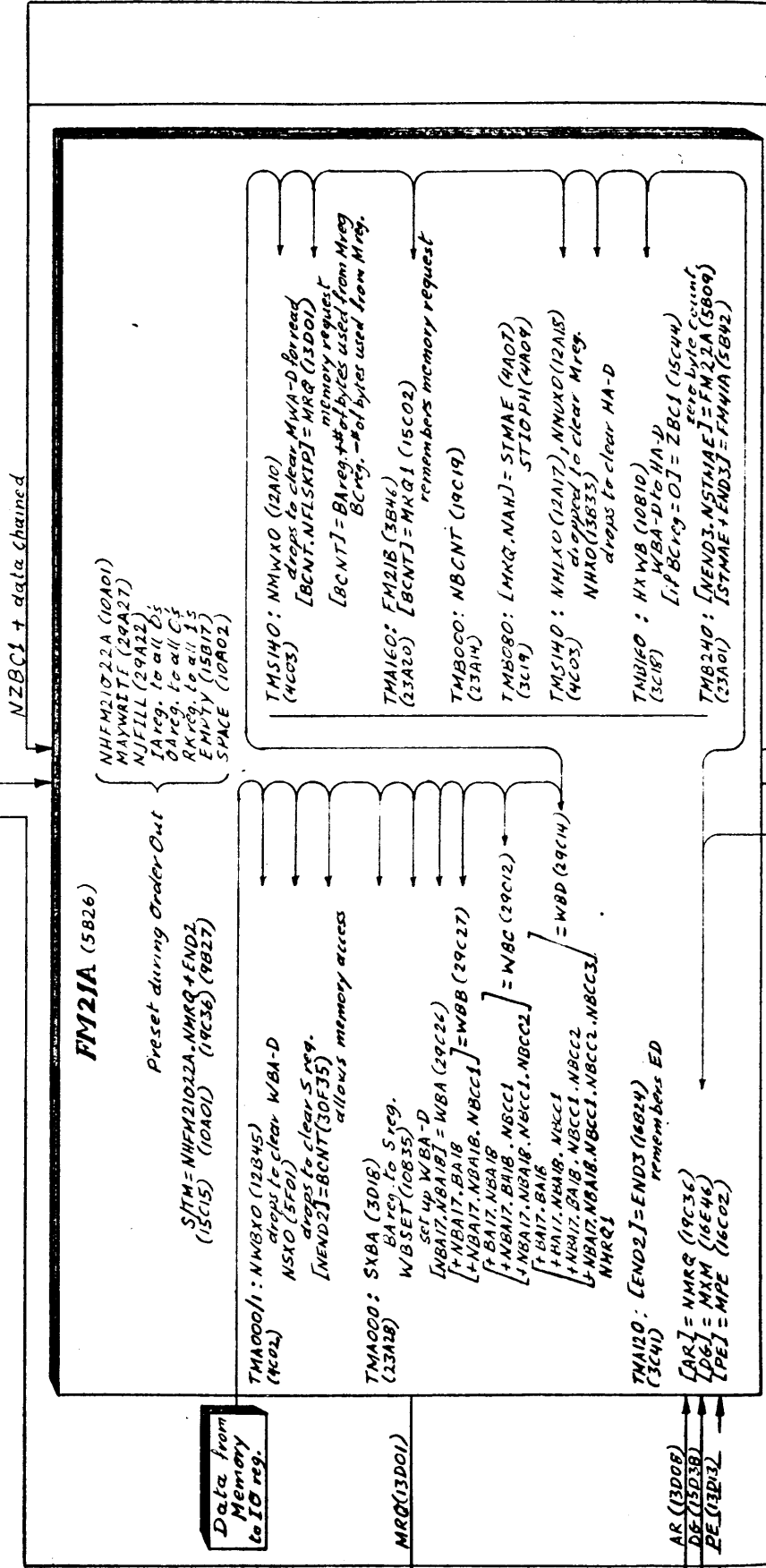
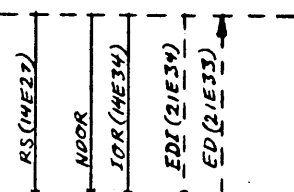
RSA (11E03)

Device Controller Interface

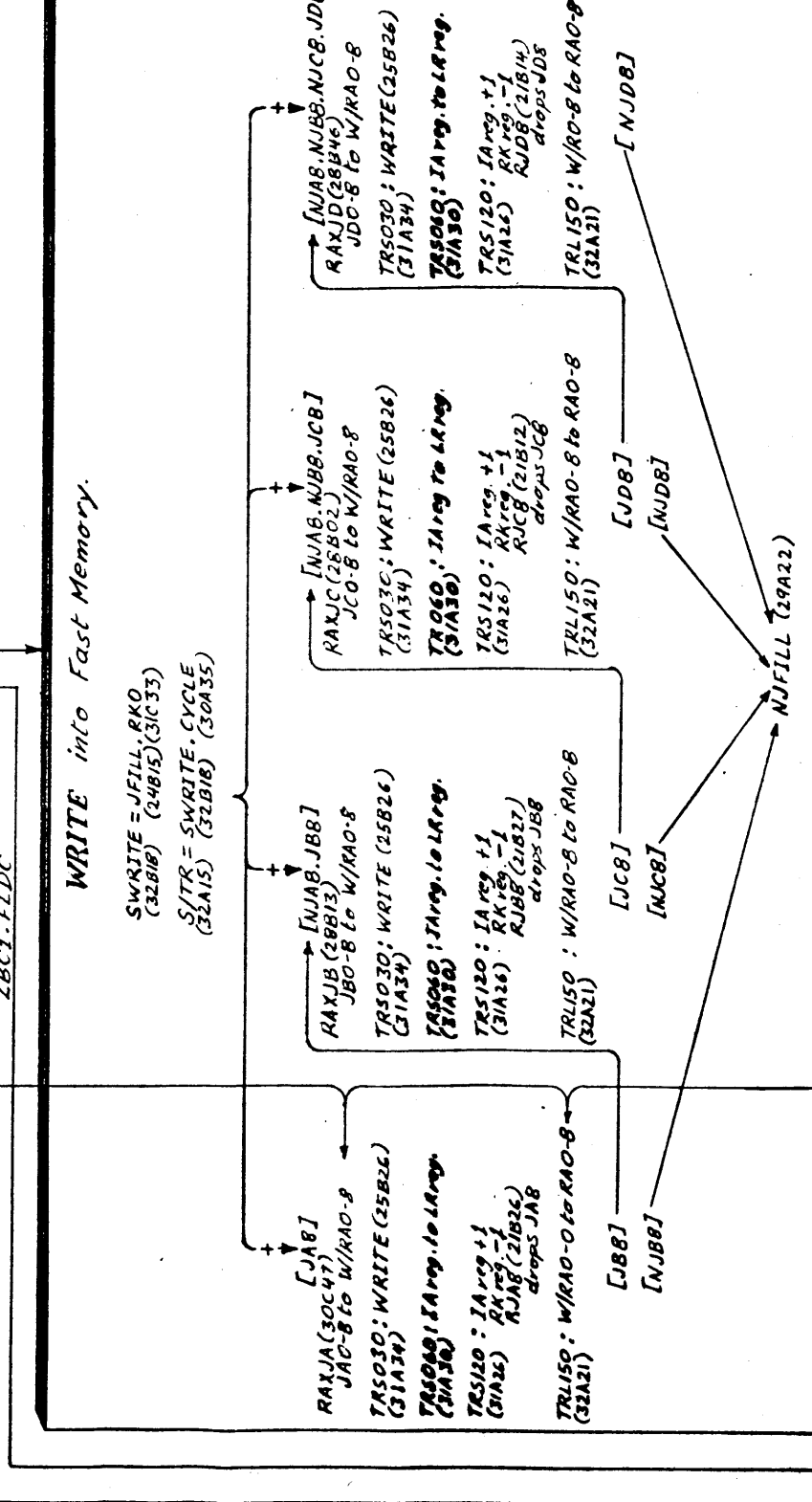
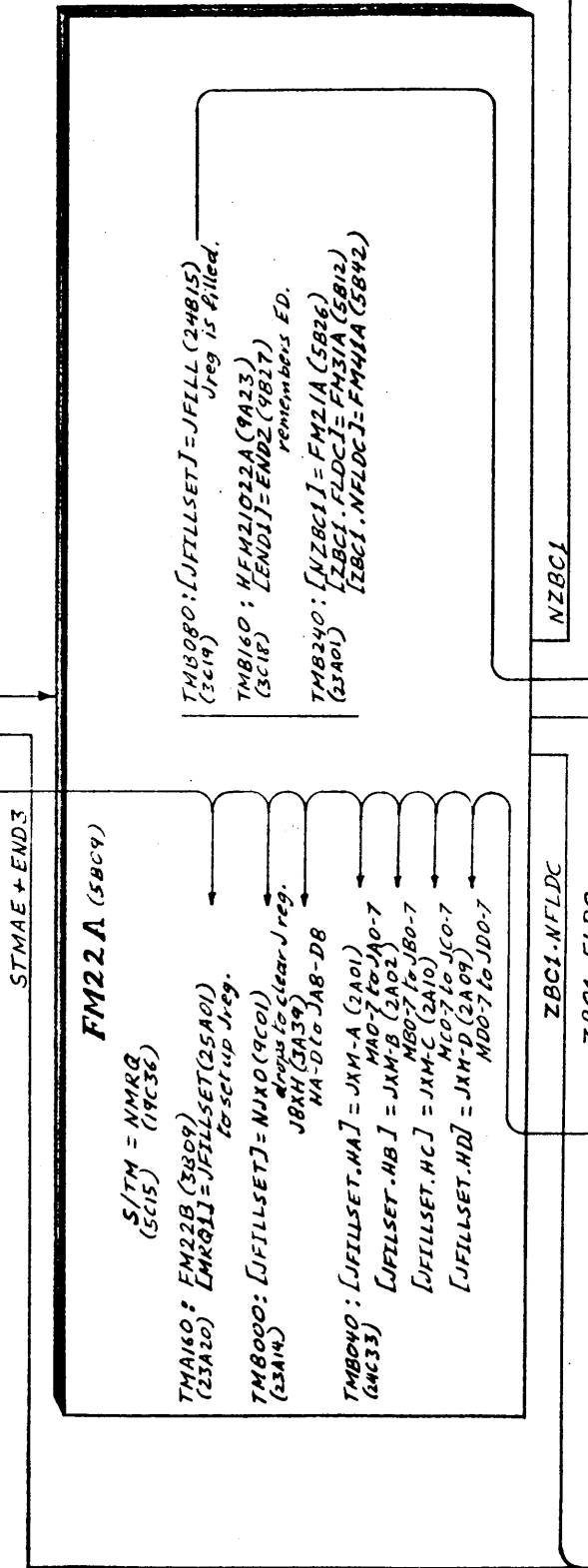
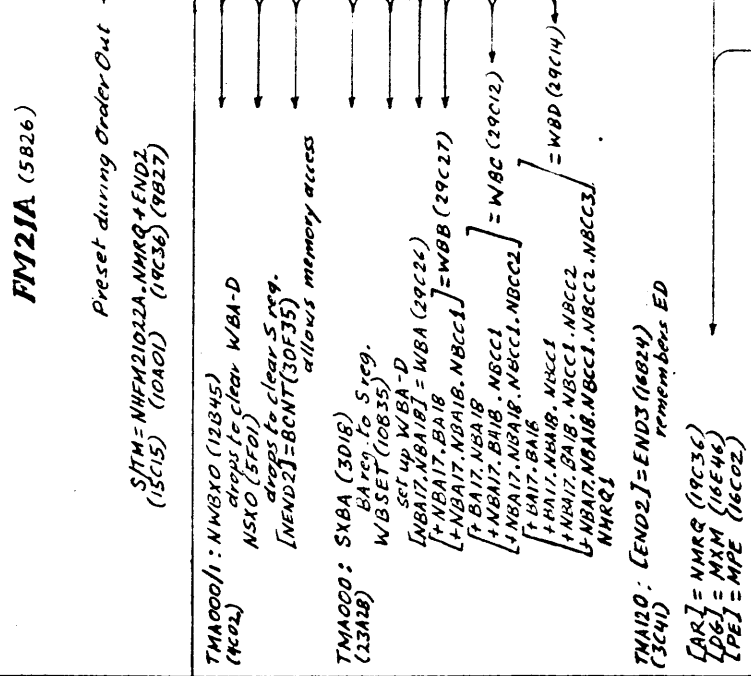
Data Out DXI (SIOP)



Device Controller Interface

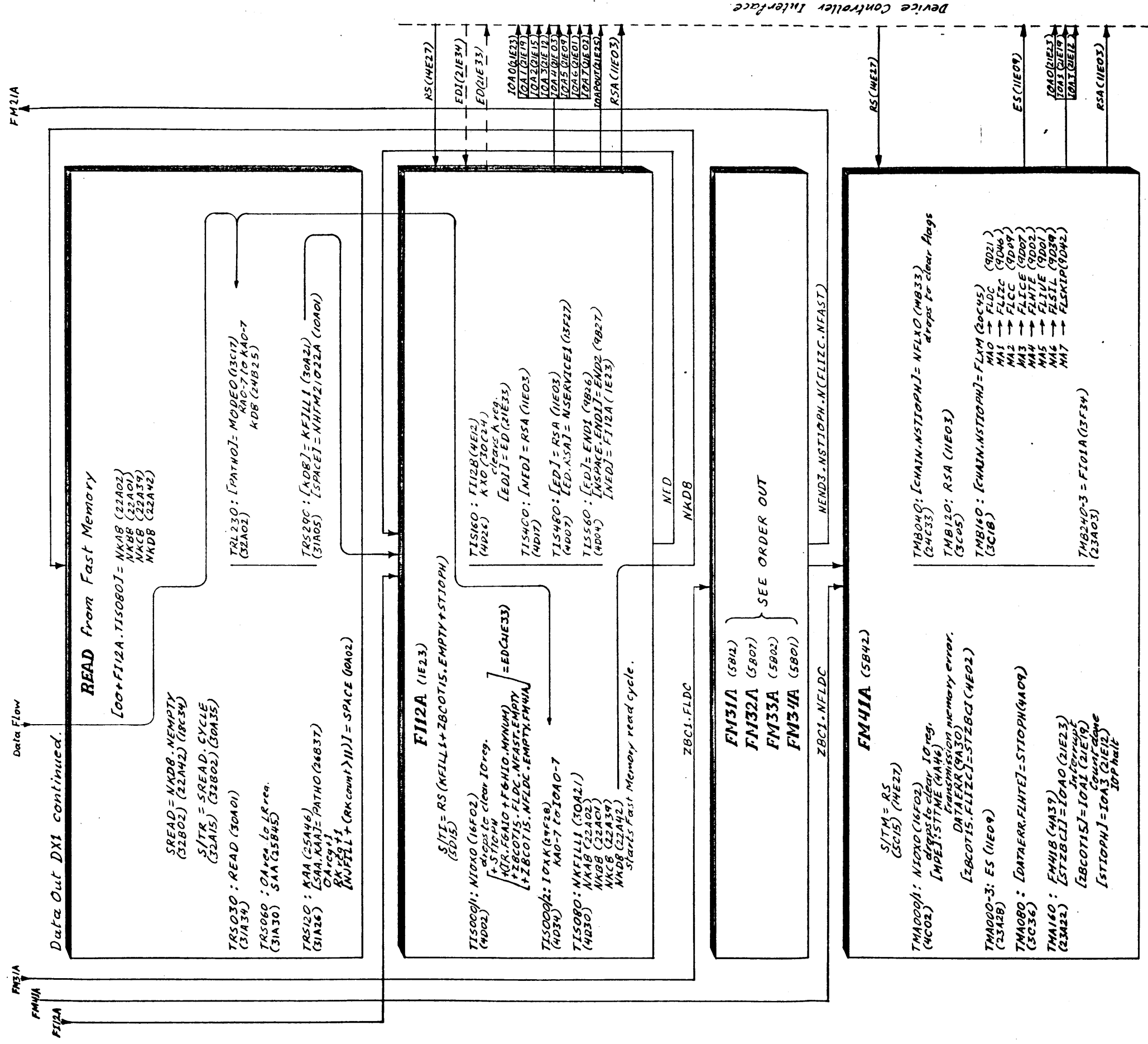


NZBC1 + data chained



data chained.

Memory Interface.



Data Out DX4 (STOP)

F101A (12F34) } SEE SERVICE CONNECTION
 FMO1A (5B39)

FM11A (2E03)
 S/TI = RS (4E27)
 (5D15)
 T1S000: [IR, F6A10 + FGH10, MVMUM] = ED (2IE33)
 (4D02) NEND1 } remember ED
 NEND2 }
 NEND3 }

T1S160: FI11B (4E27)
 (4D26) NFENASC (4F26)
 [ED1] = ED (2IE33)
 [LOK] = OUT (4F34)
 [OUT, NOK] = DC (4FC9)
 data out
 SERVICE1 (13F27)
 T1S320: FM21A (5B26)
 (4D37)
 T1S560: FI12A (1E23)
 (4D04)

D.C. Interface
 RS (4E27)
 NDOA
 IOR (4E34)
 ED (2IE34)
 ED (2IE33)

NEND2, N3BCL, NSTMAE

FM21A (5B26)

Preset during Order Out

S/TM = NHFM21022A, NMRQ + FND2
 (5C15) (10A01) (49C36) (9827)
 TMA000: NMBXO (12845)
 (4C02) BA reg. to S reg.
 NSXO (5F01)
 [N3BCL, NEND2, MAYWRITE] = BCNT (30F35)
 allows memory access
 TMA000: SXBA (3D18)
 (23A28) BA reg. to S reg.
 WBSSET (10B35)
 sets up WBA-D
 [NBA17, NBA18] = WBA (29C26)
 + NBA17, NBA18
 [NBA17, NBA18, NBCC1] = WBB (29C27)
 + NBA17, NBA18, NBCC1
 [NBA17, NBA18, NBCC1, NBCC2] = WBC (29C12)
 + NBA17, NBA18, NBCC1, NBCC2
 + NBA17, NBA18, NBCC1, NBCC2
 + NBA17, NBA18, NBCC1, NBCC2
 NMRQ1
 TMA120: [END2] = EVD3 (16B24)
 (3C41) remembers ED
 TMS140: NMMXO (12A10)
 (4C03) drops to clear MWA-D for read
 [BCNT, NFLSKIP] = MRQ (13D01)
 [BCNT] = BA reg. + # of bytes used from M reg.
 BC reg. - # of bytes used from M reg.

One way of Data Flow

Another way of Data Flow

NHFM21022A (10A01)
 MAYWRITE (29A27)
 NJFILL (29A22)
 JA reg. to all O's
 KA reg. to all 1's
 LMBY (4F17)
 SPACE (10A02)
 TMA160: FM21B (3046)
 (23A10) [BCNT] = MRQL (15C02)
 remembers MRQ
 [MRQ2] = JFILLSET (25A01)
 to setup J reg.
 TMA240: [NBNCT, NSHARE] = NMXO (9C01)
 (3C35) [NHFM21022A, FND2] = FND2 (9B27)
 remembers ED
 TMB000: [JFILLSET] = NMXO (9C01)
 (23A44) drops to clear J reg.
 JBAH (3A39)
 HA-D to JAR-DE
 [NSPACE] = NMAVWRITE
 NBCT (49C19)
 TMB040: [JFILLSET, HA] = JXM-A (2A01)
 (24C33) MHO-7 to JAO-7
 [JFILLSET, HB] = JXM-B (2A02)
 MBO-7 to JBO-7
 [JFILLSET, HC] = JXM-C (2A10)
 MCO-7 to JCO-7
 [JFILLSET, HD] = JXM-D (2A09)
 MDO-7 to JDO-7
 TMB080: [MRQ, NAI] = STMAE (4A07)
 (3C19) STIOPH (4A09)
 [JFILLSET] = JFILL (24B15)
 J reg is filled
 TMS140: NMLXO (12A17), NMXO (12A18)
 (4C03) drops to clear M reg.
 NMXO (15B33)
 drops to clear HA-D
 TMS160: NMXB (10B10)
 (3C18) WBA-D to HA-D
 [N3BCL, NEND2] = ZBC1 (15C44)
 zero byte count.
 TMB240: [NEND3, NZBCL, NSTMAE] = FM22A (5B09)
 (23A01) [NSTMAE, ZBC1, FLDC] = FM21A (5B12)
 [STMAE, END3, ZBC2, NFLDC] = FM11A (5B42)

ZBC2, FLDC
 ZBC2, NFLDC + END3 + STMAE

FM22A (5B09)

S/TM = NHFM21022A, NMRQ + FND2
 (5C15) (10A01) (49C36) (9827)
 TMA000: NMBXO (12845)
 (4C02) drops to clear WBA-D
 NSXO (5F01)
 [MAYWRITE, NZBCL, NSHARE] = BCNT (30F35)
 allows memory access
 TMA000: SXBA (3D18)
 (23A28) BA reg. to S reg.
 WBSSET (10B35)
 sets up WBA-D
 [NBA17, NBA18] = WBA (29C26)
 + NBA17, NBA18
 [NBA17, NBA18, NBCC1] = WBB (29C27)
 + NBA17, NBA18, NBCC1
 [NBA17, NBA18, NBCC1, NBCC2] = WBC (29C12)
 + NBA17, NBA18, NBCC1, NBCC2
 + NBA17, NBA18, NBCC1, NBCC2
 + NBA17, NBA18, NBCC1, NBCC2
 NMRQ2 (49C44)
 TMA120: [END2] = EVD3 (16B24)
 (3C41) remembers ED
 TMS140: NMMXO (12A10)
 (4C03) drops to clear MWA-D for read.
 [BCNT, NFLSKIP] = MRQ (13D01)
 [BCNT] = BA reg. + # of bytes used from M reg.
 BC reg. - # of bytes used from M reg.

TMA160: FM22B (5B09)
 (23A20) [MRQ] = JFILLSET (25A01)
 to set up J reg.
 [BCNT] = MRQ2 (15C47)
 remembers MRQ
 TMA240: [NBCNT] = NHFM21022A (9A23)
 (3C35) [NHFM21022A, END2] = END2 (9B27)
 remembers ED
 TMB000: [JFILLSET] = NMXO (9C01)
 (23A44) drops to clear J reg.
 JBAH (3A39)
 HA-D to JAR-DE
 [NSPACE] = NMAVWRITE
 NBCT (49C19)
 TMB040: [JFILLSET, HA] = JXM-A (2A01)
 (24C33) MHO-7 to JAO-7
 [JFILLSET, HB] = JXM-B (2A02)
 MBO-7 to JBO-7
 [JFILLSET, HC] = JXM-C (2A10)
 MCO-7 to JCO-7
 [JFILLSET, HD] = JXM-D (2A09)
 MDO-7 to JDO-7
 TMB080: [MRQ, NAI] = STMAE (4A07)
 (3C19) STIOPH (4A09)
 [JFILLSET] = JFILL (24B15)
 J reg is filled
 TMS140: NMLXO (12A17), NMXO (12A18)
 (4C03) drops to clear M reg.
 NMXO (15B33)
 drops to clear HA-D
 TMS160: NMXB (10B10)
 (3C18) WBA-D to HA-D
 [N3BCL, NEND3, ZBC1, NFLDC] = FM11A (5B42)
 zero byte count.

ZBC1, FLDC
 ZBC1, NFLDC + END3 + STMAE

MRQ (3D0)

AR (13D08)
 DE (15D38)
 PE (16D05)

Memory Interface

Data Out DX4 continued.

FM41A (5842)

S/IM = RS (1HE27)

TMA000/1: M100 (16F02)
drops to clear IO reg.
[MPE]: STIME (1A46)
TRANSMISSION MEMORY ERROR.
DATAERR (9A30)

[18C0T5: FLIZC] = STZBCI (1E02)

TMA000-3: ES (11E09)

TMA000: [DATAERR.FLHTE] = STIOPH (4A09)

TMA160: FMH1B (4A34)
TMA160: [STZBCI] = IOAC (21E23)
IOA1 (21E19)

[ZBC0T15] = IOA1 (21E19)
COUNT COMP
IOP halt.
[STIOPH] = IOA3 (21E12)

TMB040: [CHAIN.NSTIOPH] = NFLXO (14B33)
drops to clear flags.
(24C33)

TMB120: RSA (11E03)
(3C05)

TMB160: [CHAIN.NSTIOPH] = FLXM (20C45)
MA0 → FLDC (9D21)
MA1 → FLZC (9D4C)
MA2 → FLCC (9D09)
MA3 → FLICE (9D07)
MA4 → FLHTE (9D02)
MA5 → FLIUE (9D01)
MA6 → FLSIL (9D39)
MA7 → FLSNIP (9D42)

TMB240-3: FIOJA (13F34)
(23A03)

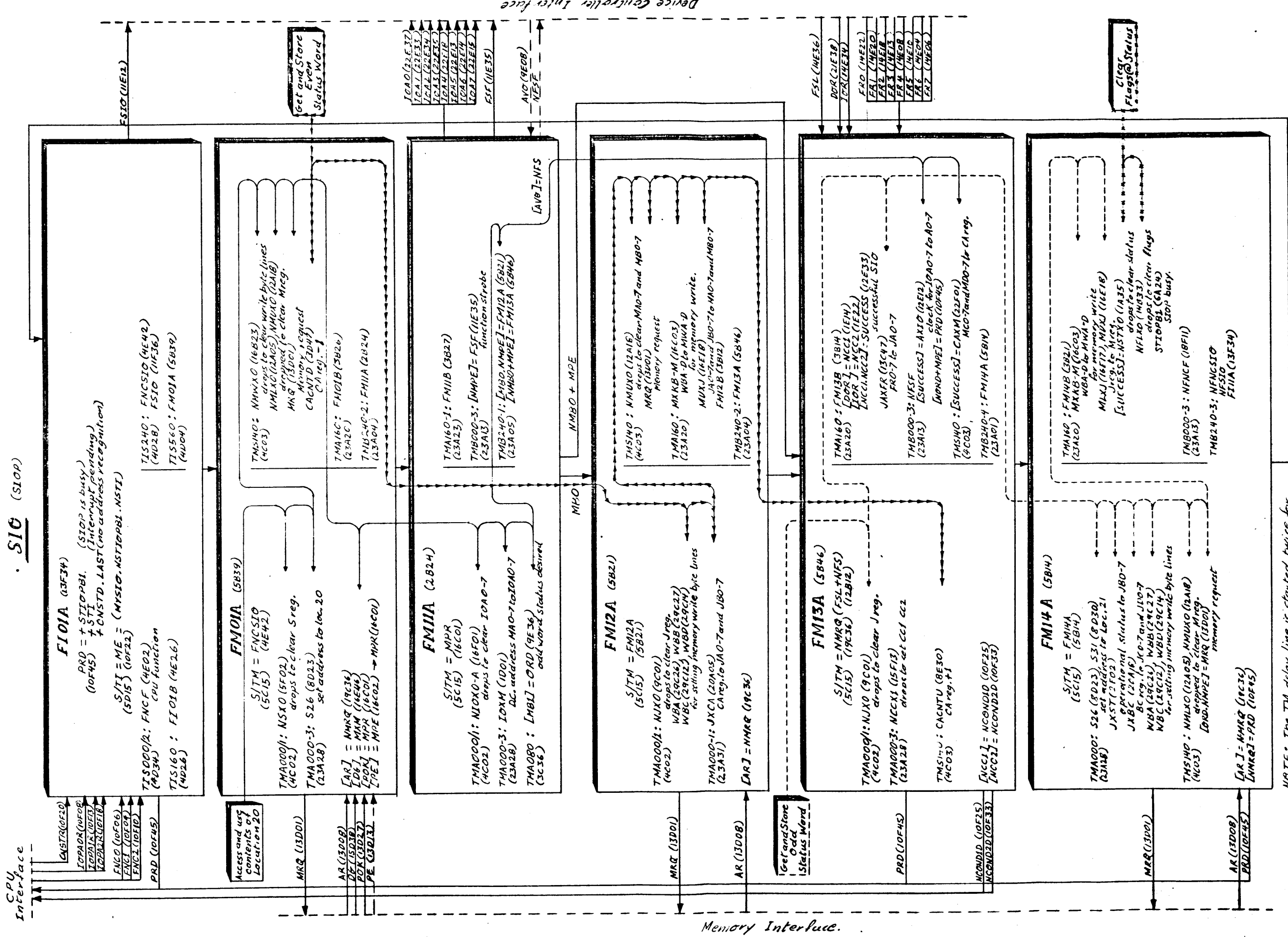
RS (14E27)

ES (11E09)

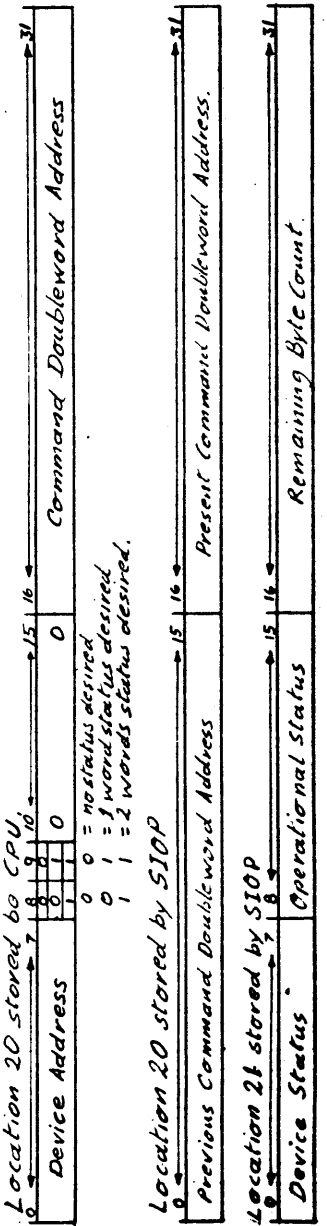
IOAC (21E23)
IOA1 (21E19)
IOA3 (21E12)

RSA (11E03)

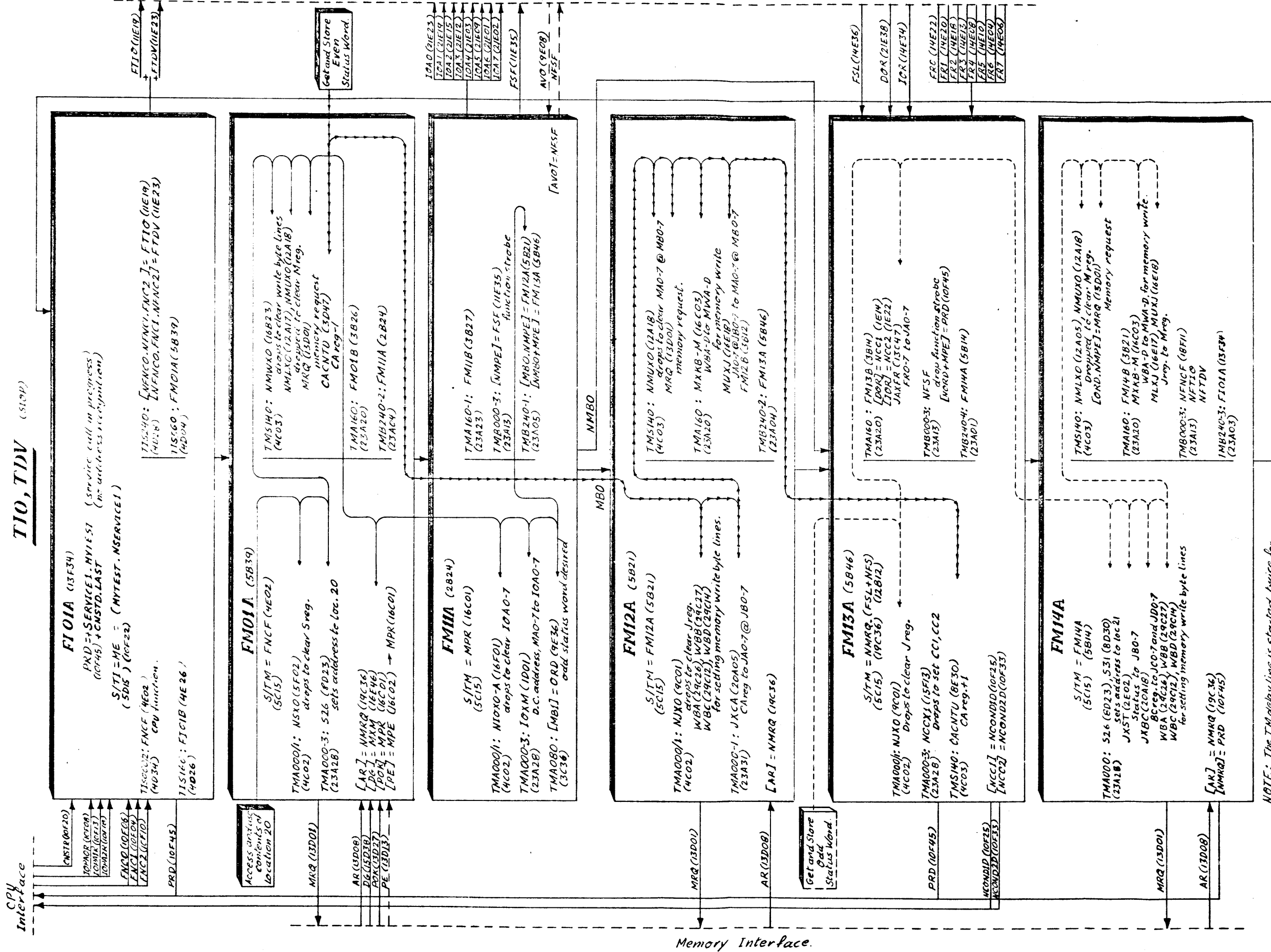
D.C. Interface



- Operational Status:
- 8 = STILL
 - 9 = STIDE
 - 10 = STIME
 - 11 = STIME
 - 12 = STIME
 - 13 = STIME
 - 14 = STIME
 - 15 = STIME
- Bit =
- 9 = Incorrect length
 - 10 = Transmission data error
 - 11 = Memory address error
 - 12 = IOP memory error
 - 13 = IOP control error
 - 14 = IOP half
 - 15 = IOP busy



TIO, TDV (STOP)



NOTE: The TM delay line is started twice for every FM phase.

Location 20 stored by CPU

Device Status	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Location 20 stored by STOP

Previous Command Doubleword Address	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Location 21 stored by STOP

TIO/Device Status	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Operational Status

Operational Status	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- Operational Status.
- Bit 8 = STILL = Incorrect length
 - 9 = STIDE = Transmission data error
 - 10 = STIME = Memory address error
 - 11 = STMAE = IOP memory error
 - 12 = STIDME = IOP memory error
 - 13 = STIDPE = IOP memory error
 - 14 = STIDPH = IOP halt
 - 15 = STIDPB = IOP busy

MEMORY

Σ5/7 or 6 MATRIX 1 & 2

8265/8465

A
 B
 C
 D
 E
 F
 Page 3-202

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
A	ZT 46	ZT 46	ZT 46	FT 79	FT 79	FT 83	XT 10	AT 60		AT 60	FT 83	BT 36	AT 60	BT 36	AT 60	XT 10	IT 16	AT 60	BT 36	AT 60	BT 36	FT 83	AT 60		AT 60	XT 10	FT 83	FT 79	FT 79	ZT 46	ZT 46	ZT 46		
B	TO BANK A 30A	31A	32A	M00A M07A	M16A M23A	M:2A		L29 L31		M15 M27			L29 L31		M15 M27			M15 M27	L29 L31				M15 M27	L29 L31			M32B	M16B M23B	M00B M07B	TO BANK B 30A	31A	32A		
C	FT 79	FT 79	FT 79	FT 79	FT 79	FT 82	AT 60		AT 60		BT 15	AT 60	BT 36	AT 60	BT 36	BT 36	BT 36	BT 36	AT 60	BT 36	AT 60	BT 16	IT 16	AT 60		AT 60	FT 82	FT 79	FT 79	FT 79	FT 79	FT 79		
D	-L REG. A -			M08A M15A	M24A M31A		MQ		M00 M13			MQ		M00 M13				M00 M13			MQ				M00 M13			MQ		M24B M31B	M08B M15B	-L REG. B -		
E	ZT 45	ST 49		ST 49	LT 106	AT 10	LT 106	AT 75	AT 75	LT 106	AT 10	LT 106	ST 49					ST 49	FT 66	ST 49	LT 106	AT 10	LT 106	AT 75	AT 75	LT 106	AT 10	LT 106	ST 49	ZT 45	ST 49	XT 10	XT 10	
F	XT 10		XT 10		P4: AHA	L15 L28	P4: AHB	PORT SEL. MATRIX A	PORT SEL. MATRIX B	P3: AHA	L15 L28	P3: AHB							AH		P2: AHA	L15 L28	P2: AHB	PORT SEL. MATRIX A	PORT SEL. MATRIX B	P1: AHA	L15 L28	P1: AHB						
G		ZT 46	ZT 46	FT 79	FT 79	FT 83	XT 10	AT 60		AT 60	FT 83	BT 36	AT 60	BT 36	AT 60	XT 10	IT 16	AT 60	BT 36	AT 60	BT 36	FT 83	AT 60		AT 60	XT 10	FT 83	FT 79	FT 79	ZT 46	ZT 46			
H		TO BANK A 31B	32B																														TO BANK B 31B	32B
I	FT 79	FT 79	FT 79	FT 79	FT 79	FT 82	AT 60		AT 60		BT 15	AT 60	BT 36	AT 60	BT 36	BT 36	BT 36	BT 36	AT 60	BT 36	AT 60	BT 16	IT 16	AT 60		AT 60	FT 82	FT 79	FT 79	FT 79	FT 79	FT 79		
J	XT 10	ST 49	XT 10	ST 49	LT 106	AT 10	LT 106	AT 75	AT 75	LT 106	AT 10	LT 106	ST 49					ST 49	FT 66	ST 49	LT 106	AT 10	LT 106	AT 75	AT 75	LT 106	AT 10	LT 106	ST 49	XT 10	ST 49	XT 10		
K																																		

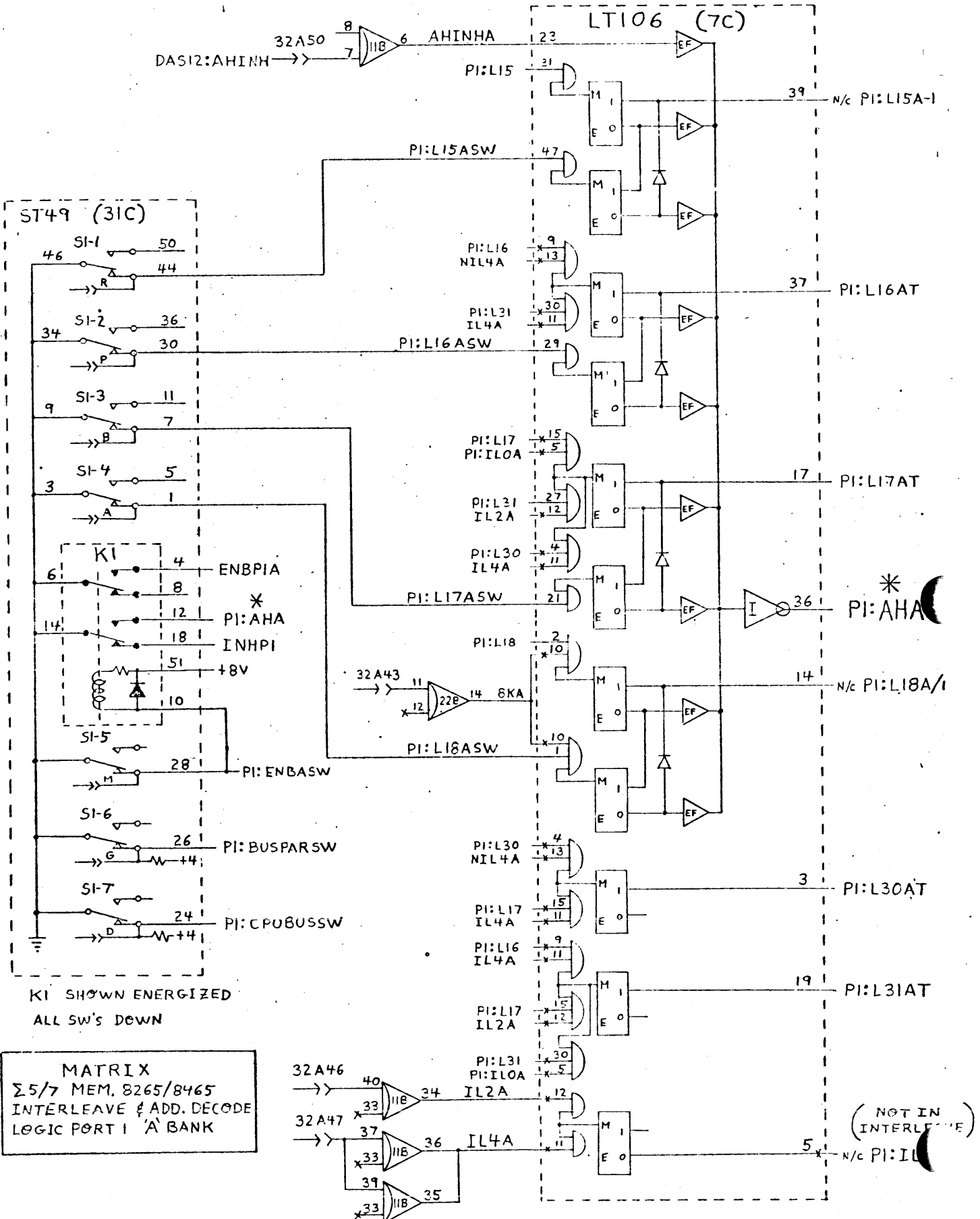
1-8 = PORT INTERFACE CABLES
 * = REMOVE IF NO 'B' BANK S1 OR S2
 1A-8A = STARTING ADD. SW'S 'A' BANK
 1B-8B = STARTING ADD. SW'S 'B' BANK
 9 = REMOVE IF RESPECTIVE PORT NOT IMP.
 ALSO APPLIES TO S1 MATRIX

ST49	
64K	L15 STARTING
32K	L16 ADDRESS'S
16K	L17
8K	L18
INHP	PORT DISABLE
BUSS	PORT CAN SEND OR
PARITY	RECEIVE M32
CPU	ENABLES MF FROM
BUSS	DRIVER TO PE BUSS

SHEET 1 of 2

10/20/70
COCHRANE

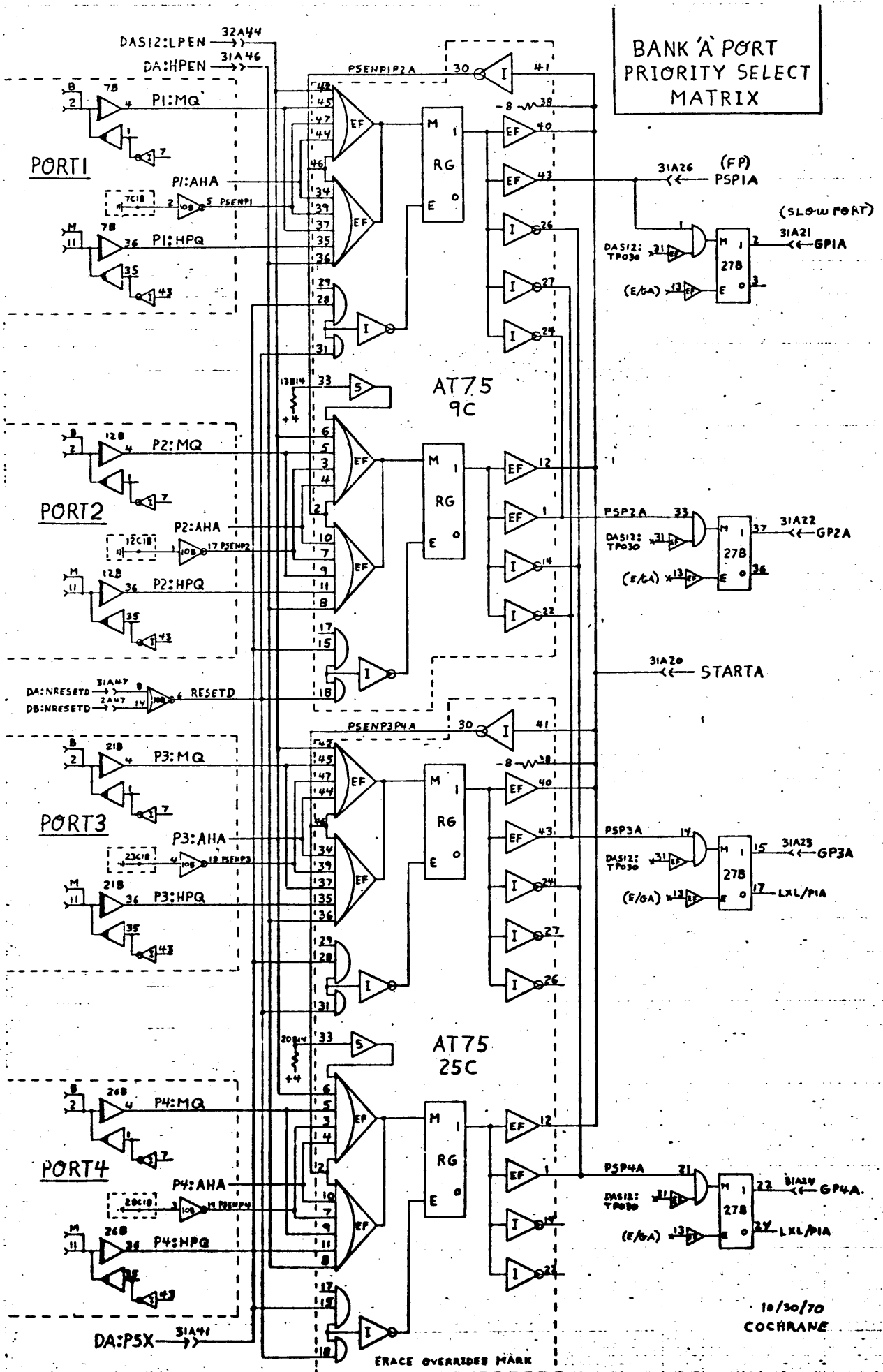
10



KI SHOWN ENERGIZED
ALL SW'S DOWN

MATRIX
Σ5/7 MEM. 8265/8465
INTERLEAVE & ADD. DECODE
LOGIC PORT 1 'A' BANK

(NOT IN INTERLEAVE)



BANK 'A' PORT PRIORITY SELECT MATRIX

PORT 1

PORT 2

PORT 3

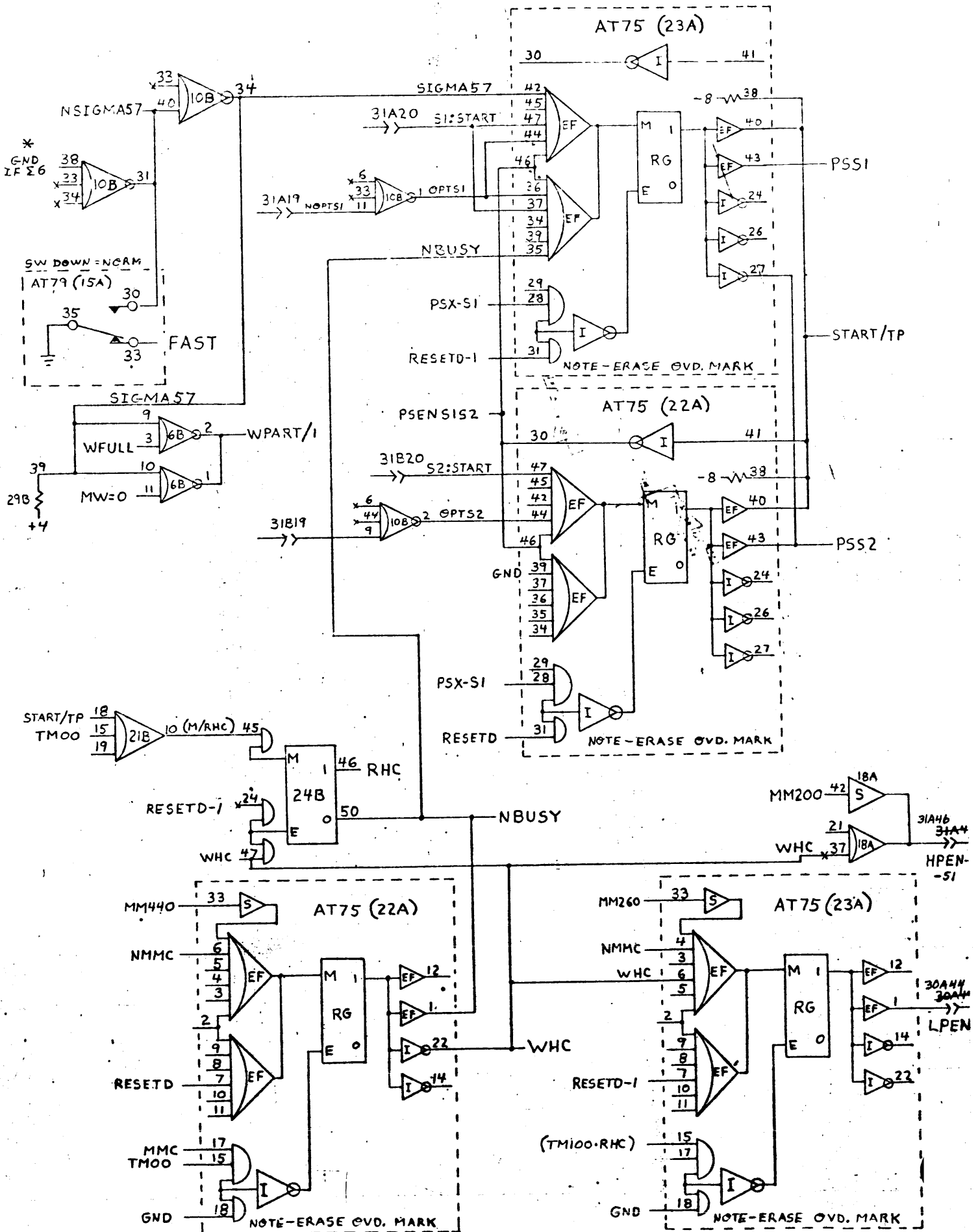
PORT 4

AT75 9C

AT75 25C

10/30/70
COCHRANE

ERASE OVERRIDES MARK



Σ 5/7 MEM. 8265/8465
 DRIVER 'A' or 'B'
 Page 3-206

11/27/70
 COCHRANE

STAPLE

STAPLE

FOLD

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